Microelectronics

Introduction to the IC technology

M.Rencz

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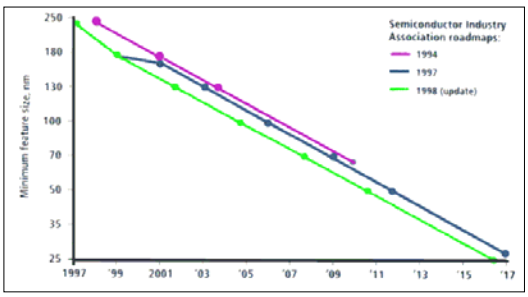
Integrated circuits

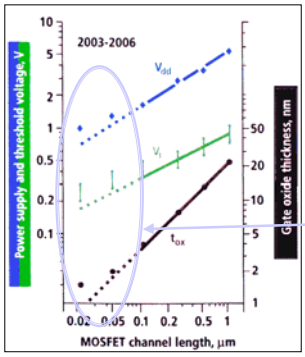
Development is controlled by the „*roadmaps*". Self-fulfilling predictions *for the tendencies of development.*

1. Roadmap requirements for IC fabrication			
Year	1997-2001	2003-2006	2009-2012
Semiconductor technology needs			
Feature size, nm	250-150	130-100	70-50
Millions of transistors per square centimeter	4-10	18-39	84-180
Number of wiring layers	6-7	7-8	8-9
Assembly and packaging technology needs			
Pad pitch, nm	250-150	130-100	70-50
Cents per pin	0.7-2.3	0.5-1.8	0.4-1.3
Power, W	1.2-61	2-96	2.8-109
Die size, mm^2	50-385	60-520	70-750
Performance, MHz	200-730	530-1100	840-1830
Voltage, V	1.2-2.5	0.9-1.5	0.5-0.9
Pin count	100-900	160-1475	260-2690

Source: National Technolgy Roadmap for Semiconductors

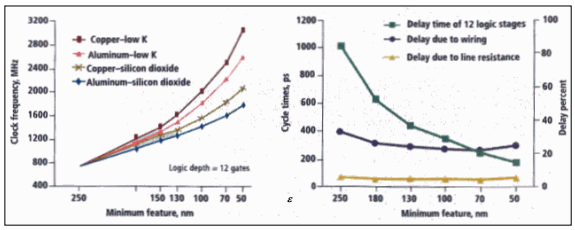


Expected decrease in line width



Oxide thickness, Power supply and threshold voltage tendencies

Approaching physical limits



Interconnect resulted delay has to be decreased. The delay is proportional to the R and C of the interconnect lines. (see later)

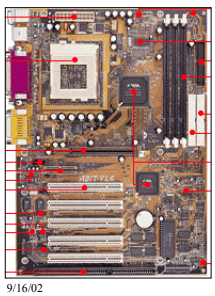
Decreasing R: ***copper*** instead of *Al*

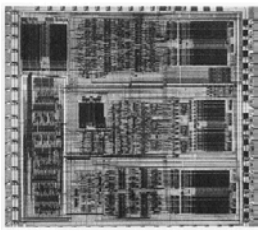
Decreasing C: lower ε insulator instead of SiO_2

$$\varepsilon_r\big|_{SiO2} = 3.9$$

VLSI rudiments

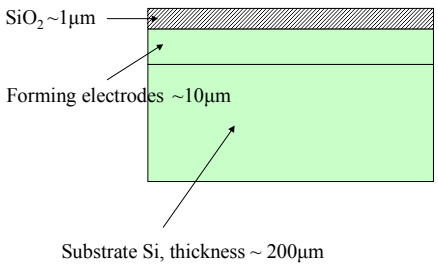
Packaged integrated circuits on a PCB
(Computer motherboard)



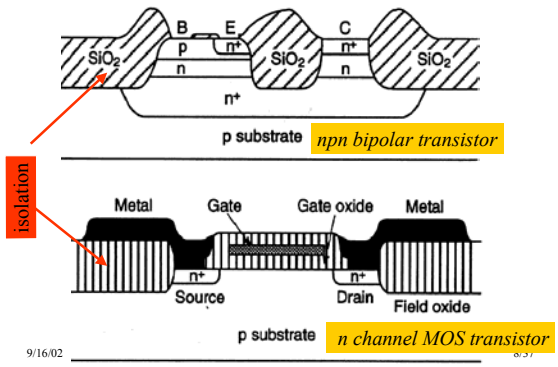


Microprocessor chip layout

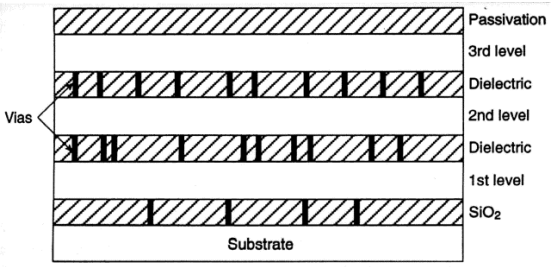
Cross-section of a chip



Cross-section of transistors



Cross-section of a 3 layer interconnect (5-6 metal layers are usual today)



Forming the vertical structure: technology
Forming the horizontal structure: design
separated in space and time

Their relationship is given by the ***Design rules*** referring to the technology.

Fabricating VLSI circuits: the
planar technology

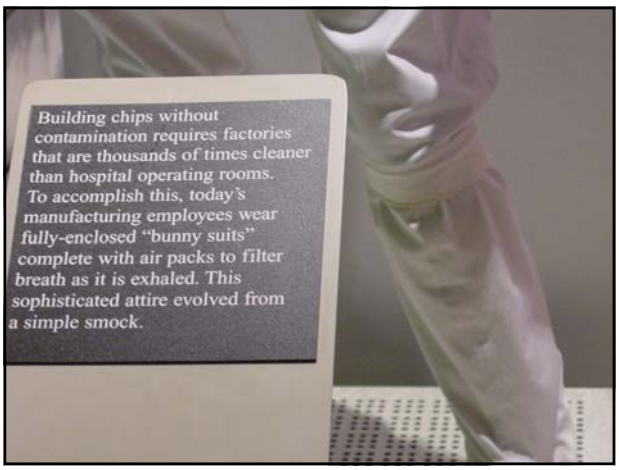
Planar: refers to the fact that all the circuits are fabricated in a plane
Base: *the silicon single crystal, fabricated in bars*. The 2-12" diameter large, about 0.25 mm thick *wafers* are sliced from these. On one wafer several thousands of IC chips or dies are fabricated at the same time

Finished wafers before dicing

The group of wafers processed together: a *party*

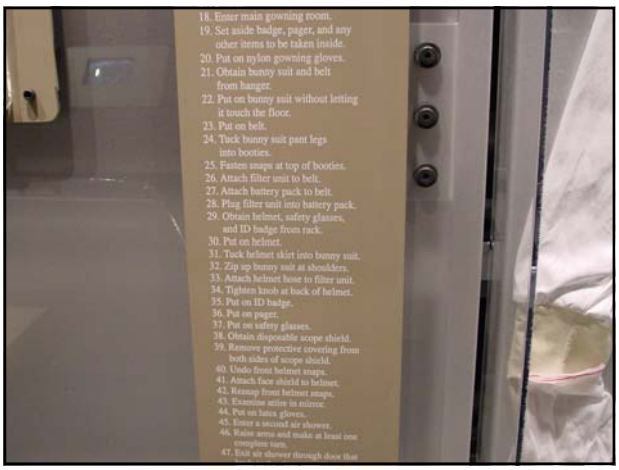
A party is being put into a furnace

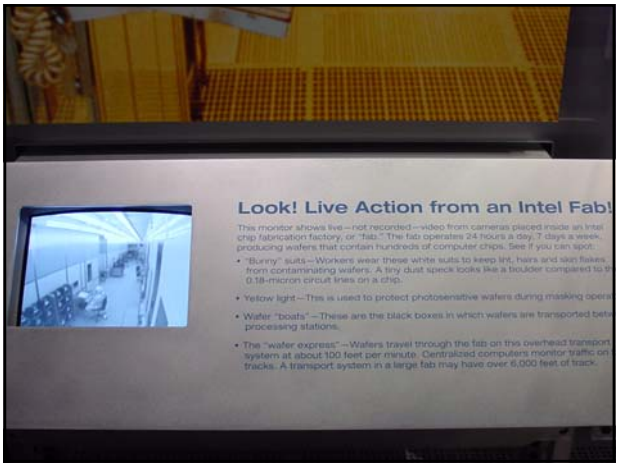
Very high cleanness requirements: *clean rooms*

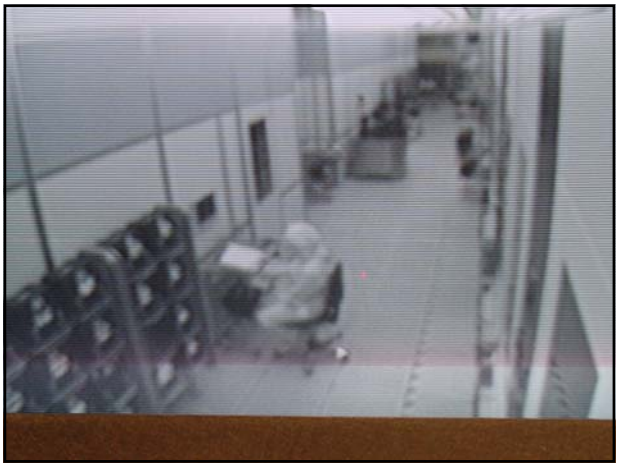

Building chips without contamination requires factories that are thousands of times cleaner than hospital operating rooms. To accomplish this, today's manufacturing employees wear fully-enclosed "bunny suits" complete with air packs to filter breath as it is exhaled. This sophisticated attire evolved from a simple smock.


EXIT


Suiting Up
This is a typical sequence of steps that everybody who plans to enter a fab must follow:
1. Store personal items.
2. Discard any gum, candy, etc.
3. Remove any makeup with clean room soap and water.
4. Take a drink of water to wash away throat particles.
5. Cover any facial hair with a surgical mask or beard/mustache cover.
6. Put on a lint-free head cover.
7. Clean shoes with shoe cleaners.
8. Place shoe covers over street footwear.
9. Enter an air shower designed to blow off loose particles.
10. Exit air shower and enter shoe change room.
11. Clean any small, pre-approved items to be taken inside.
12. Pick up booties.
13. Sit on "dirty" side of bench.
14. Put on one bootie.
15. Swing bootied foot to "clean" side of bench.
16. Put on other bootie on "dirty" side.
17. Swing bootied foot to "clean" side.
18. Enter main gowning room.
19. Set aside badge, pager, and any other items to be taken inside.
20. Put on nylon gowning gloves.
21. Obtain bunny suit and belt from hanger.
22. Put on bunny suit without letting it touch the floor.


18. Enter main gowning room.
19. Set aside badge, pager, and any other items to be taken inside.
20. Put on nylon gowning gloves.
21. Obtain bunny suit and belt from hanger.
22. Put on bunny suit without letting it touch the floor.
23. Put on belt.
24. Tuck bunny suit pant legs into booties.
25. Fasten snaps at top of booties.
26. Attach filter unit to belt.
27. Attach battery pack to belt.
28. Plug filter unit into battery pack.
29. Obtain helmet, safety glasses, and ID badge from rack.
30. Put on helmet.
31. Tuck helmet skirt into bunny suit.
32. Zip up bunny suit at shoulders.
33. Attach helmet hose to filter unit.
34. Tighten knob at back of helmet.
35. Put on ID badge.
36. Put on pager.
37. Put on safety glasses.
38. Obtain disposable scope shield.
39. Remove protective covering from both sides of scope shield.
40. Undo front helmet snaps.
41. Attach face shield to helmet.
42. Resnap front helmet snaps.
43. Examine attire in mirror.
44. Put on latex gloves.
45. Enter a second air shower.
46. Raise arms and make at least one complete turn.


Look! Live Action from an Intel Fab!
This monitor shows live—not recorded—video from cameras placed inside an Intel chip fabrication factory, or "fab." The fab operates 24 hours a day, 7 days a week, producing wafers that contain hundreds of computer chips. See if you can spot:
• "Bunny" suits—Workers wear these white suits to keep lint, hairs and skin flakes from contaminating wafers. A tiny dust speck looks like a boulder compared to th 0.18-micron circuit lines on a chip.
• Yellow light—This is used to protect photosensitive wafers during masking opera
• Wafer "boats"—These are the black boxes in which wafers are transported betw processing stations.
• The "wafer express"—Wafers travel through the fab on this overhead transport system at about 100 feet per minute. Centralized computers monitor traffic on tracks. A transport system in a large fab may have over 6,000 feet of track.



Microelectronics fabrication process

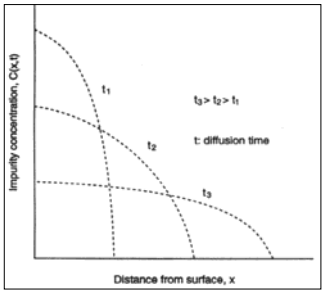
A sequence of
- doping,
- deposition
- lithographic

process steps

Doping procedures: aims at changing the doping at certain volumes of the semiconductor

methods:
- diffusion
- ion implantation

Diffusion: as a result of the elevated temperature (about.1000°C) the dopant atoms from the ambient diffuse into the silicon at the locations where this is not prevented by SiO_2. The ***silicon dioxide „masks"*** against the diffusion.



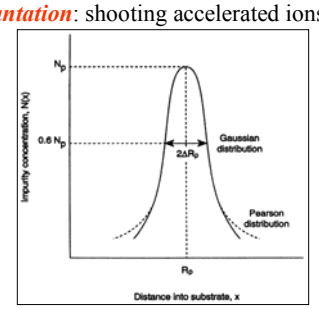
Doping profile after diffusion

x = 0 is the surface, x points perpendicularly inwards the Si

The doping of the surface layers is stronger

Side diffusion has to be considered

Ion implantation: shooting accelerated ions into the Si



Doping profile after ion implantation

x = 0 is the surface, x points perpendicularly inwards the Si

Advantages of ion-implantation over the diffusion

- higher accuracy,
- low temperature operation
- no size difference between the mask and the doped surface area

disadvantages:

- damaged crystal structure
- less productive than diffusion

Layer deposition steps

Chemical or physical methods to produce contiguous layer on the surface

Oxidation

Production of SiO_2 layer on the surface of Si in oxygen ambience at about 1000°C temperature. The SiO_2 layer on the surface is perfect conductor, behaving selectively against chemicals

The double role of SiO_2

1. Fabrication technological (masks)
2. Electronic
   - insulation between the surface layers (Thick oxide)
   - dielectric of MOS transistors (thin oxide)

Epitaxial layer deposition

Forming of a Si layer on the surface that continues the single crystal structure, but e.g. with lower doping density 1200°C temp.process.

CVD (Chemical Vapor Deposition)

deposition of amorphous or polycrystalline Si onto the surface

PVD (Physical Vapor Deposition)

For the deposition of metal layers (evaporation or sputtering)

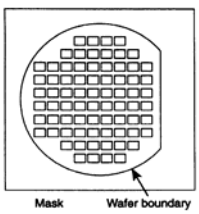
Steps of the lithography

To form the patterning in the SiO_2

Steps

- photoresist deposition on the surface
- patterning
- oxide etching

Chip patterns: *reticle*, wafer patterns ***masks***.



- Photo-technical steps
- Illumination through the masks
- The mask patterns imaged into the SiO_2
- New masks for all the technological steps →a technology is defined by a ***series of masks***
- Pattern data are produced by CAD programs

Possibilities for wafer patterning

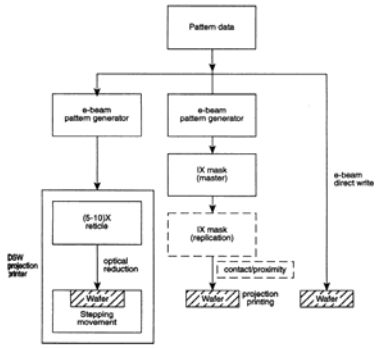
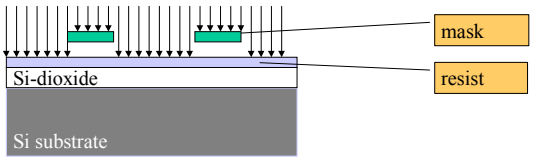
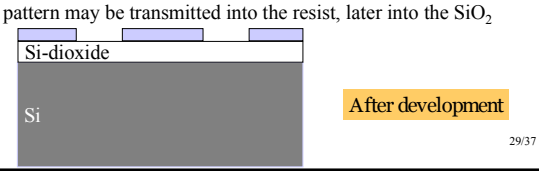


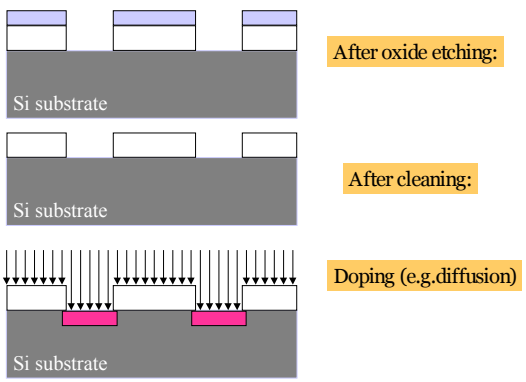
Photo-lithographic steps

Patterning the SiO_2



At the illuminated areas the photo-resist polymerises, → becomes resistive against certain chemicals, so that the mask pattern may be transmitted into the resist, later into the SiO_2



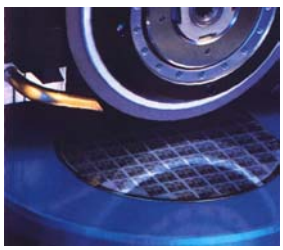


The SiO_2 pattern masks against the diffusion

Individual steps

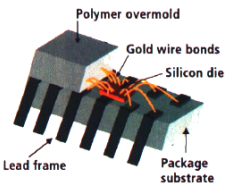
Wafer operations are group operations→ cheap.
Individual operations are expensive, should be minimised.
Most of the testing steps have to be carried out on the wafer, the bad chips must not be packaged

Dicing

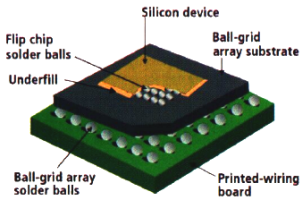


Packaging

The most frequent packaging methods



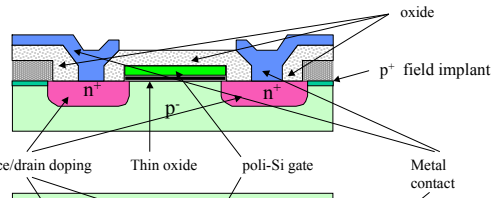
Wire bonded



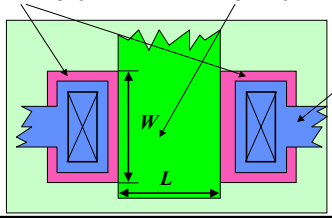
flip chip

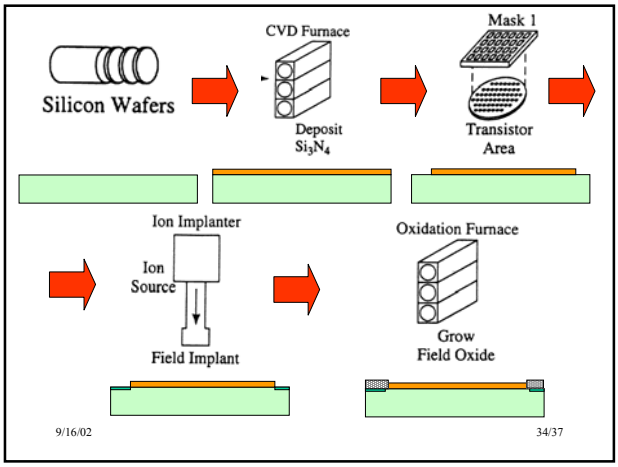
MOS IC fabrication steps

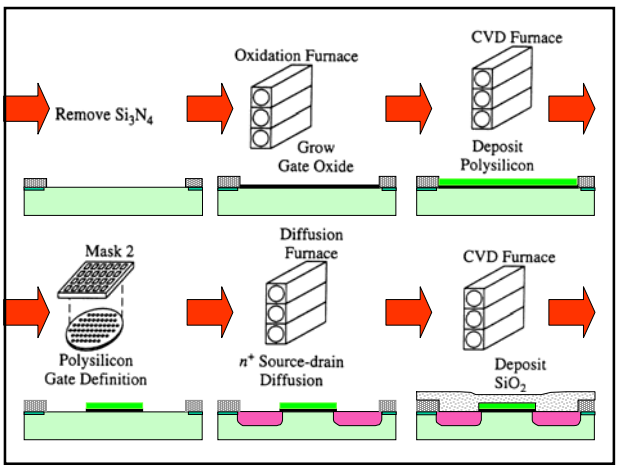
The structure:

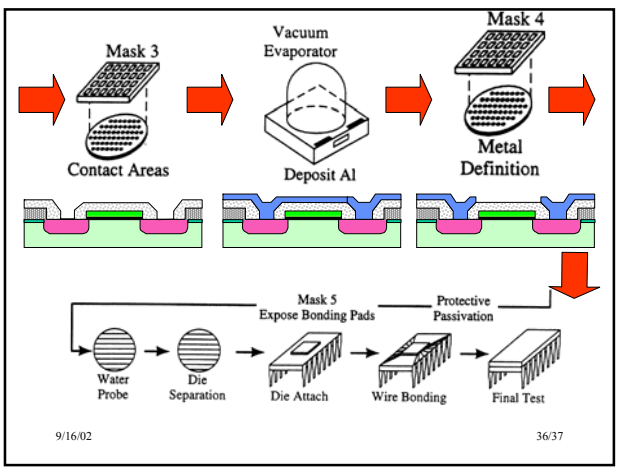


Layout:




Silicon Wafers
CVD Furnace
Deposit Si_3N_4
Mask 1
Transistor Area
Ion Implanter
Ion Source
Field Implant
Oxidation Furnace
Grow Field Oxide
9/16/02
34/37


Remove Si_3N_4
Oxidation Furnace
Grow Gate Oxide
CVD Furnace
Deposit Polysilicon
Mask 2
Polysilicon Gate Definition
Diffusion Furnace
n^+ Source-drain Diffusion
CVD Furnace
Deposit SiO_2


Mask 3
Contact Areas
Vacuum Evaporator
Deposit Al
Mask 4
Metal Definition
Mask 5
Expose Bonding Pads
Protective Passivation
Water Probe
Die Separation
Die Attach
Wire Bonding
Final Test
9/16/02
36/37

Example: detail of a fabricated IC,
electron-microscopic image