Application Report
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Electrostatic Discharge (ESD)

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ABSTRACT

This application report provides an overview of electrostatic-discharge (ESD) test models, failure modes, protection strategies, and Texas Instruments (TI) procedures to guard against ESD failures.

Contents

Introduction **2**
What is ESD? 2
ESD Test Models 2
Human-Body Model (HBM) 2
Machine Model (MM) 2
Charged-Device Model (CDM) 3
ESD Failures **3**
Latent Failures 3
ESD Failure Modes 3
ESD Protection Strategy **4**
ESD Protection Methods 4
ESD Design Rules 5
ESD Design Checker 5
ESD Protection Analysis 6
ESD Avoidance 6
ESD Control Program 6
Training and Certification 7
ESD Team 7
Audit Compliance 7
TI ESD Handling Procedures 7
References **7**

Introduction

There is growing interest in the effects of ESD on the performance of semiconductor integrated circuits (ICs) because of the impact ESD has on production yields and product quality. ESD problems are increasing in the electronics industry because of the trends toward higher speed and smaller device sizes. ESD is a major consideration in the design and manufacture of ICs. Texas Instruments (TI) always has been at the forefront of driving improvements in ESD protection and control, minimizing yield losses and field failures, and maintaining its reputation as a supplier of high-quality, reliable products.

What is ESD?

Static charge is an unbalanced electrical charge at rest. Typically, it is created by insulator surfaces rubbing together or pulling apart. One surface gains electrons, while the other surface loses electrons. This results in an unbalanced electrical condition known as static charge. When a static charge moves from one surface to another, it becomes ESD. ESD is a miniature lightning bolt of charge that moves between two surfaces that have different potentials. It can occur only when the voltage differential between the two surfaces is sufficiently high to break down the dielectric strength of the medium separating the two surfaces. When a static charge moves, it becomes a current that damages or destroys gate oxide, metallization, and junctions. ESD can occur in any one of four ways: a charged body can touch an IC, a charged IC can touch a grounded surface, a charged machine can touch an IC, or an electrostatic field can induce a voltage across a dielectric sufficient to break it down.

ESD Test Models

ESD can have serious detrimental effects on all semiconductor ICs and the system that contains them. Standards are developed to enhance the quality and reliability of ICs by ensuring all devices employed have undergone proper ESD design and testing, thereby minimizing the detrimental effects of ESD. Three major test methods are widely used in the industry today to describe uniform methods for establishing ESD-withstand thresholds (highest passing level). They are:

Human-Body Model (HBM)

The HBM was developed to simulate the action of a human body discharging accumulated static charge through a device to ground, and employs a series RC network consisting of a 100-pF capacitor and a 1500-Ω resistor.

Machine Model (MM)

The MM simulates a machine discharging accumulated static charge through a device to ground. It comprises a series RC network of a 200-pF capacitor, and nominal series resistance of less than 1 ohm. The output waveform usually is described in terms of peak current and oscillating frequency for a given discharge voltage.

Charged-Device Model (CDM)

The CDM simulates charging/discharging events that occur in production equipment and processes. Potential for CDM ESD events occur when there is metal-to-metal contact in manufacturing. One of many examples is a device sliding down a shipping tube and hitting a metal surface. The CDM addresses the possibility that a charge may reside on a lead frame or package (e.g., from shipping) and discharge through a pin that subsequently is grounded, causing damage to sensitive devices in the path. The discharge current is limited only by the parasitic impedance and capacitance of the device. CDM testing consists of charging a package to a specified voltage, then discharging this voltage through the relevant package leads. At TI, the CDM testing is conducted using a field-induced CDM (FCDM) simulator.

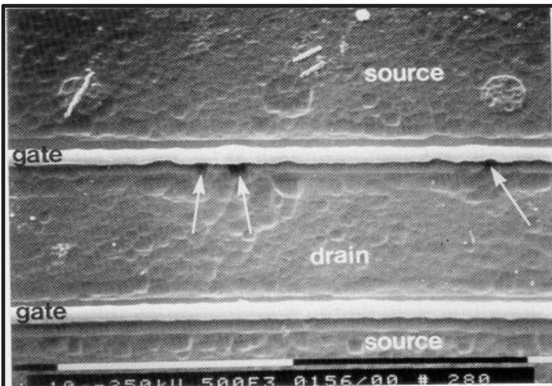
ESD Failures

Latent Failures

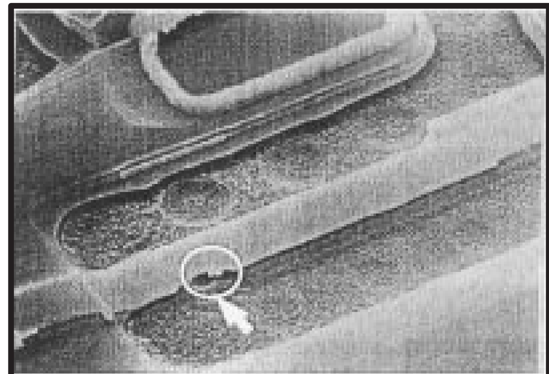
ESD events not only reduce assembly yields, but also can produce device damage that goes undetected by factory testing, and later, is the cause of a latent failure. These devices with latent ESD defects are called walking wounded because they have been degraded, but not destroyed, by ESD. This occurs when an ESD pulse is not sufficiently strong to destroy a device, but nevertheless causes damage. Often, the device suffers junction degradation through increased leakage or a decreased reverse breakdown, but the device continues to function and is still within data-sheet limits. A device can be subjected to numerous weak ESD pulses, with each successive pulse further degrading a device until, finally, there is a catastrophic failure. There is no known practical way to screen for walking-wounded devices. To avoid this type of damage, devices must be given continuous ESD protection, as outlined later in this application report.

ESD Failure Modes

Different ESD models tend to produce different types of failure and require different types of control and protection. Basic failure mechanisms include oxide punchthrough, junction burnout, and metallization burnout. Some typical ESD damage phenomena are shown in figure 1.



Drain-junction damage in an NMOS after HBM stress. Note the thermal damage to silicon.



Gate-oxide damage to an input buffer after CDM stress. Note the rupture in gate oxide.

Figure 1. Typical ESD Damage

ESD Protection Strategy

IC chips are protected by a strategy to discharge the ESD events that might occur on any pin of the package that is exposed to its environment. Furthermore, the protection strategy involves consideration of HBM, MM, and CDM events. For every new technology, the protection-element building blocks are first characterized through test chips, then appropriate protection schemes are formulated. These schemes are analyzed for their effectiveness through a second phase of testing chips before implementing resultant designs in production chips. The protection designs and their variations for the different signal and power pins of the IC chip are selected based on the required applications. Simulations also are used, where appropriate, to ensure the effectiveness of the scheme and its compatibility with the pin it is designed to protect. Before fully implementing the total-protection design and releasing it for fabrication, a software program *(ESD Checker)* is run. The purpose of the program is to detect design and layout errors that might contribute to ESD hazards.

ESD Protection Methods

The protection-device scheme considers all current paths to avoid thermal damage to silicon, either in the protection circuit or in the internal circuits, and all voltage-buildup scenarios are considered, in an effort to prevent gate-oxide damage. For example, a generalized scheme is shown in Figure 2, and the components are described in the following paragraphs.

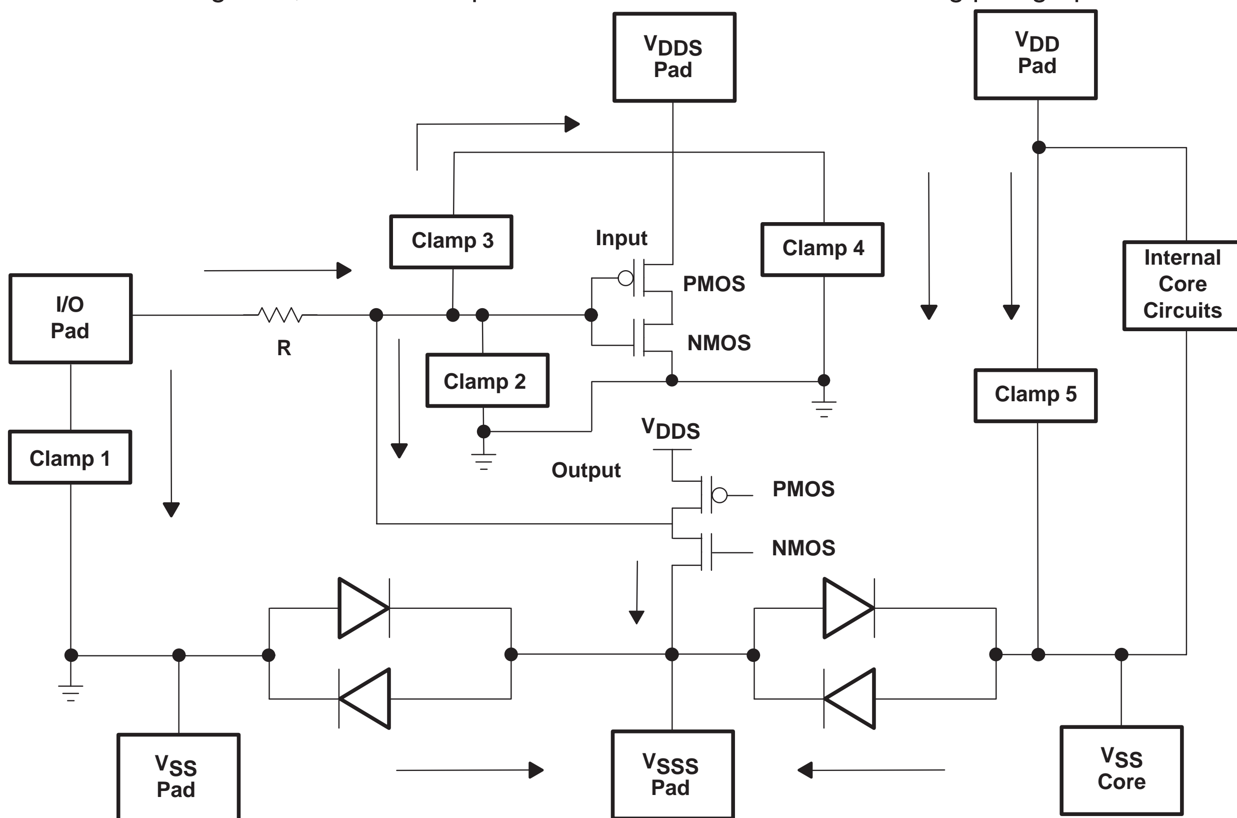


Figure 2. Overall Protection Method for HBM, MM, and CDM Methods

Clamp 1 is the primary protection device that protects against ESD surges at the I/O pad by clamping the voltage and allowing the high ESD current to be discharged safely to the ground terminal. The clamp design is selected based on the technology and the application specifications of the I/O signal circuitry. This clamp is essential for HBM, MM, and CDM methods.

Clamp 2 is isolated by resistor R, and its main function is to protect the gate oxide of the input NMOS buffer. Clamp 2 also triggers primary Clamp 1. At the same time, resistor R is chosen carefully to limit current to the output buffer and protect the buffer transistors, as well as to satisfy the output-buffer operational requirements. This clamp is essential and is particularly critical for the CDM method.

Clamp 3 is important in protecting the PMOS input buffer gate. The design and implementation of this clamp is critical for CDM protection.

Clamps 4 and 5 protect all of the internal circuits between any power supply and ground. For different V_{DD} supplies, a clamp is placed at every site to ensure that all core and internal logic circuits are protected from an ESD event on the V_{DD} pads. The design of this clamp must take into consideration the burn-in voltage requirements, latchup requirements, and, in general, must ensure that electrical overstress (EOS) events do not cause failure. This clamp is essential for HBM, MM, and CDM methods.

Because IC designs use different ground references for noise isolation between the logic and the core, the ESD design must ensure that the current path is available for all stress combinations between an I/O pad and internal grounds. The diode implementation between the grounds thus allows effective ESD current flow. In essence, the diodes, along with the proper clamps to ground, provide effective protection for HBM and MM, as well as CDM methods.

ESD Design Rules

The protection design implementation becomes complicated for different I/O signal configurations. Also, placement of unrelated circuits near an I/O pad causes unexpected current paths through interactions and may render the protection device ineffective. The same could occur in the internal connections between the power supplies, preventing the power-supply clamp from operating. All of these issues are covered in ESD design documents so that product ESD design is addressed properly from the beginning.

ESD Design Checker

The layout and circuit connections of an IC product are very complex and can lead to numerous unexpected errors, even for simple ESD designs. The ESD checker is a sophisticated software tool developed by Texas Instruments to detect ESD design errors and enforce compliance to ESD rules. This tool ensures that, before a product is released for fabrication, all potential ESD violations are detected. The checker software also gives designers guidance to correct any errors that are detected.

ESD Protection Analysis

After a product has been processed, packaged devices are characterized for ESD with a thoroughly established corporate-wide methodology to comprehensively test every combination of stress for HBM, MM, and CDM, and to verify that no potential problems exist. If there are failures, the methodology defines the proper and efficient methods to debug the cause and identify any necessary design fixes. Failure analysis techniques are effectively used in the diagnosis. Product prequalification failures are analyzed fully to not only understand the phenomena, but also to establish new rules to avoid such failures in other products. The ESD-checker software and the ESD-design rules are updated for continuous ESD reliability improvement.

ESD Avoidance

Because ESD can occur only when different potentials are involved, the best way to avoid ESD damage is to keep the ICs at the same potential as their surroundings. The logical reference potential is ESD ground. So, the first and most important rule in avoiding ESD damage is to keep ICs and everything that comes in close proximity to them at ESD ground potential.

Four supplementary rules support this first rule:

- Any person handling ICs must be grounded either with a wrist strap or ESD protective footwear, used in conjunction with a conductive or static-dissipative floor or floor mat.
- The work surface where devices are placed for handing, processing, testing, etc., must be made of static-dissipative material and be grounded to ESD ground.
- All insulator materials either must be removed from the work area or they must be neutralized with an ionizer. Static-generating clothes should be covered with an ESD-protective smock.
- When ICs are being stored, transferred between operations or workstations, or shipped, they must be maintained in a Faraday-shield container whose inside surface (touching the ICs) is static dissipative.

ESD-Control Program

Semiconductor device technology trends and the evolution of factory automation and fine-pitch assembly continue to place greater pressure on all IC manufacturers to provide effective ESD controls. ESD-control management requires attention to effective and efficient implementation of static controls in manufacturing, distribution, maintenance and repair, and designing-in ESD-protection circuitry.

Three basic areas that are key to providing an effective ESD control program are:

- Manufacturing process controls, materials, and qualification
- Component qualification
- Awareness, corporate committee coordination, and external standards.

Training and Certification

ESD-awareness training is established to provide a basic understanding of ESD problems. It is open to all shop personnel, technicians, engineers, and management. All personnel who come in close proximity with ESD-sensitive ICs must receive more in-depth ESD training initially, and again each year, as a minimum. No ESD program can be successful unless people who handle ICs understand the need for ESD controls and are trained in local ESD control policies, procedures, and requirements.

ESD Team

The corporate-level ESD team consists of area coordinators who have overall responsibility for each facility's ESD-control program. Each coordinator is responsible for writing local ESD handling procedures, keeping them updated, ensuring ESD training completion, and material evaluation.

Audit Compliance

Periodic audits, ranging from daily to yearly, are held to ensure that all ESD handling procedures are being followed and that all ESD control products (e.g., wrist straps, heel straps, ionizers, table mats, floor mats, etc.) are functioning properly.

TI ESD-Handling Procedures

The TI worldwide ESD-handling procedures are available to customers upon request.

References

1. EIA-625A *Requirements for Handling Electrostatic Discharge Sensitive (ESDS) Devices*
2. EIA-541 *Packaging Material Standards for ESD Sensitive Items*
3. MIL-STD 883D *Method 3015.7 ”Military Standard for Test Methods and Procedures Microelectronics: ESD Sensitivity Classification*
4. JESD22-A114-B *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model*
5. JESD22-A115-A *Electrostatic Discharge (ESD) Sensitivity Testing Machine Model*
6. JESD22-C101-A *Field-Induced Charged-Device Model Test Method for Electrostatic Discharge Withstand Thresholds of Microelectronic Components*

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