Franco Maloberti

Layout of Analog
CMOS
Integrated Circuit
Part 3
Passive components: Resistors, Capacitors
Outline

- Introduction
- Process and Overview Topics
- Transistors and Basic Cells Layout
- Passive components: Resistors, Capacitors
- System level Mixed-signal Layout
Integrated Capacitors

Capacitors in IC are parallel plate capacitors

\[ C = \frac{\varepsilon_0 \varepsilon_r \ WL}{t_{ox}} \]

No fringing effect

<table>
<thead>
<tr>
<th>Material</th>
<th>Rel. Permittivity</th>
<th>Diel. Strength</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiO₂ Dry Oxide</td>
<td>3.9</td>
<td>11 V/nm</td>
</tr>
<tr>
<td>SiO₂ Plasma</td>
<td>4.9</td>
<td>3-6 V/nm</td>
</tr>
<tr>
<td>Si₃N₄ LPCVD</td>
<td>6-7</td>
<td>10 V/nm</td>
</tr>
<tr>
<td>Si₃N₄ Plasma</td>
<td>6-9</td>
<td>5 V/nm</td>
</tr>
</tbody>
</table>

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Types of Integrated Capacitors

- Poly-poly
- Sandwich
- Lateral plates (flux capacitor)
- Poly-diffusion
- Poly-channel
Features of Integrated Capacitors

Electrodes: metal; polysilicon; diffusion

Insulator: silicon oxide; polysilicon oxide; CVD oxide

\[ C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} WL \]

\[ \left( \frac{\Delta C}{C} \right)^2 = \left( \frac{\Delta \varepsilon_r}{\varepsilon_r} \right)^2 + \left( \frac{\Delta t_{ox}}{t_{ox}} \right)^2 + \left( \frac{\Delta L}{L} \right)^2 + \left( \frac{\Delta W}{W} \right)^2 \]

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Factor affecting accuracy

\[
\left( \frac{\Delta \varepsilon_r}{\varepsilon_r} \right) \quad \text{• Oxide damage}
\]

\[
\left( \frac{\Delta t_{\text{ox}}}{t_{\text{ox}}} \right) \quad \text{• Grow rate}
\]

\[
\left( \frac{\Delta L}{L} \right) ; \left( \frac{\Delta W}{W} \right) \quad \text{• Etching}
\]

- Impurities
- Bias condition
- Bias history (for CVD)
- Stress
- Temperature
- Poly grain size
- Etching
- Alignment
To achieve good matching:

- Use of unity capacitors connected in parallel
- Use $W = L$ fairly large

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Flux Capacitor Layout

- Use of the same metal layer
- Exploit the lateral flux
- The parasitic capacitance plate-substrate is low because the metal sits on thick oxide
- Use thick metal layers
- Maximize the perimeter (use of fractals)
- Very good matching!
Common Centroid Structures

\[ C_2 = C_1 \\
C_3 = 2C_1 \\
C_4 = 4C_1 \\
C_5 = 8C_1 \]
Matching of Capacitors

Matching accuracy is better than matched resistors, because:

- \( \frac{\Delta \varepsilon_r}{\varepsilon_r} \ll \frac{\Delta \rho}{\rho} \)

- \( \frac{\Delta W}{W}_{\text{cap}} < \frac{\Delta W}{W}_{\text{res}} \) (because the capacitors are square)

- \( \frac{\Delta t_{\text{ox}}}{t_{\text{ox}}} < \frac{\Delta x_j}{x_j} \)
W' = W - 2x
L' = L - 2x

Effective area:

A' = W'L' = WL - 2(L + W)x
A' = A - Px

The undercut effect gives the same proportional reduction if the perimeter-area ratio is kept constant.
Matched Capacitors: Exercise

Layout the following three capacitors

- $C_1 = 0.95\, \text{pF}$
- $C_2 = 1.24\, \text{pF}$
- $C_3 = 1.37\, \text{pF}$

The absolute accuracy is not important. What matters is the capacitance ratios.
Fringing Effect

- Equation: \( C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} WL \) is an approximation

\[ C = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} (W - t_{ox})(L - t_{ox}) + C_{fring} \]

- Fringing depends on the boundary conditions
## MOS Capacitors Features

<table>
<thead>
<tr>
<th>Type</th>
<th>$t_{ox}$ nm</th>
<th>Accuracy %</th>
<th>Temperature Coefficient ppm/°C</th>
<th>Voltage Coefficient ppm/V</th>
</tr>
</thead>
<tbody>
<tr>
<td>poly - diff.</td>
<td>15 - 20</td>
<td>7 - 14</td>
<td>20 - 50</td>
<td>60 - 300</td>
</tr>
<tr>
<td>poly I - poly II</td>
<td>15 - 25</td>
<td>6 - 12</td>
<td>20 - 50</td>
<td>40 - 200</td>
</tr>
<tr>
<td>metal - poly</td>
<td>500 - 700</td>
<td>6 - 12</td>
<td>50 - 100</td>
<td>40 - 200</td>
</tr>
<tr>
<td>metal - diff.</td>
<td>1200 - 1400</td>
<td>6 - 12</td>
<td>50 - 100</td>
<td>60 - 300</td>
</tr>
<tr>
<td>metal I - metal II</td>
<td>800 - 1200</td>
<td>6 - 12</td>
<td>50 - 100</td>
<td>40 - 200</td>
</tr>
</tbody>
</table>
## Parasitic Capacitances

<table>
<thead>
<tr>
<th></th>
<th>diffusion</th>
<th>poly-poly or poly-metal</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{p,b}$</td>
<td>0.05C</td>
<td>0.02 C</td>
</tr>
<tr>
<td>$C_{p,t}$</td>
<td>0.01C</td>
<td>0.005 C</td>
</tr>
</tbody>
</table>

High impedance node connected to the top plate

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Rules for Capacitor Matching

- Use identical geometries
- Use large unity capacitance (minimize fringing)
- Use common centroid arrangement
- Use dummy capacitors
- Use shielding
- Account for the connections’ contribution
- Don’t run connections over capacitor
- Place capacitor in low stress areas
- Place capacitors far from power devices
Integrated Capacitors

- Use unit capacitors
- Make bigger capacitors integer multiples of the unit capacitor
- Use common centroid layout to match capacitors
- Use multiple contacts to lower series resistance
A resistor is made of a strip of resistive layer.

\[
R = 2R_{\text{cont}} + \frac{L}{W} R^{\square}
\]

The endings resistance can be significant!
Diffused Resistances

a, b) diffusion

c) n-well (or p-well)

d) Pinched well
Polysilicon Resistances

Conductive layers can be used to shield the conductor-oxide-conductor structure.
Well or Pinched-well Resistors

- Well layers have a large specific resistance
  - but
  - They have a large voltage and temperature coefficient
  - They are weakly insulated from the surrounding
  - Layers close to the surface contribute to the conductivity
Large Value Resistors

In order to have large value resistors:

• Use of long strips (large L/W)
• Use of layers with high sheet resistance (bad performances)

Layout: rectangular “snake”

(!!)
Resistance at the corners
Current flows in different directions

DON’T USE IT IN PRECISE APPLICATIONS!
Prevent Current Leakage!

- N-Well
- Substrate bias
- n⁺ diffusion
- p⁺ diffusion

Prevents lateral leakage

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# Features of Resistors

<table>
<thead>
<tr>
<th>Type of layer</th>
<th>Sheet Resistance $\Omega/0$</th>
<th>Accuracy $%$</th>
<th>Temperature Coefficient $\text{ppm/}^\circ\text{C}$</th>
<th>Voltage Coefficient $\text{ppm/V}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>n + diff</td>
<td>30 - 50</td>
<td>20 - 40</td>
<td>200 - 1K</td>
<td>50 - 300</td>
</tr>
<tr>
<td>p + diff</td>
<td>50 - 150</td>
<td>20 - 40</td>
<td>200 - 1K</td>
<td>50 - 300</td>
</tr>
<tr>
<td>n - well</td>
<td>2K - 4K</td>
<td>15 - 30</td>
<td>5K</td>
<td>10K</td>
</tr>
<tr>
<td>p - well</td>
<td>3K - 6K</td>
<td>15 - 30</td>
<td>5K</td>
<td>10K</td>
</tr>
<tr>
<td>pinched n - well</td>
<td>6K - 10K</td>
<td>25 - 40</td>
<td>10K</td>
<td>20K</td>
</tr>
<tr>
<td>pinched p - well</td>
<td>9K - 13K</td>
<td>25 - 40</td>
<td>10K</td>
<td>20K</td>
</tr>
<tr>
<td>first poly</td>
<td>20 - 40</td>
<td>25 - 40</td>
<td>500 - 1500</td>
<td>20 - 200</td>
</tr>
<tr>
<td>second poly</td>
<td>15 - 40</td>
<td>25 - 40</td>
<td>500 - 1500</td>
<td>20 - 200</td>
</tr>
</tbody>
</table>
Resistor’s Accuracy

\[ R = \frac{L}{W} R_\square = \frac{L}{W} \cdot \frac{\bar{\rho}}{x_j} \]

If the parameters are statistically independent the standard deviation of the resistance is:

\[
\left( \frac{\Delta R}{R} \right)^2 = \left( \frac{\Delta L}{L} \right)^2 + \left( \frac{\Delta W}{W} \right)^2 + \left( \frac{\Delta \bar{\rho}}{\bar{\rho}} \right)^2 + \left( \frac{\Delta x_j}{x_j} \right)^2
\]

Since in general \( L >> W \)

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Resistor’s Accuracy (cont.)

\[
\begin{pmatrix}
\frac{\Delta \rho}{\rho}
\end{pmatrix}
\]
for polysilicon resistors is larger than for diffused resistors.

(Polysilicon is composed of a conglomerate of independently oriented grain of crystalline silicon)

Accuracy:

Absolute accuracy is poor because of the large parameter drift.

Ratio (or matching) accuracy is better because it depends on the local variation of parameters.
Factor Affecting Accuracy

\[
\left( \frac{\Delta \rho}{\rho} \right)
\]

- Polysilicon grain size
- Doping dose
- Crystal defects
- Stress
- Temperature

\[
\left( \frac{\Delta L}{L}, \frac{\Delta W}{W} \right)
\]

- Etching
- Boundary
- Side diffusivity

\[
\left( \frac{\Delta x_j}{x_j} \right)
\]

- Implant dose
- Side diffusivity
- Deposition rate
Plastic packages cause a large pressure on the die (= 800 Atm.). It determines a variation of the resistivity. For <100> material the variation is unisotropic, so the minimum is get if the resistance have a 45° orientation.

**Temperature:**

Temperature gradient on the chip may produce thermal induced mismatch.

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Effect of Etching

Wet etching: isotropic (undercut effect)
$H_F$ for SiO$_2$; $H_3$PO$_4$ for Al
$\Delta x$ for polysilicon may be 0.35 - 0.5 $\mu$m with standard deviation 0.02 $\mu$m.

Reactive ion etching (R.I.E.) (plasma etching associated to “bombardment”): unisotropic.
$\Delta x$ for polysilicon is 0.2 $\mu$m with standard deviation 0.015 $\mu$m

Boundary:
The etching depends on the boundary conditions
Use of dummy strips

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Side Diffusion

Contribution of Endings

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Exercise: draw a 121212121212 connection and compare the two solutions
Exercise: draw a common centroid structure (12 elements per resistor)
Resistor Guidelines

For matching:
- Use of equal structures
- Not too narrow \((W = 10\, \text{mm})\)
- Interdigitize
- Thermal effect compensation
- \(45^\circ\) orientation (if stressed)

For good TC:
- Use of \(n^+\) or \(p^+\) layers
- Use of poly layers

For absolute value:
- Use of diffused layers
- Suitable endings
Simple Model

Field oxide  T1  Poly  T2  Deposited oxide (ILO)

Substrate

(A)

T1  R1  T2

C1  C2

SUBS

(B)

T1  R1  R2  T2

C1  C2  C3

SUBS

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Metal Resistor

The sheet resistance of Al metallization is around 100 mΩ/□
Adjusting Resistor Values

Sliding contact: requires to change the contact mask only

Metal fuse and Poly-fuse

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Use of Fuses To Adjust Resistors

(A)  

F_1  

4R_{lsb}  

F_2  

2R_{lsb}  

F_3  

R_{lsb}  

Rx

(B)  

F_1  

R_{msb}  

F_2  

R_{msb}/2  

F_3  

R_{msb}/4  

Rx

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Rules for Resistor Matching

- Use the same material
- Identical geometry, same orientation
- Close proximity
- Interdigitate arrayed resistors
- Use dummy elements
- Place resistors in low stress area
- Place resistors away from power devices
- Use electrostatic shielding
- Use proper endings
Integrated Resistors

❖ Issue to remember
    ✷ Integrated resistors and features
    ✷ Resistor endings
    ✷ Make bigger resistors integer multiples of the unit resistor
    ✷ Finger two or more resistors for matching
    ✷ Do not snake a resistor; use metal to make turns
    ✷ Well under the resistor to shield from interference
    ✷ Substrate bias around the resistor