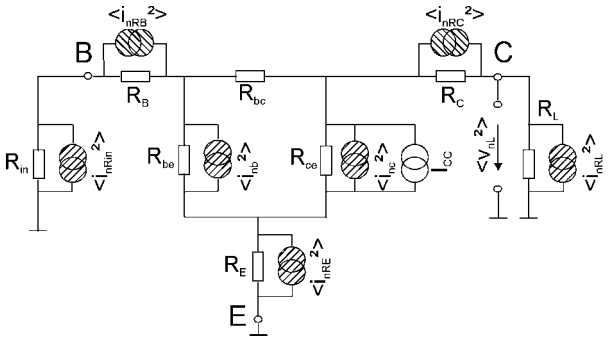
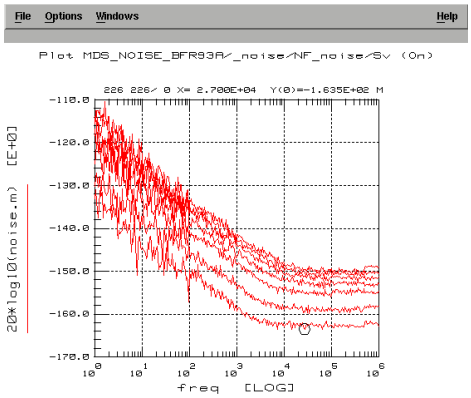
1/f Noise Modeling for Semiconductors

NOTE:
This docu describes the 1/f bipolar and MOS transistor toolkit before its implementation into IC-CAP as Agilent product number 85195B.





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1. Introduction

Phase noise of oscillator circuits is among the key parameters of today's communication systems. It limits the modulation quality of the information signal, and the cross-talk to adjacent channels. In the receiver, on the other hand, it can reduce the selectivity and the demodulation quality. With today's trend to even more complex modulation schemes, low phase noise becomes even more critical. Therefore, minimizing noise with the design of high frequency communications circuits is a must for the cost-effective exploitation of limited bandwidth, and to obtain low bit error rates.

In order to predict the noise behavior of such systems correctly, accurate noise models are required. Without them, the design and optimization of an amplifier's noise figure or the phase noise of oscillators cannot be successful.

A key element is the transistor. While for linear circuits the modeling of the noise at the operating frequency f_0 is sufficient, non-linear circuits do also convert the low-frequency noise up to the operating frequency range. For oscillators as an example, the 1/f low frequency noise at f_m will be mixed upwards to contribute to the phase noise of the total circuit at the frequencies f_0+f_m and f_0-f_m. Therefore, noise modeling of transistors can be split into a high and a low frequency segment. Fig.1 depicts the Collector low-frequency noise spectral density [A^2/Hz] of a bipolar transistor.

It can be seen that the resolution of the toolkit measurement setup is at about $0.2nA/\sqrt{Hz}$.

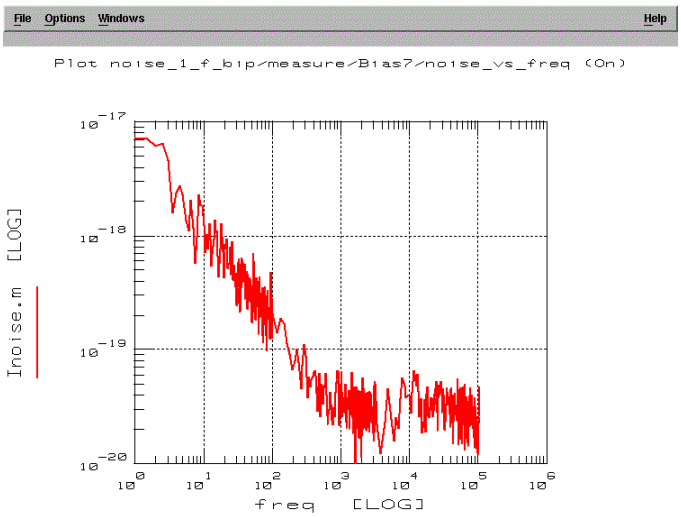


Fig.1: low frequency noise spectral density current of a bipolar transistor [A^2/Hz], measured at the Collector.

Broadband noise in bipolar or FET models is determined essentially by thermal noise and shot noise. These noise sources are automatically determined within the model from the large signal model parameters. An important prerequisite for this is, however, that the noise determining parameters, e.g. the Base resistor of bipolar transistors, has been determined carefully and that their values have a physical meaning. The low frequency noise, on the other hand, dominated by the 1/f noise, is modeled by some specific model parameters. In general, these are the AF and KF and sometimes BF/EF parameters, covered in this chapter. With some models, like the BSIM3v3, an alternate 1/f noise model is available too [10,15].

Since there is much confusion about noise terms, noise units etc., we will first commence with a small chapter on

Noise Terms Definitions

In order to keeps things simple, we consider white noise of a resistor. This frequency-independent and bias-independent noise is described in terms of a voltage by the well-known formula

$$\overline{v_{nR}^2} = 4 \cdot k \cdot T \cdot \Delta f \ * \ R$$

with

$\overline{v_{nR}^2}$	*effective noise voltage* (root means square value), in $[V^2]$
$4 \cdot k \cdot T \cdot \Delta f$	this product represents a power, with dimension [A*V]
R	resistance value

Since the term $4kT\Delta f$ represents a power, and if we normalize this power to Δf, we end up with a power density. Usually, this normalization is done for $\Delta f=1Hz$.

$$\frac{\overline{v_{nR}^2}}{\Delta f} = 4 \cdot k \cdot T \ * \ R$$

This result can be plotted against frequency. In case of our resistor, it is a constant value. For semiconductors, such a plot can also exhibit frequency dependencies, e.g. 1/f noise. In any case, such a plot shows a spectrum.

Therefore, this term $\frac{\overline{v_{nR}^2}}{\Delta f}$ is called *power noise spectral density*.

However, this is not exact, referring to the dimensions. A more appropriate term is therefore *voltage noise spectral density*. Its symbol is usually S_{nv}, and its dimension is $[V^2 / Hz]$

$$S_{nv} = \frac{\overline{v_{nR}^2}}{\Delta f} \quad = \quad 4 \cdot k \cdot T \ * \ R$$

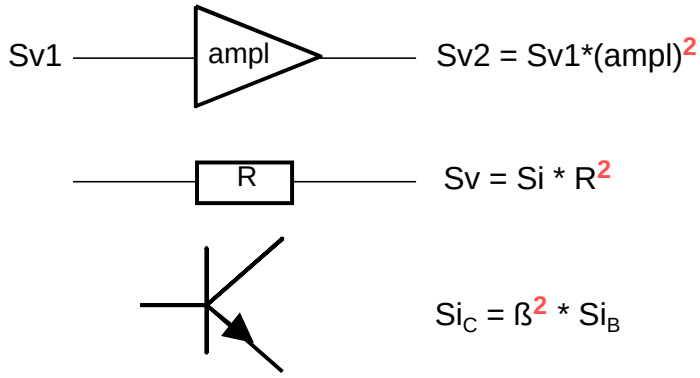
In some cases, the square root of S_{nv} is used, called the *equivalent noise voltage*, E_{nv} $[V/\sqrt{Hz}]$.

$$E_{nv} = \sqrt{\frac{\overline{v_{nR}^2}}{\Delta f}}$$

Note: using E_{nv} instead of S_{nv} does not require to calculate noise transmissions/amplifications using squares of R, amplification etc. See below.

Note: When expressing noise in terms of currents, e.g. $S_{ni} = \frac{\overline{i_{nR}^2}}{\Delta f} = 4 \cdot k \cdot T * \frac{1}{R}$, the same terminology applies.

Note: when performing circuit calculations based on *noise spectral densities*, keep in mind that you have to calculate with squares instead of the commonly used expressions!



2. Types of Noise in Semiconductors

This chapter deals with the description of the different noise mechanisms and their noise density spectrum in semiconductor components. It is basically aimed to highlight the main fundamentals rather than to explain the individual physical effects. We start with the thermal noise of the ohmic parasitics, and lead then over to the semiconductor-specific noise sources.

Thermal Noise

Related to the thermal oscillation of electrons in a resistor, we can measure a current at its contacts, without applying an external voltage. This is the thermal noise current. The effective current is described by

$$\overline{i_{nR}^2} = 4 \cdot k \cdot T \cdot \frac{1}{R} \cdot \Delta f \qquad (1)$$

An equivalent schematic for this condition is a noise-free resistor with a current noise source in parallel.

In analogy to this circuit, a noise-free resistor and a serial noise voltage source can be used as well. In this case, the effective voltage is given by

$$\overline{v_{nR}^2} = \overline{i_{nR}^2} * R^2 \overset{(1)}{=} 4 \cdot k \cdot T \cdot R \cdot \Delta f \qquad (2)$$

See fig. 2.

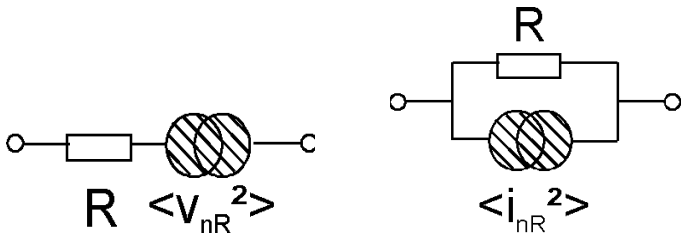


Fig. 2: equivalent schematic of a noisy resistor

Note: since noise sources have a mean value of '0', but an effective value of usually non-zero, effective voltages and currents are used to calculate the circuit performance with respect to the noise sources. This means that such an effective voltage is amplified by the square of the amplifier's gain! As another example, two parallel current noise sources can be represented by a single noise current source with a value of

$$\overline{i_{nR\_total}^2} = \overline{i_{nR1}^2} + \overline{i_{nR2}^2} \overset{(1)}{=} 4 \cdot k \cdot T \cdot \left(\frac{1}{R_1} + \frac{1}{R_2} \right) \cdot \Delta f$$

Also, the ohmic law is now referring to the square of voltages and currents, see equation (2).

Back to the thermal resistor noise, the equivalent noise power density spectra are

$$C_i(f) = 4 \cdot k \cdot T \cdot \frac{1}{R} \qquad (3)$$

and $$C_V(f) = 4 \cdot k \cdot T \cdot R \qquad (4)$$

These frequency independent noise spectra represent a simplification. An accurate calculation based on a quantum mechanic model gives

$$C_i(f) = 4 \cdot \frac{1}{R} \cdot h \cdot f \left(\frac{1}{2} + \frac{1}{e^{\frac{h \cdot f}{k \cdot T}} - 1} \right) \tag{5}$$

so that equations (1) to (4) are basically only valid for `h*f<<k*T` , i.e. for 'low' frequencies and high temperatures. However, the quantum noise for `h*f>>k*T` has to be considered basically only for frequencies very much higher than in RF and microwave applications, i.e. the $>10^{13}$Hz range.

Shot Noise

The current through the space charge area of a diode is composed of many individual current impulses, due to the transport of individual charge carriers. Since this motion of electrons/wholes is statistical, we always have, besides the expected DC current, also a noise component. With the assumption of individual, rectangular current impulses of the width τ for every charge component, we can calculate a power density spectrum after [1,2]

$$C_i(f) = 2 \cdot e \cdot I \cdot \frac{\sin^2(\pi \cdot f \cdot \tau)}{(\pi \cdot f \cdot \tau)^2} \tag{6}$$

For low frequencies, i.e. small values of $\tau * f$, there is `sin(x)/x ~ 1` and we get the commonly used equation

$$C_i^{NF}(f) = 2 \cdot e \cdot I \tag{7}$$

for the shot noise. Fig. 3 shows the equivalent schematic of an ideal, but noisy diode. The noise current is described by a current source in parallel with the small signal conductance.

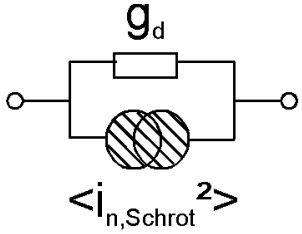


Fig.3: small signal equivalent schematic of diode noise

Generation-Recombination Noise

In semiconductors, there is a static charge carrier generation/recombination process. This refers to a statistic change of the carrier states. Referring to the energy band model, transitions between conduction and valence band as well as various trap levels are possible, leading to a noise spectrum following

$$C(f) = C_0 \cdot \frac{1}{1 + \left(\frac{f}{f_g} \right)^2} \tag{8}$$

The current dependency of the combination/recombination noise, also called burst-noise or popcorn-noise [3], is generally reflected by a modeling equation like

$$C(f) = KB \cdot \frac{I^{AB}}{1 + \left(\frac{f}{FB}\right)^2} \tag{9}$$

with the modeling parameters KB, AB and FB.

1/f Noise

A pretty often measurable phenomenon is noise with a spectrum proportional to 1/f. This leads to the name 1/f noise. Another name is flicker noise. It is caused essentially by recombination effects at defects in the semiconductor volume, the borders of diffusion areas or the material surface.

An empirical description after Hooge [4, 5] is a spectrum with

$$C_{1/f} = \frac{\alpha}{N_{tot}} \cdot \frac{1}{f} \tag{10}$$

where N_{tot} means the total number of moving charges in the device. The Hooge-Parameter α is a material characteristic.

In most simulation programs, the current dependency of the 1/f noise is covered in analogy to the generation/recombination noise by an exponential form like

$$C_{1/f} = KF \cdot \frac{I^{AF}}{f^{B}} \tag{11}$$

with the model parameters AF, KF and B. B is commonly set to '1'.

3. Noise Models in Simulation Programs

When simulating the noise behavior of circuits, all circuit components need to have noise models included. All lossy components will exhibit thermal noise, corresponding to the simulation temperature TEMP. Semiconductor devices will additionally also exhibit 1/f noise.

Resistors

Their noise distribution is modeled by white noise, as described above.
I.e., the effective current is described by

$$\overline{i_r^2} = 4 \cdot k \cdot T \cdot \frac{1}{R} \cdot \Delta f$$

representing a noise-free resistor with a current noise source in parallel.
Alternatively, a noise-free resistor and a serial noise voltage source can be used as well.

$$\overline{v_r^2} = 4 \cdot k \cdot T \cdot R \cdot \Delta f$$

Inductors, Capacitors, and Lines

are considered noise-free. This is valid for ideal components. For real RF components, including parasitic losses (SPICE sub-circuits), the noise contributions stem basically from the parasitic resistors.

Diodes

The main noise source of diodes is shot noise. Besides this, 1/f noise as well as thermal noise due to the parasitic resistor is observed. The capacitance C_{Diode}, covering the space charge and the diffusion capacitance, does not contribute to the noise.
This leads to a small signal schematic with the noise sources

$$\overline{i_D^2} = 2 \cdot e \cdot I_d \cdot \Delta f + KF \cdot \frac{I_d^{AF}}{f} \cdot \Delta f \qquad (12)$$

and

$$\overline{i_R^2} = 4 \cdot k \cdot T \cdot \frac{1}{R_{par}} \cdot \Delta f \qquad (13)$$

after fig.4. Since the shot noise formula refers directly to the diode current I_d and the thermal noise to the parasitic resistor R_{par} , it is only the parameters AF and KF which have to be modeled additionally.

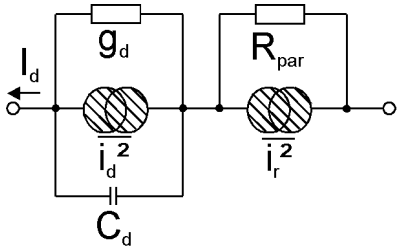


Fig. 4: noise equivalent schematic of a diode

Bipolar Transistors

SPICE and similar simulators feature a noise schematic for bipolar transistors after fig.5.

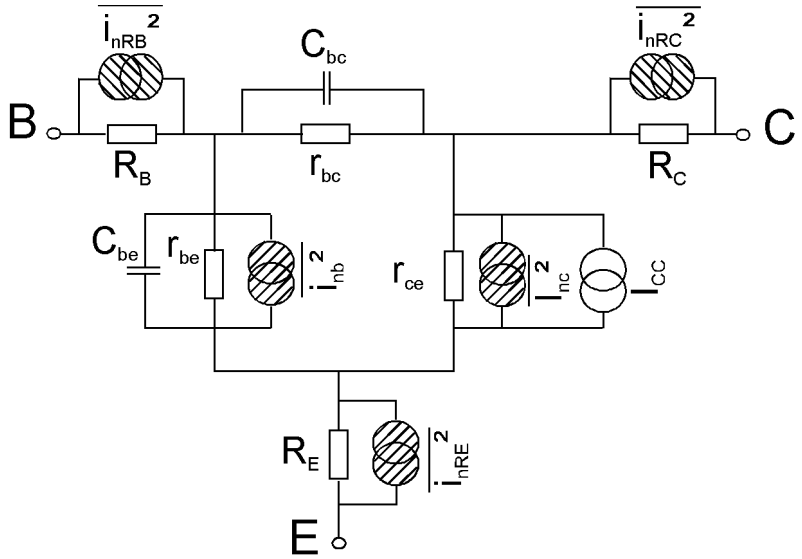


Fig.5: noise schematic of a bipolar transistor.

Associated with each physical resistor (R_b at the Base, R_c at the Collector and R_e at the Emitter), is a thermal noise source

$$\overline{i_{R,i}^2} = 4 \cdot k \cdot T \cdot \frac{1}{R_i} \cdot \Delta f , \quad i = b, c, e \tag{14}$$

Base and Collector currents are considered to be independent. Therefore, the shot noise can be described by a source

$$\overline{i_{b,S}^2} = 2 \cdot e \cdot I_b \cdot \Delta f \tag{15}$$

at the Base and

$$\overline{i_{c,S}^2} = \overline{i_{nc}^2} = 2 \cdot e \cdot I_c \cdot \Delta f \tag{16}$$

at the Collector. The total 1/f noise of the transistors is described by a noise source in parallel with the Base-Emitter contact. This leads to the noise source at the Base following

$$\overline{i_{nb}^2} = 2 \cdot e \cdot I_b \cdot \Delta f + KF \cdot \frac{I_b^{AF}}{f} \cdot \Delta f \tag{17}$$

with, again, the noise model parameters AF and KF.

Agilent's Advanced Design System (ADS) include with the BJT transistor model additionally a generation/recombination noise effect in the noise spectrum of the Base. Referring to equ. (17), this means

$$\left(\overline{i_{nb}^2}\right)^{ADS,BJT} = 2 \cdot e \cdot I_b \cdot \Delta f + KF \cdot \frac{I_b^{AF}}{f} \cdot \Delta f + KB \cdot \frac{I_b^{AB}}{1+\left(\frac{f}{FB}\right)^2} \cdot \Delta f \tag{18}$$

with the new model parameters KB, AB and FB.

With PSPICE, the Collector current i_c includes an additional 1/f noise source. This gives

$$\left(\overline{i_{nc}^2}\right)^{PSPICE} = 2 \cdot e \cdot I_c \cdot \Delta f + KF \cdot \frac{I_c^{AF}}{f} \cdot \Delta f \qquad (19)$$

using the same parameters KF and AF of the Base contact.

The VBIC model for bipolar transistors [6] includes, similar to the UCB SPICE BJT model, thermal noise sources as well as shot noise for the Base-Emitter current and the transport current. The 1/f noise is described again by a noise source between Base and Emitter. With

$$\left(\overline{i_{nb}^2}\right)^{VBIC} = 2 \cdot e \cdot I_b \cdot \Delta f + KF \cdot \frac{I_b^{AF}}{f^{BF}} \cdot \Delta f \qquad (20)$$

however, the frequency dependence is additionally modeled by the parameter BF. Besides the main NPN transistor, VBIC includes also a parasitic PNP transistor. Its noise contribution is modeled in analogy to the NPN, sharing the same model parameters for the 1/f noise. More details can be found in [7,8].

Noise in the MEXTRAM model is described like with the SPICE BJT model [9]. Besides thermal noise, there are shot noise sources associated with the Base-Emitter current as well as the transport current.. 1/f noise is described after (17).

Junction FETs

The noise schematic of field effect transistors is most often like in fig.6 [3].

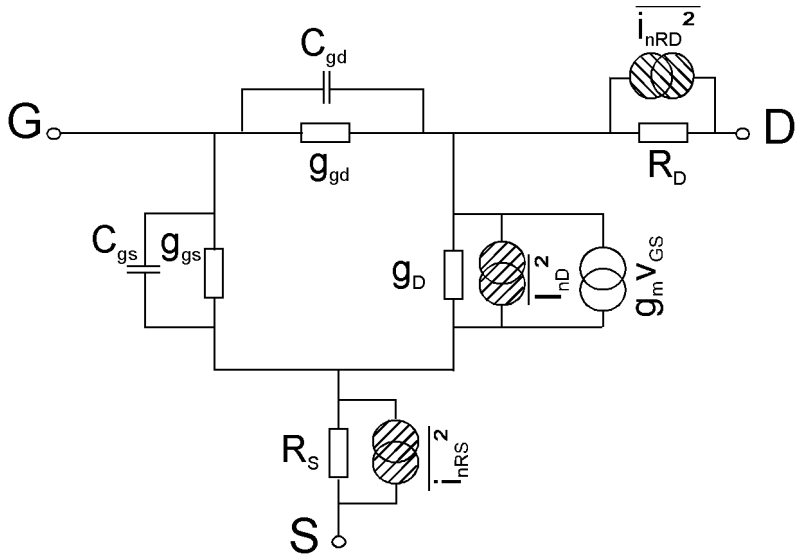


Fig.6: Noise equivalent schematic for field effect transistors

The noise behavior is described by four noise sources. The resistors R_D and R_S are associated with thermal noise after

$$\overline{i_{RD}^2} = 4 \cdot k \cdot T \cdot \frac{1}{R_D} \cdot \Delta f \qquad (21)$$

and

$$\overline{i_{RS}^2} = 4 \cdot k \cdot T \cdot \frac{1}{R_S} \cdot \Delta f \qquad (22)$$

The amplifier effect of JFETs is based on changes in the channel resistor. This leads to describing the noise of the channel current I_D also by thermal noise

$$\overline{i_{nD,th}^2} = \frac{8}{3} \cdot k \cdot T \cdot g_m \cdot \Delta f \tag{23}$$

Additionally, an 1/f noise source is assumed with the channel after

$$\overline{i_{nD}^2} = \frac{8}{3} \cdot k \cdot T \cdot g_m \cdot \Delta f + KF \cdot \frac{I_D^{AF}}{f} \cdot \Delta f \tag{24}$$

with the model parameters AF and KF. The shot noise of the Gate current is usually neglected.

This model is valid for the simulators SPICE2, SPICE3, PSPICE and ADS. With HSPICE, an additional series resistor at the Gate is assumed with corresponding thermal noise. For the thermal noise of the channel, there is a choice to replace equ.(23) by a more accurate model [3].

With
$$\left(\overline{i_{nD,th}^2}\right)^{HSPICE} = \frac{8}{3} \cdot k \cdot T \cdot \beta \cdot \left(v_{gs} - V_{T0}\right) \cdot \frac{1 + \alpha + \alpha^2}{1 + \alpha} \cdot GDSNOI \cdot \Delta f \tag{25}$$

and
$$\alpha = \begin{cases} 1 - \dfrac{v_{ds}}{v_{gs} - V_{T0}} & \text{linear region} \\ 0 & \text{saturation region,} \end{cases} \tag{26}$$

it differentiates between linear and saturated region. And, with GDSNOI , an additional noise parameter is introduced.

MOSFETS

The noise formulation of MOSFET models in most of the commonly used simulation programs is based on the SPICE2 model of the UCB University of California, Berkeley, described in [3]. It is known, however, that the thermal channel noise included in this model is essentially valid only in the saturated region of the output characteristics [11]. Therefore, the latest UCB model, the BSIM3v3 model [10], models the noise differently, see further below.

Fig.7 depicts the noise equivalent schematic of the SPICE2 MOS2 and MOS3 model. Like with the JFET transistor, the resistors R_D and R_S are associated with thermal noise after

$$\overline{i_{Rd}^2} = 4 \cdot k \cdot T \cdot \frac{1}{R_d} \cdot \Delta f \tag{27}$$

and
$$\overline{i_{Rs}^2} = 4 \cdot k \cdot T \cdot \frac{1}{R_s} \cdot \Delta f \tag{28}$$

The channel noise is described by

$$\overline{i_{nD}^2} = \frac{8}{3} \cdot k \cdot T \cdot g_m \cdot \Delta f + KF \cdot \frac{I_D^{AF}}{f \cdot C_{ox} \cdot L_{eff}^2} \cdot \Delta f \tag{29}$$

using again the parameters AF and KF for the flicker noise. C_{ox} and L_{eff} are calculated inside the model from the other model parameters.

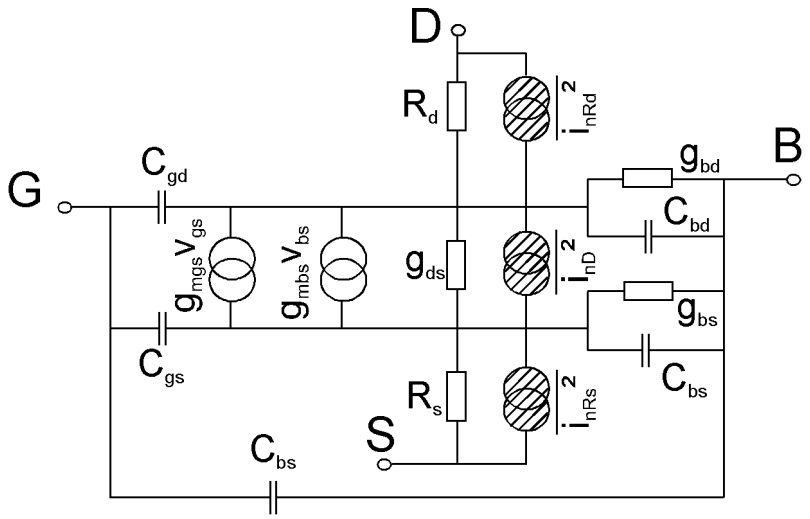


Fig.7: Noise equivalent schematic of the SPICE2 MOS level2 and level3 transistor model.

In PSPICE, an additional thermal noise of the Gate and of the Bulk resistor is included. With ADS, the models MOSFET Level 1-3 and EEMOS1 are also based on fig.7. With EEMOS1, however, no 1/f noise is included.. With HSPICE, like with the mentioned JFETs from above, the user has the choice between this and an alternate noise description. The thermal channel noise is described again after equ. (25), with the exception

$$\alpha = \begin{cases} 1 - \dfrac{v_{ds}}{V_{D,sat}} & \text{in the linear region} \\ 0 & \text{in the saturation region} \end{cases} \tag{30}$$

With the BSIM3v3 model of UCB SPICE3, the user can select for both, the flicker noise as well as for the thermal channel noise, one of the following models. This is done by setting the model parameter noimod accordingly. Either, a slightly modified SPICE2 model describes the 1/f noise by

$$\overline{i_{1/f}^2} = KF \cdot \frac{I_D^{AF}}{f^{EF} \cdot C_{ox} \cdot L_{eff}^2} \cdot \Delta f \tag{31}$$

Here, with the same functionality like in the VBIC bipolar model, an additional parameter EF has been introduced, modeling the frequency dependence of the noise spectrum. The thermal channel noise is calculated in BSIM3v3 after

$$\overline{i_{th}^2} = \frac{8}{3} \cdot k \cdot T \cdot (g_m + g_{ds} + g_{mb}) \cdot \Delta f \tag{32}$$

Or, depending on the parameter NOIMOD, the BSIM3v3 noise model calculates the 1/f noise after

$$\overline{i_{1/f}^2} = f(NOIA, NOIB, NOIC, EF, EM) \tag{33}$$

using a relatively complex formula, and involving the five new noise parameters NOIA, NOIB, NOIC, EF and EM as well as large signal model parameters [34].

For the channel noise, it is

$$\overline{i_{th}^2} = \frac{4 \cdot k \cdot T \cdot \mu_{eff}}{L_{eff}^2} \cdot \left|Q_{inv}\right| \cdot \Delta f \tag{34}$$

with

$$Q_{inv} = -W_{eff} \cdot L_{eff} \cdot C_{ox} \cdot V_{gsteff} \cdot \left(1 - \frac{A_{bulk}}{2 \cdot \left(V_{gsteff} + 2 \cdot v_t\right)} \cdot V_{dseff}\right) \tag{35}$$

The procedure described further below in this paper, covering the 1/f noise parameter extraction, can therefore be applied to the BSIM3v3 model only if the SPICE2 model for the 1/f noise has been selected specifically by the parameter NOIMOD. For extracting the parameters NOIA, NOIB, NOIC, EF and EM, see the BSIM3v3 toolkit for IC-CAP.

MESFETS

The noise behavior of MESFETs is modeled in the simulation programs PSPICE and HSPICE essentially analogous to the corresponding JFET -models [3]. See [12] for more details.

As a final remark, the noise bandwidth Δf is set to Δf=1Hz in most simulators.

4. 1/f Noise Measurement Setup

When measuring noise of high frequency transistors, we continue to distinguish between a low frequency range up to several MHz, followed then by a second range up to the maximum operating frequency of the device (GHz). In the first range, the noise power density spectrum is measured in order to characterize the 1/f noise and the generation/recombination noise. In the upper range, the noise figure F_{min}, and the parameters R_n , $\underline{Y}_{opt}$ are measured.

We will now discuss a possible measurement setup for the first range, the 1/f noise characteristics. It is depicted in figure 8. It consists of an HP4142 or HP415x SMU, which, however, is operated in 'power supply' mode. This means that it is triggered to output either a current or voltage (depending on the type of transistor), and to keep this current or voltage switched on, until the 1/f noise measurement is over and a new 'stop' command is sent to the SMU. The SMU is connected to the Gate or Base of the transistor by a 1Hz filter. Its output resistance is switchable. For MOS transistors, a low output impedance of the filter is required (e.g. 50Ω), while a high output impedance (e.g. 500kΩ) is used for bipolar transistors.

Note: for a bipolar transistor, the 1/f noise is generated in the Base region. If the 1Hz filter had a low output impedance, it would shorten this noise source and we would measure/simulate a too low 1/f noise characteristic. The higher the 1Hz filter's output impedance is, the less shortening occurs, see also [14]. In the toolkit, a value of ~330kΩ has been found to work best.

The output of the transistor is connected to a special low-noise current amplifier. Besides amplifying the 1/f noise, this amplifier also serves to bias the Drain or Collector of the transistor, and also to compensate the DC Drain or Collector current with an ultra-low noise DC current source. This allows to amplify only the noise current of the transistor:

$$\overline{V^2_{output\_amplifier}} = R^2 \cdot \overline{I^2_{noise\_transistor}}$$

With this setup, the cabling is minimized. Only 2 short coax cables are used to bias the transistor and to measure the noise. Therefore, extremely reliable and extremely clean noise measurements are obtained.
The output of the noise amplifier is further connected to an HP35670 dynamic signal analyzer, which then converts the 1/f noise time signals into a frequency spectrum.
The whole setup is controlled by special IC-CAP macros for bipolar transistors, and for MOS transistors. Ready-to-use extraction routines for the noise parameters AF, KF and EF (for MOS) are included as well.

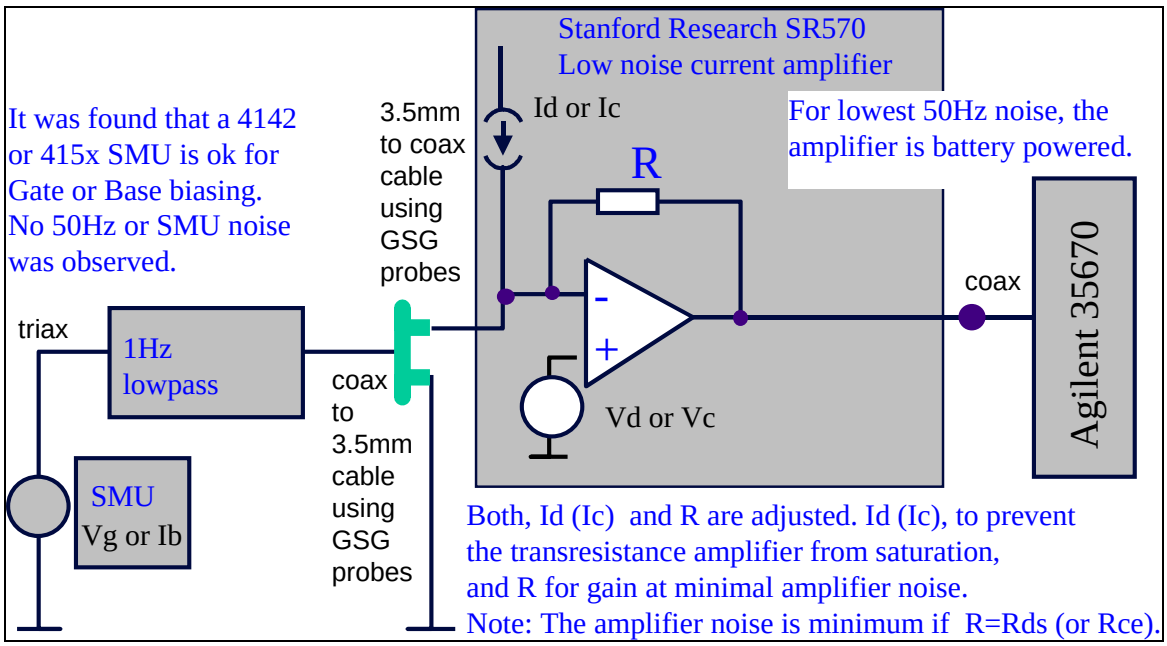


Fig.8a: Block diagram of the 1/f noise measurement setup of the IC-CAP toolkit

Note: For on-wafer measurements, special attention has to be paid regarding shielding. It is recommended to use a prober with a special 1/f shielding. However, most important, it is recommended to use the G-S-G RF probes instead of using DC probes !

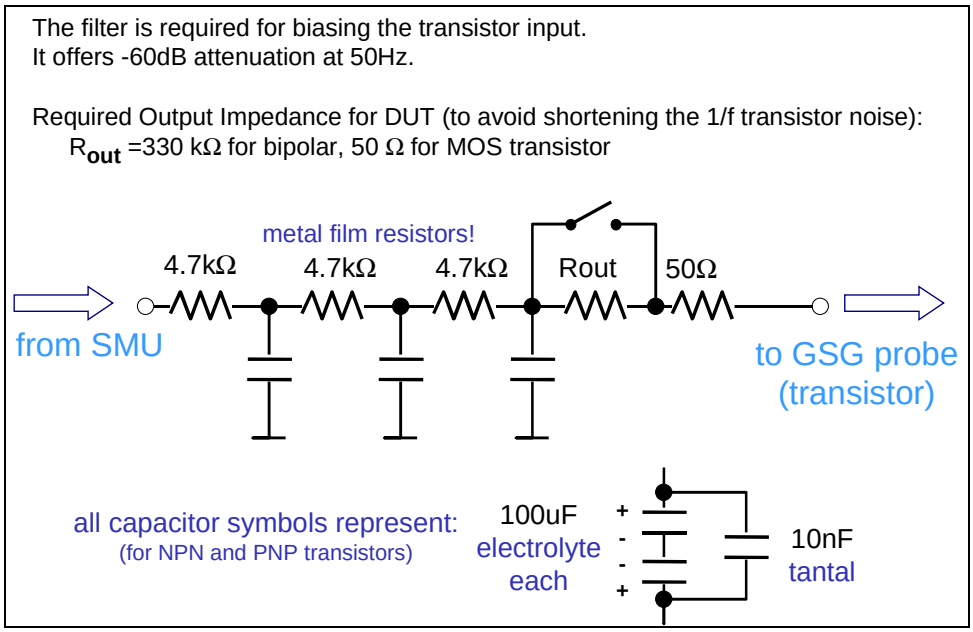


Fig.8b: 1Hz DC bias filter

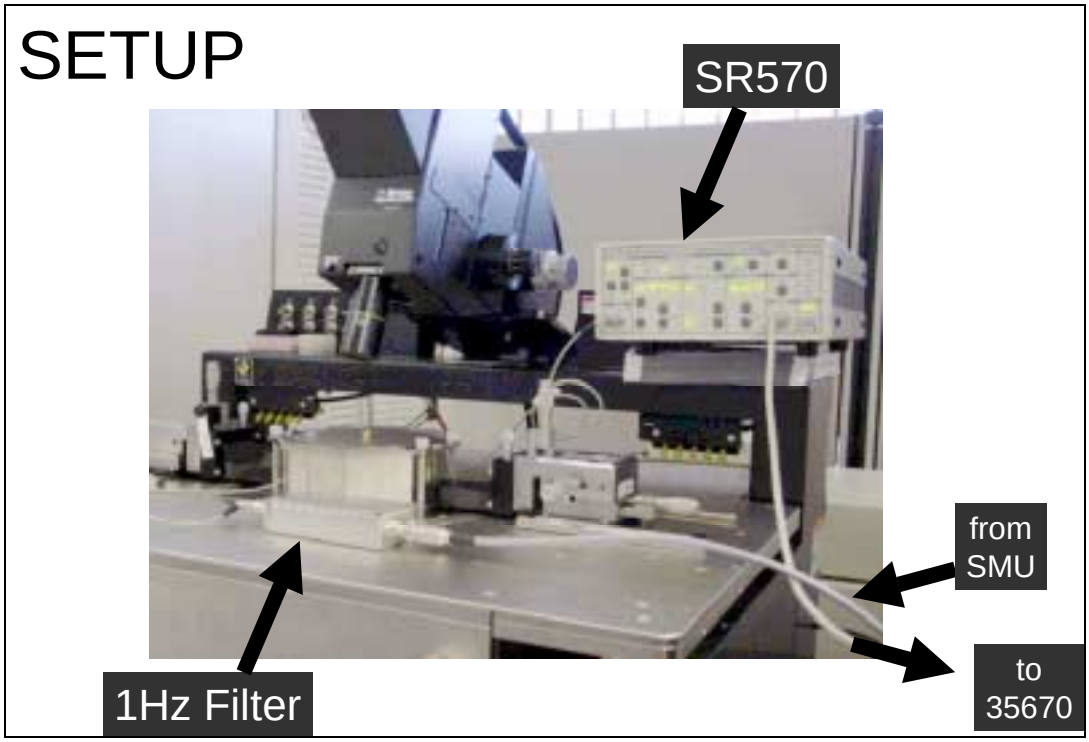


Fig.8c: The measurement setup

The 1/f noise modeling toolkit contains all required IC-CAP measurement setups and driver macros for measuring the bipolar and MOS transistor 1/f noise and to extract the model parameters. Fig.9 shows its structure, and fig.10 the macros for measurements and parameter extractions.

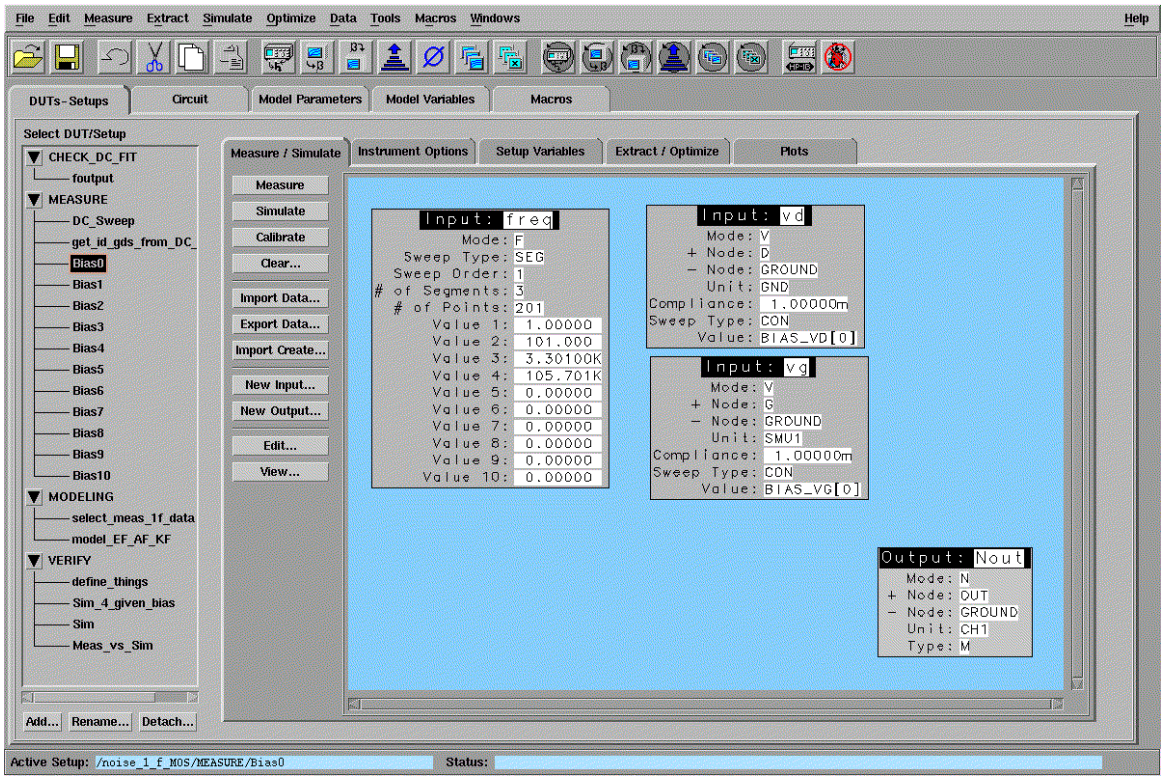


Fig. 9: structure of the 1/f noise modeling toolkit.

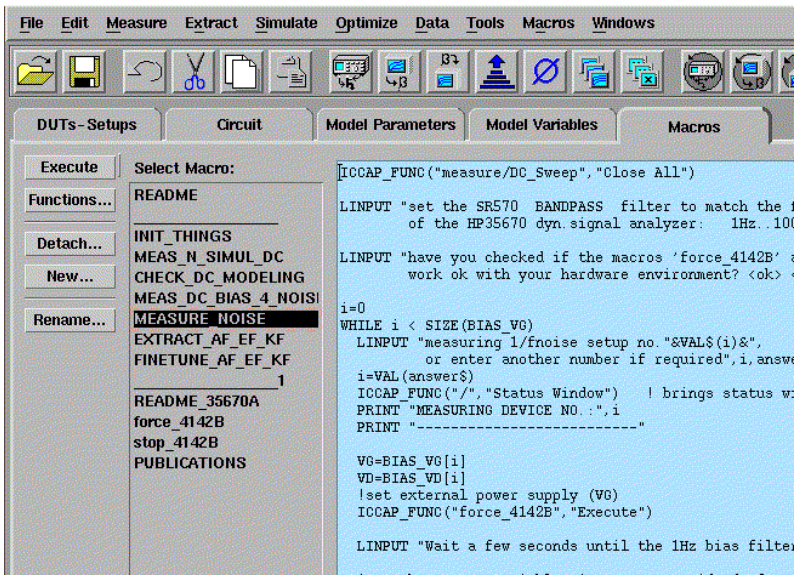


Fig.10: toolkit macros for controlling the measurements and the extractions

Measurement resolution of the setup of fig.8:

The current noise spectral density resolution obtainable with this system has been measured as ~5E-21 A^2/Hz.

5. AF, KF and BF/EF Noise Parameter Extraction and Verification

Considering the parameter extraction, we refer to the method introduced in [13, see also 14]. Following this approach, there is no need to exactly determine the corner frequency f_c like with other proposed methods. For the corner frequency f_c, the 1/f noise equals the white noise. For frequencies below that, the 1/f noise is dominant, allowing to neglect all other noise sources for the further analysis. The current noise source of the transistor can now be calculated out of the measured noise at the output of the transresistance amplifier.

Bipolar Transistors:

For the bipolar transistor models, the origin of the 1/f noise is the Base region, see equation (17). However, the effective 1/f current noise spectral density [A^2/Hz] is measured at the Collector of the transistor. Therefore, the 1/f noise at the Base has to be calculated first after

$$S_{iB} = \frac{1}{\beta^2_{(I_{B\_DC})}} \cdot S_{iC} \qquad \left[\frac{A^2}{Hz}\right] \tag{36}$$

To begin with the parameter extraction, we first repeat the formula of the 1/f effective noise current generated at the Base (equ.17)

$$\overline{i_{nB\,1/f}{}^2} = KF \cdot \frac{I_{B\_DC}^{AF}}{f} \cdot \Delta f \qquad \left[A^2\right] \tag{37}$$

Note: the VBIC model features an additional 1/f noise parameter, BF, see equ.(20). It acts like the EF parameter in the BSIM3v3 model: to fit the -10dB/decade slope of the measured 1/f noise. For details about its extraction, please refer to the next section on MOS transistors.

In order to match equ.(37) to equ.(36), we normalize to Δf and set Δf = 1Hz. This gives the Base current noise spectral density

$$S_{iB} = \frac{\overline{i_{nB\,1/f}{}^2}}{1Hz} = KF \cdot \frac{I_{B\_DC}^{AF}}{f} \qquad \left[\frac{A^2}{Hz}\right] \tag{38}$$

Since the 1/f slope is a 'given' for our actual modeling problem, our next step is to get rid of it by multiplying the measured curve with the frequency points 'f'. This results in a flat trace where we had the 1/f slope before.

$$S_{iB} \cdot f = KF \cdot I_{B\_DC}^{AF} \tag{39}$$

The advantage of this method is that we are now easily able to identify the value of the 1/f noise at 1Hz, what will be used in the next step. The 1Hz noise value is simply calculated as the mean value of a maximum flat sub-range of these so transformed data.

Considering the extrapolated measurement result at 1Hz, the above formula simplifies to

$$S_{iB@1Hz} = KF \cdot I_{B\_DC}^{AF} \tag{40}$$

This means, we are now ready to obtain an 1Hz value of our 1/f noise for each bias condition I_{B_DC}.

In the next step, we draw these values against the bias current. We apply a logarithmic conversion to the above formula and obtain

$$\log_{10}\left(S_{iB@1Hz}\right) = \log_{10}(KF) + AF \cdot \log_{10}\left(I_{B\_DC}\right) \tag{41}$$

what can be interpreted as a linear function like

$$y = a + b \cdot x \tag{42}$$

where

$$y = \log_{10}\left(S_{iB@1Hz}\right)$$
$$a = \log_{10}(KF)$$
$$b = AF$$

and the DC bias current at the Base is transformed by $x = \log_{10}\left(I_{B\_DC}\right)$

A linear regression is applied, which returns the y-intersect 'a' and the slope 'b' of a best fitting line for equ.(42).

The noise parameters AF and KF are then calculated after

$$AF = b \tag{43}$$

and

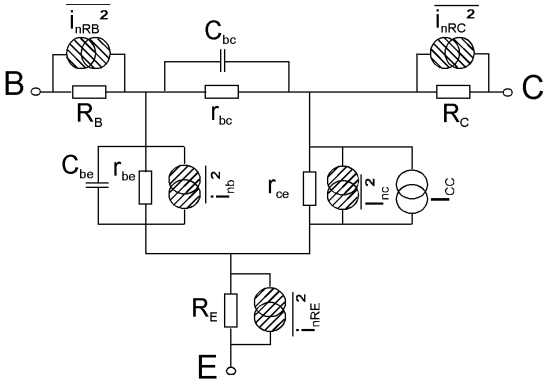
$$KF = 10^{a} \tag{44}$$

Step-by-step modeling procedure for bipolar transistors:

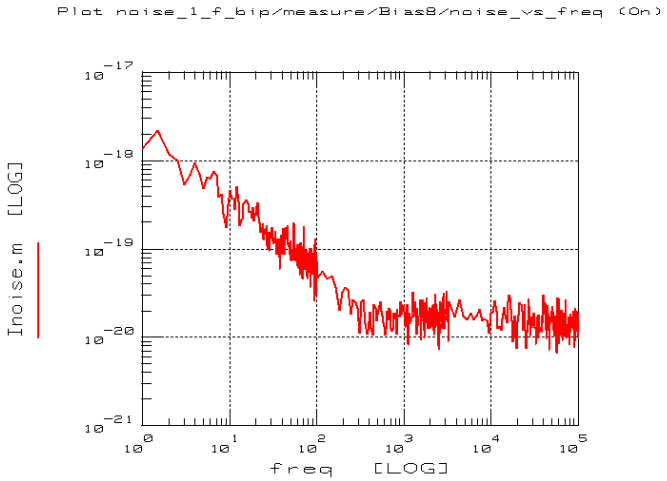
1.) for a first DC bias condition (e.g. iB_DC = 1uA, vCE = 2V), the 1/f noise spectral density is measured. As stated above, for the bipolar transistor, the 1Hz Base filter's output impedance is set to a high value, e.g. 330kΩ.

NOTE: This value must be considerably bigger than the input resistance $r_{BE} = \frac{\partial v_{BE\_DC}}{\partial i_{B\_DC}}$.

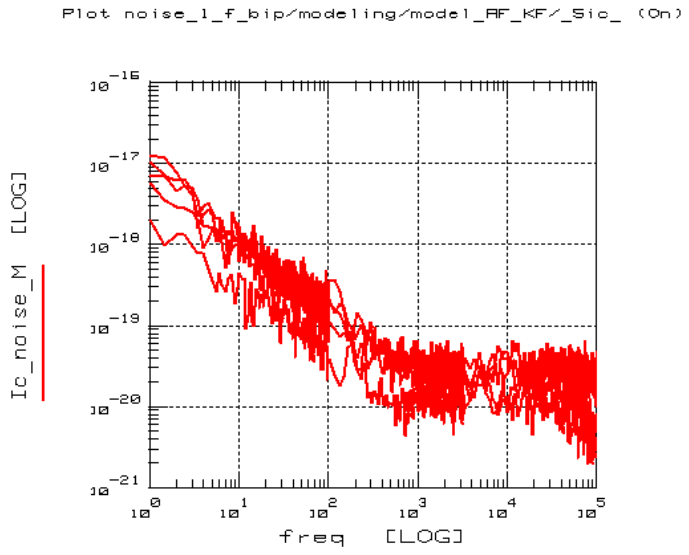
Otherwise, it would shorten the 1/f noise current source i_{nB}^2 at the Base!



The following plot shows the measured noise current at the Collector:

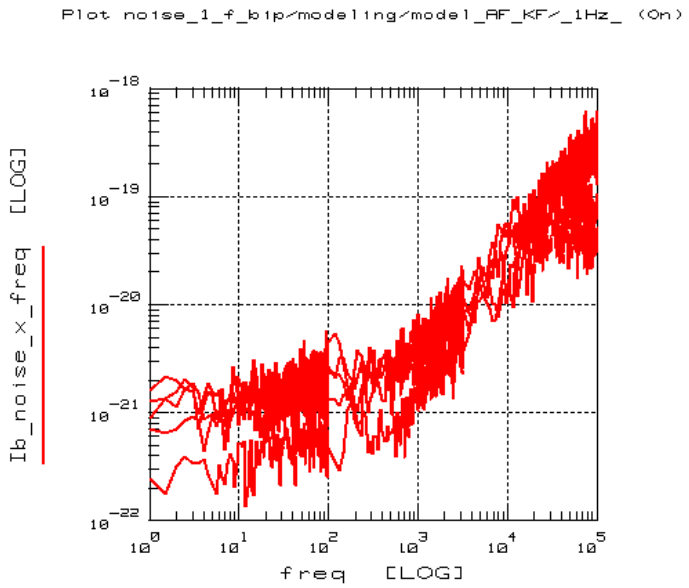


2.) this is repeated for e.g. 5 more different Base currents, but the same vCE.
And we get five 1/f noise curves for each iB_DC bias condition:



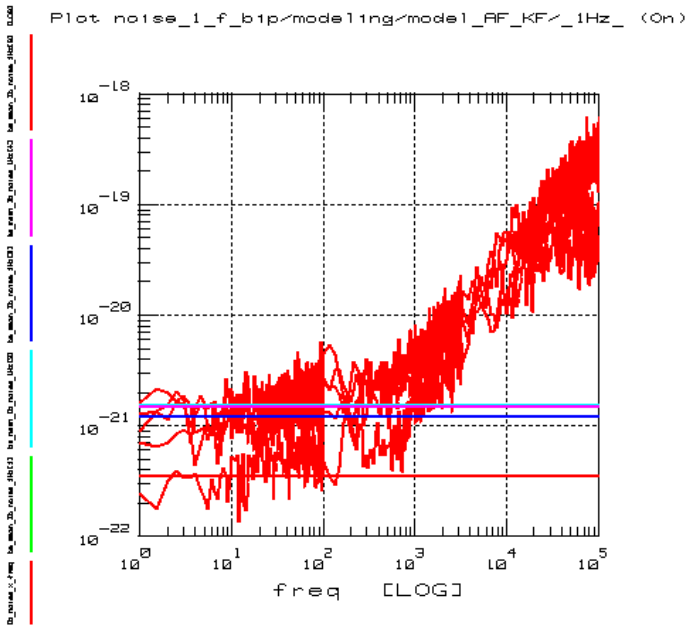
3.) We have so far considered the noise current data measured at the Collector of the transistor. The 1/f noise source of a bipolar transistor is, however, located and modeled in the Base region. Therefore, we have to divide the above obtained Collector current noise spectral density S_{iC} by beta^2, and obtain S_{iB}, see equ.(36) above.

4.) After we have obtained S_{iB} at the Base, we multiply it by 'freq' , see (39), and obtain:

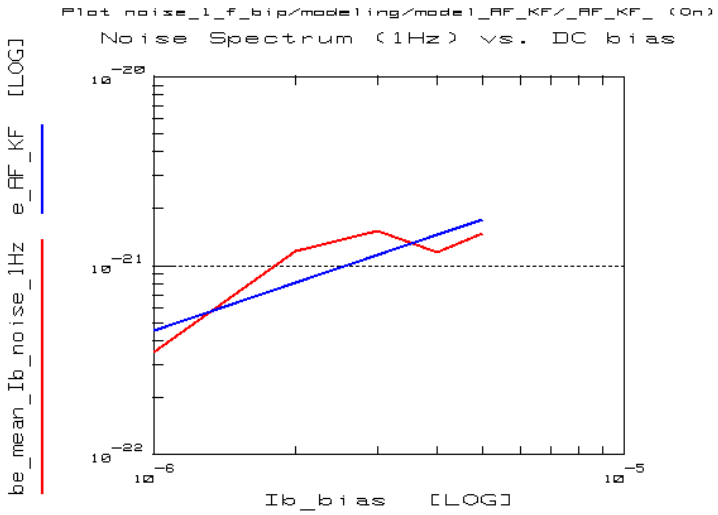


Thus, the 1/f noise appears as flat traces and can easily be identified.

5.) we calculate the mean value of each transformed 1/f curve for each Base bias condition from the max. flat traces. These mean values represent the 1Hz values of the 1/f current noise spectral density, as a function of the iB_DC bias.

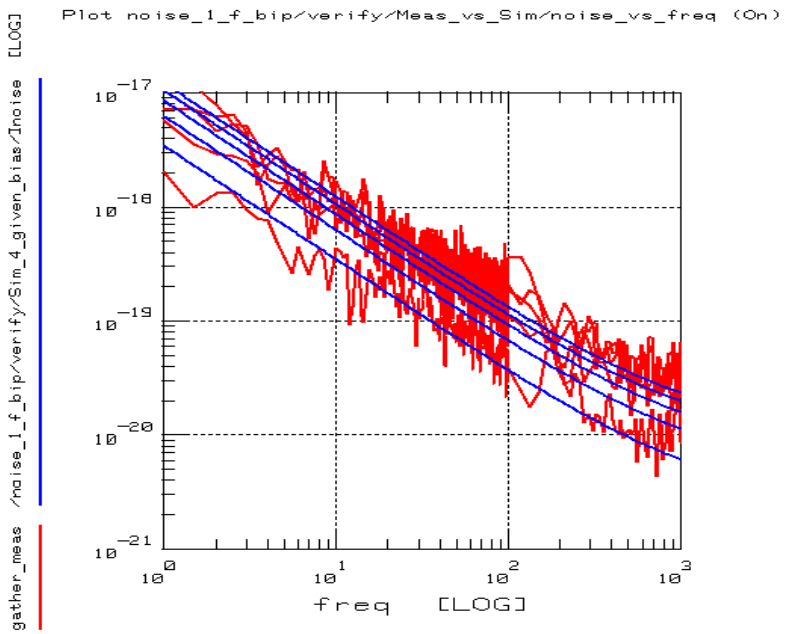


6.) Finally, we are ready to draw the 1Hz Base noise data points against the DC bias i_{B_DC}, and fit a line to these data points, see equations (41) and (42).



From the y-intersection and the slope of the fitted curve, we calculate AF and KF after equations (43) and (44).

7.) After the model parameters have been obtained, the simulation result of the Collector current noise spectral density is compared with the original measured data, and the AF and KF model parameters are fine-tuned.



Measured and simulated Collector noise spectral density [A^2/Hz] for the bipolar transistor.

MOS Transistors:

The 1/f noise description for MOS transistors in this chapter refers to the AF, KF, EF formulation. For details about how to model the 1/f noise in BSIM3v3 using the parameters NOIA, NOIB etc., see publication [15].

What makes the modeling easier compared to the bipolar case, is that the dominant 1/f noise source is located at the output of the transistor, i.e. the Drain-Source channel. On the other hand, the transistor Gate impedance is high. Related to the measurement setup and our 1Hz filter at the Gate, this corresponds to a low output impedance. We choose 50Ω.

On the other hand, a 3rd model parameter is used to reflect slight differences from the theoretical 1/f slope: the parameter EF.

Also, different to the bipolar case, the 1/f noise formulation of the BSIM3v3 model includes some geometry parameters.

As with the bipolar case, we first refer to the formula for the 1/f Drain-Source effective noise current as

$$\overline{i_{nD\,1/f}^{\,2}} = KF \cdot \frac{I_{D\_DC}^{AF}}{f^{EF} \cdot COX * Leff^{2}} \cdot \Delta f \qquad (45)$$

with

$$COX = \frac{\varepsilon_0\, \varepsilon_{Si}}{TOX} = \frac{3.45E-11}{TOX}$$

$$Leff = L - 2*\left(LINT + \frac{LL}{L^{LLN}} + \frac{LW}{W^{LWN}} + \frac{LWL}{L^{LLN} * W^{LWN}} \right)$$

or simplified: $Leff = L - 2*LINT$

Again, we normalize to Δf, then set Δf = 1Hz and obtain the Drain-Source current noise spectral density in A^2/Hz.

$$S_{iD} = \frac{\overline{i_{nD\,1/f}^{\,2}}}{1Hz} = KF \cdot \frac{I_{D\_DC}^{AF}}{f^{EF} \cdot COX * Leff^{2}} \qquad (46)$$

As the first modeling step, we extract the parameter EF, the 1/f slope correction. A log conversion of equation (45) gives:

$$\log_{10}(S_{iD}) = const. - EF \cdot \log_{10}(f) \qquad (47)$$

I.e. we convert both the measured noise data and the frequency points logarithmically and apply a regression curve fitting. The parameter EF is then the '-slope' of the fitted line.

Since the $1/f^{EF}$ slope is now already modeled, we can get rid of it by multiplying the measured curve with the frequency points 'f^{EF}'. This results in a flat trace where we had the $1/f^{EF}$ slope in the measurements before.

$$S_{iD} \cdot f^{EF} = KF \cdot \frac{I_{D\_DC}^{AF}}{COX * Leff^2} \tag{48}$$

After this step, we are again easily able to identify the value of the $1/f^{EF}$ noise at 1Hz: it is simply calculated as the mean value of a maximum flat sub-range of these so transformed data.

Considering the extrapolated measurement result at 1Hz, the above formula simplifies to

$$S_{iD@1Hz} = KF \cdot \frac{I_{D\_DC}^{AF}}{COX * Leff^2} \tag{49}$$

This means, we are now ready to obtain an 1Hz value of our $1/f^{EF}$ noise for each bias condition i_{D_DC}.

In the next step, we draw these values against the i_{D_DC} bias current. We apply a logarithmic conversion to the above formula and obtain

$$\log_{10}\left(S_{iD@1Hz}\right) = \log_{10}\left(\frac{KF}{COX \cdot Leff^2}\right) + AF \cdot \log_{10}\left(I_{D\_DC}\right) \tag{50}$$

what can be interpreted as a linear function like

$$y = a + b \cdot x \tag{51}$$

where

$$y = \log_{10}\left(S_{iD@1Hz}\right)$$

$$a = \log_{10}\left(\frac{KF}{COX \cdot Leff^2}\right)$$

$$b = AF$$

and the DC bias current at the Base is transformed by $x = \log_{10}\left(I_{D\_DC}\right)$

A linear regression is applied, which returns the y-intersect 'a' and the slope 'b' of a best fitting line.

The noise parameters AF and KF are then calculated after

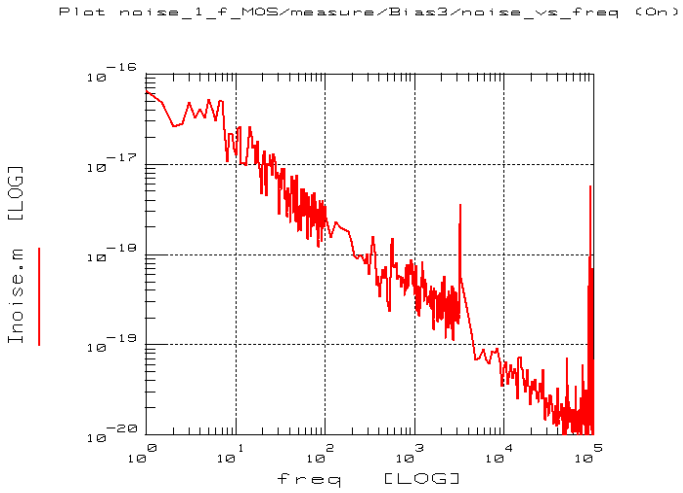
$$AF = b \tag{52}$$

and

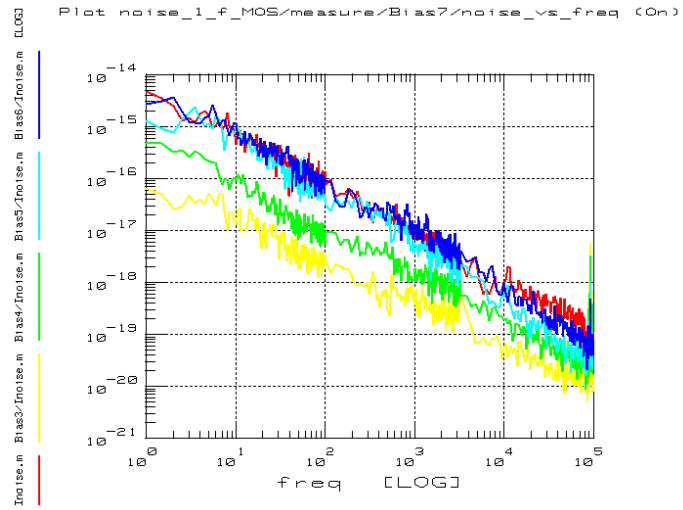
$$KF = COX \cdot Leff^2 \cdot 10^a \tag{53}$$

Step-by-step modeling procedure for BSIM3v3 CMOS transistors:

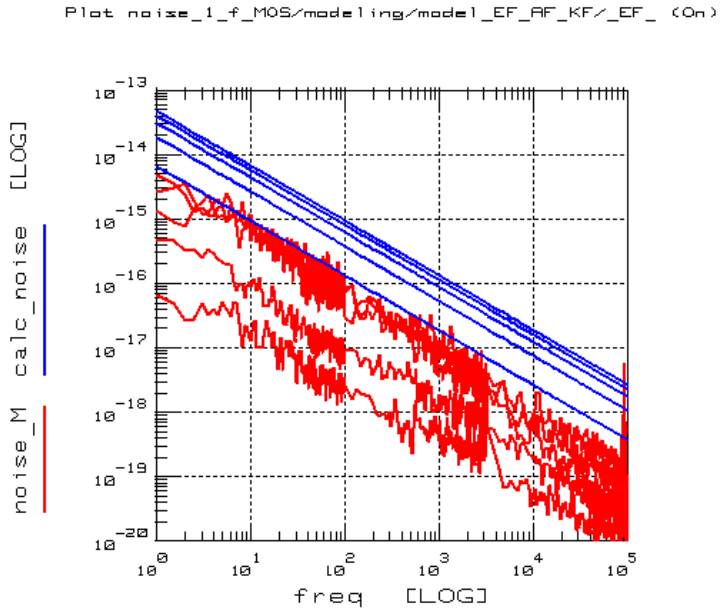
1.) for a first DC bias condition (e.g. vG = 0.6V, vDS = 1V), the 1/f Drain current noise spectral density [A^2/Hz] is measured. The 1Hz Base filter's output impedance is set to 50Ω. The following plot shows the measurement result:



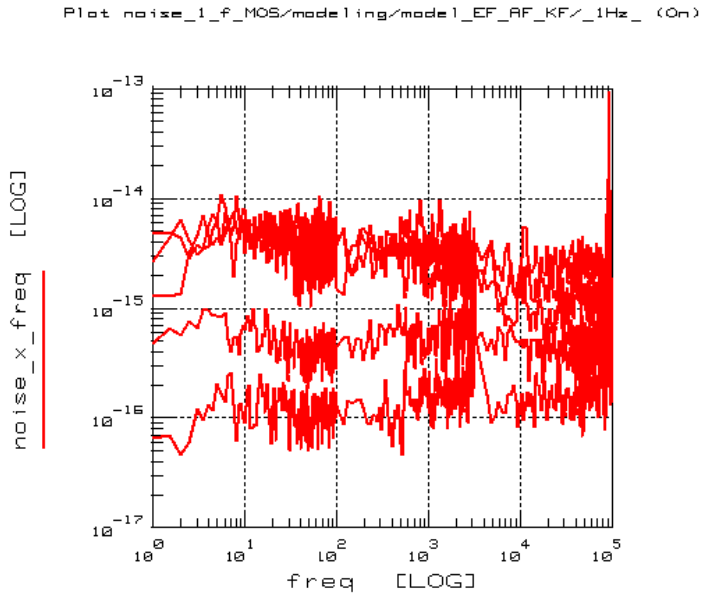
2.) this is repeated for e.g. 5 more different Gate voltages, but the same vDS.
And we get five 1/f noise curves for each vG DC bias condition:



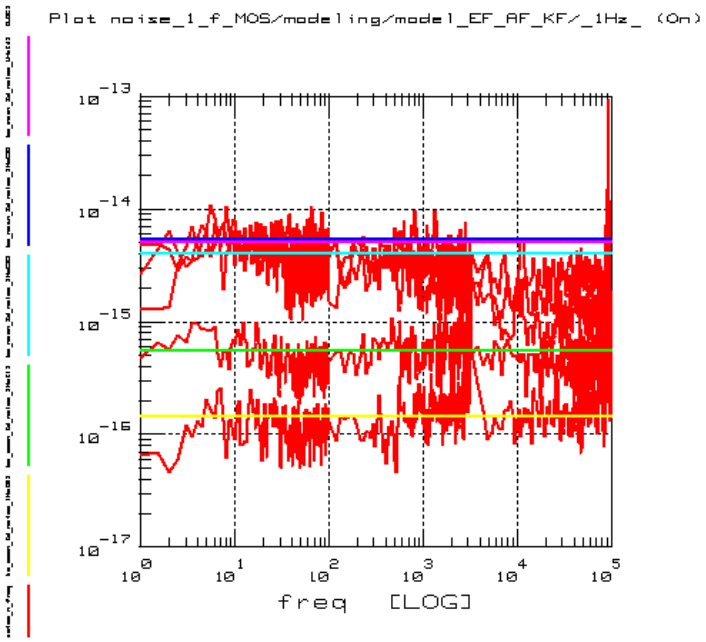
3.) In the next step, we extract the EF parameter after (47), and check if the slopes of the intermediate simulations match.
(Note: the AF and KF have not yet been extracted, therefore only the slopes are important to compare!)



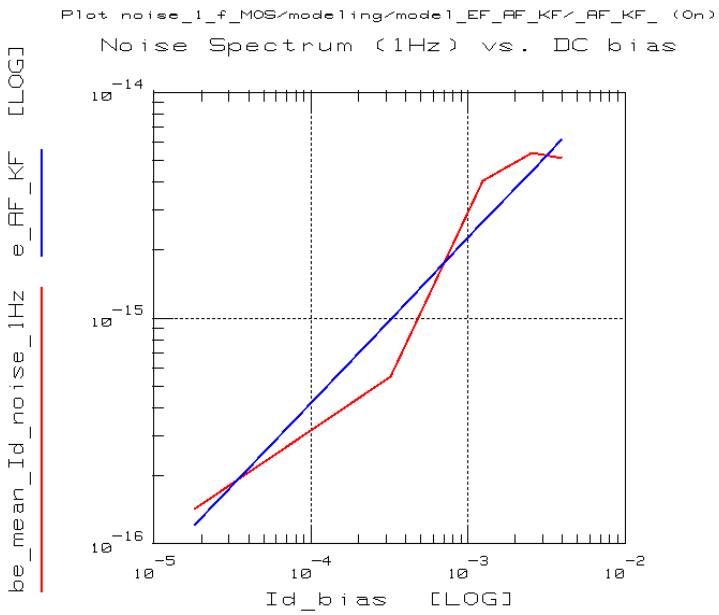
4.) Now, we are ready to multiply by f^{EF} in order to easier extract the 1Hz value of the noise.



5.) we calculate the mean value of each transformed 1/f curve for each vG bias condition from the max. flat regions. These mean values represent the 1Hz values of the 1/f Drain current noise spectral density, as a function of the iD_DC bias.

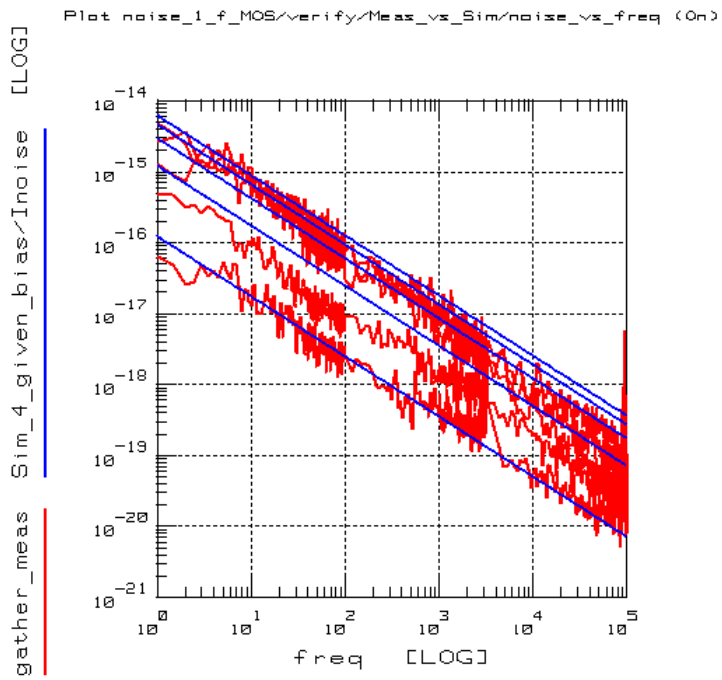


6.) Finally, we are ready to draw the 1Hz Drain current noise data points against the DC bias current i_{D_DC}, and to fit a line to these data points, see equations (50) and (51).



From the y-intersection and the slope of the fitted curve, we calculate AF and KF after equations (52) and (53)

7.) After the model parameters have been obtained, the simulation result is compared with the original measured data, and the AF, KF and EF model parameters are fine-tuned.

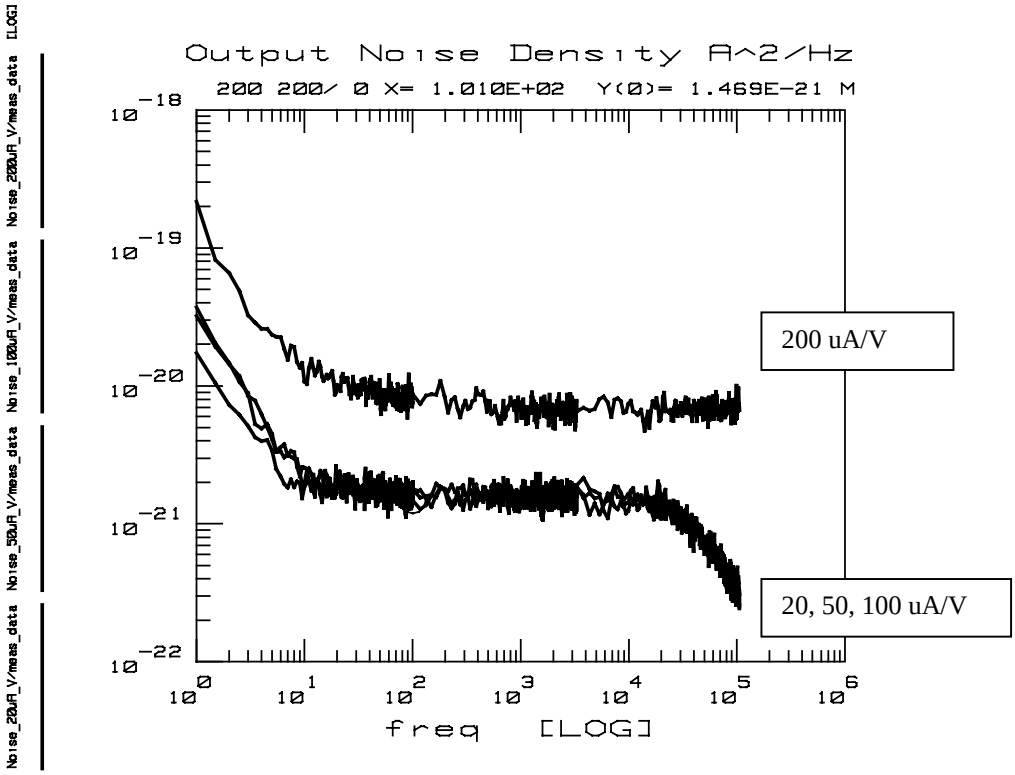


Measured and simulated Drain current noise spectral density [A^2/Hz] for the MOS transistor

NOTE:

The noise data returned from hspice and spice3 differs from the noise data returned from hpeesofsim, mns, and spectre.
hspice and spice3 have units of V^2/Hz and the other simulators have V/Sqrt(Hz).

Appendix:
Noise floor information on the toolkit measurement setup



The figure above shows the current noise density of the system measured at the device output (at the low noise current amplifier LNA).
The noise is expressed in A^2/Hz and varies with the LNA sensitivity. The figure shows the noise floor for the 4 most commonly used values of the LNA sensitivity: 20 uA/V, 50 uA/V, 100 uA/V and 200 uA/V.

Comments:

- The 1/f noise observed at the beginning of the trace is due to the internal 1/f noise of the LNA.
- The noise drop observed at low sensitivity values (high gain) is due to the bandwidth limitation of the LNA. Note that this is not in the frequency band used for the extraction (typically between 10 Hz and 1 kHz). Using a sensitivity of 200 uA/V or greater does not have this limitation but on the other hand, increases the noise floor.
- This noise floor should be compared to the output current noise density of the DUT . If the DUT is a CMOS, this would be the drain current noise density. If the DUT is a bipolar, this should be the collector current noise density. Note that in the bipolar case, the current noise source is actually modeled at the input (base current). The Ib noise density is determined by dividing the Ic noise density by the DUT current gain (squared).

7. Acknowledgements and Publications

I would like to thank specially F. X. Sinnesbichler of the Technical University Munich, Institute of High Frequency Techniques, for having laid the base for this manual. A big part of the chapters stem from this work. I would also especially acknowledge Mr.Sinnesbichler's IC-CAP workshop about Noise modeling in Munich, July 1998.

In the same way, I have to acknowledge Mr.Knoblinger of Infineon Technologies AG in Munich, for his hint on using the special low-noise current amplifier as an excellent and straight-forward way to measure 1/f noise accurately and without big influences from power line frequency harmonics.

For important discussions on the noise terminology, I'd like to mention Mr. Berkner, also Infineon Technologies AG in Munich.

For detailed verification tests and measurements of the proposed measurement setup I am grateful to A.Blaum, O.Pilloud, G.Scalea, J.Victory, Motorola, Geneva

Web Info

Stanford Research Web Page: http://www.srsys.com/

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Kobe, Japan, March 19-22,2001

The use of the SR560 low-noise voltage amplifier (lower system noise, but no internal DC bias available) is published in:
Hardy et al., Low-Frequency Noise in Proton Damaged LDD MOSFET's,
IEEE Trans. on el. devices, vol.46, no.7, July 1999, P.1341

APPENDIX: Parts list for 1/f noise toolkit:

```
Instruments:
1     Wafer Probe Station with GSG probes
         (alternatively shielded DC probes)
1     Agilent DC Analyzer 414x or 415x (input biasing for transistor)
1     custom made Lowpass Filter (1Hz), input triax,
          output coax or 3.5mm connector
          following the recommended circuit description
1     Stanford Research Amp SR570
1     35670A Dynamic Signal Analyzer
1     Multimeter for controlling the DC bias provided by the SR570

Cables:
1     Cable: filter output (coax or 3.5mm) to GSG probe (3.5mm)
1     Cable: GSG probe (3.5mm) to SR570 (coax)
1     Cable: SR570 (coax) to 35670A (coax)

IC-CAP:
      85199A (framework), 85199B(analysis module: simulator interface)
      85199D (DC analyzer driver)
      85199G (35670 driver),
      85195B (1/f noise toolkit for AF, KF, EF parameter extraction
              for NPN-BJTs and MOS)
```