On-chip RF Isolation Techniques

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1 Atheros Communications, Inc.

BCTM 12.1 October 1, 2002
Key Take-away Point

IT DEPENDS!

• What is the maximum isolation I can achieve?

• How do I win the isolation argument with my co-workers?

• Will I get anything useful out of this talk?
Outline

• Technology impacts
  – Technology overview
  – Buried layers
  – Triple wells
• Grounding effects
• Guard rings
• Shielding
  – Patterned ground shield
• On-chip decoupling capacitance
• Summary
Lightly-Doped Wafer Resistivity

Non-conductive Backside
Lightly-Doped Wafer Resistivity

\[ d = 2.5 \times T_{\text{Wafer}} \]

Non-conductive Backside
Lightly-Doped Wafer Resistivity

\[ d \ll T_{\text{Wafer}} \]

\[ R_{\text{Substrate}} \]

\[ d_2 = 2 \times d_1 \quad : \quad R_2 < 2 \times R_1 \]

Non-conductive Backside
Lightly-Doped Substrate Isolation

- Lightly doped material
- Maximum isolation when source and victim are closer to the guard band
- Bonding inductance will affect isolation

\[
\text{Isolation} = 20 \log_{10} \left( \frac{V_{\text{victim}}}{V_{\text{noise}}} \right) [\text{dBV}]
\]

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Lightly-Doped Wafer Resistivity

\[ d \ll T_{Wafer} \]

\[ d_2 = 2 \times d_1 : R_2 < 2 \times R_1 \]

Floating Conductive Backside
Lightly-Doped Wafer Resistivity

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Lightly-Doped Wafer Resistivity

Floating Conductive Backside
BiCMOS Technology Basics

- Substrate: p⁻ (~12 ohm-cm)
- Field Implant: (~0.2 ohm-cm)
- Well: (~1 ohm-cm)
- Buried Layer: (~0.005 ohm-cm)
- Contact: (~0.005 ohm-cm)
- Sinker: (~0.005 ohm-cm)
- Deep Trench

F. Clement in J. Huijsing et al, KAP, ‘99
Buried Layer with Lightly-Doped Wafers

- $T_{\text{epi}}$ (~3 um)
- $T_{\text{buried}}$ (~1 um)
- $T_{\text{bulk}}$ (~400 um)

- p epitaxial layer
  (~1 ohm-cm)
- p$^+$ buried layer
  (~0.005 ohm-cm)
- p$^-$ wafer
  (~12 ohm-cm)

\[ R_{\text{bulkepi}} \sim 5 \times R_{\text{buried}} \]
Breaking the Buried Layer

- $T_{\text{epi}}$ (~3 um)
- $T_{\text{buried}}$ (~1 um)
- $T_{\text{bulk}}$ (~400 um)
- Deep trench
- n well (~1 ohm-cm)
- p epitaxial layer (~1 ohm-cm)
- p$^+$ buried layer (~0.005 ohm-cm)
- p$^-$ wafer (~12 ohm-cm)
- n$^+$ buried layer (0.005 ohm-cm)
Sony: 622 Mb/s Optical Receiver IC

Isolation for High Sensitivity

A trans-impedance amplifier is isolated from the other circuit blocks

(1) substrate contact region
(2) the $N^-$-layer (removed $P^+$) region

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Sony Noise Simulation

- Substrate noise distribution
  - SubstrateStorm
- Noise source injection points
  - Logic ground
- Noise source amplitude of 100%

![Diagram showing noise amplitude at substrate with different color codes for noise reduction from 1% to 0.05%]

No guard ring: 1% noise, 20x noise reduction
Double-guard: 0.05% noise

Substrate contact: N^- layer breaking buried layer

Trans-impedance amplifier

W: 50 µm
W: 10 µm

Noise amplitude at substrate:
- 1.65 to 100%
- 1.45 to 1.65%
- 1.25 to 1.45%
- 1.05 to 1.25%
- 0.85 to 1.05%
- 0.65 to 0.85%
- 0.45 to 0.65%
- 0.25 to 0.45%
- 0.05 to 0.25%
- 0.00 to 0.05%
NMOS: Triple Well Isolation

- $T_{\text{epi}}$ (~3 µm)
- $T_{\text{buried}}$ (~1 µm)
- $T_{\text{bulk}}$ (~300 µm)

Layers:
- **n sinker** (~0.005 ohm-cm)
- **p epitaxial layer** (~1 ohm-cm)
- **p+ buried layer** (~0.005 ohm-cm)
- **p- wafer** (~12 ohm-cm)

- **n+ buried layer** (~0.005 ohm-cm)
Motorola: GSM/GPRS Baseband IC

Process technology HiP7LP: *compatible with TSMC*

- Gate length $L_{poly}$: 0.13 $\mu$m
- Single gate Ox: 30 A
- Dual gate Ox: 50 A
- Supply voltage: 1.6 to 3.0 V
- Metal: 5 layer Cu
- Substrate: P+
- Nwell resistors: 700 ohm/sq
- Salicided Poly res.: 7.0 ohm/sq
- Metal Cap: 0.8 fF/$\mu$m²

Benefits of IPW isolation

Isolation Strategy

D. Redmond, ISSCC 2002
Noise from inverter core

Triple well

Sensor

Vss

Vcc or Vdd

180 μm

1000 μm

• Separate ground used for the digital core
• All simulations use SubstrateStorm with a 0.35 μm BiCMOS technology
• Remove triple well and compare with identical p+ guard ring
Package Effects on Triple-well Isolation

Guard Ring and Triple Well Isolation vs. Frequency

Frequency (Hz)

Attenuation (dB)

-120
-110
-100
-90
-80
-70
-60
-50
-40


TW_Vcc_0.5nH
Ring_0.5nH
TW_Vdd_0.5nH
Ring_0nH
TW_Vdd_0nH

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Grounding Effects

- Use multiple supplies to isolate areas
- Minimize inductance
STMicroelectronics: LNA + Mixer Integration

• Initial design had one substrate ground
• Simulations showed too much noise coupling
• Separated supply regions to isolate LNA from mixer

One substrate ground

Two substrate grounds
Coupling Paths

Equivalent behavior with pad or seal ring !!!
Guard Rings in a Lightly-Doped Process

- Guard rings are more effective in a lightly doped process
- A well region can break the channel stop and increase the isolation
Guard Ring Inductance Simulation Structure

Noise from inverter core

10 µm guard ring

45 µm wide sensor

1000 µm
Guard Ring Inductance Simulations

Inductance Effects on Guard Ring Isolation ($W = 10 \, \mu m$)

![Graph showing inductance effects on guard ring isolation](image)

- **No Guard Ring**
- $L = 0.5 \, \text{nH}$
- $L = 0.3 \, \text{nH}$
- $L = 0.1 \, \text{nH}$
Ericsson & STMicroelectronics: Single-chip BLUETOOTH ASIC

- 0.18 µm CMOS
- 2.5 – 3.0 V
- 75 mW in RX
- 90 mW in TX
- 2 MHz IF
- 5 GHz VCO
- 5.5 mm²
- Special attention to crosstalk

P. van Zeijl, ISSCC 2002

Tallis Blalack, BCTM 2002, Paper 12.1
Guard Ring Width Simulation Structure

Noise from inverter core

Guard ring

Sensor

0.3 nH

Vss

1000 μm

10 μm wide spacing
Guard Ring Width Simulations

Guard Ring Width Effects on Isolation (L = 0.3 nH)

- Attenuation (dB) vs. Frequency (Hz)
- Blue line: No Guard Ring
- Red line: W = 2 um
- Green line: W = 100 um
- Black line: W = 300 um
Guard Ring Isolation Summary

The maximum achievable guard ring isolation is?

Dependent on:

– Technology
– Spacing
– Width
– Grounding scheme
– Package parasitics
– …
Shielding of Signal Lines

Tie to reference bias $V_{\text{ref}}$

$R \ll \frac{1}{\omega C}$ (5 to 10 X)

Use p diffusion or poly instead of nwell above several hundred MHz

$V_{\text{ref}}$
Patterned Ground Shield Design

- Pattern
  - Orthogonal to spiral
    (induced loop current)
- Resistance
  - Low for termination of the electric field
  - Avoid attenuation of the magnetic field
Q Improvement – Tank Impedance Doubled

![Graph showing Q tank and frequency response with symbols for Poly PGS and No Shield]
Noise Coupling Measurement
Effect of Polysilicon Ground Shield on Noise Coupling
Conclusions on Patterned Ground Shield

- Improves Q by eliminating substrate loss
  - up to 33% at 1-2 GHz
- Improves isolation by preventing substrate coupling
  - up to 25 dB at 1 GHz
- Simplifies modeling
- Eliminates substrate dependency
- Requires no additional process steps
Atheros: 802.11a Radio Transceiver

- 0.25 μm standard digital CMOS for 5 GHz WLAN
- Transmitter 22 dBm output power
- Receiver 8 dB noise figure
- –112dBC/Hz (Δf = 1 MHz)
- 40+ on-chip spirals with PGS
- Shielded RF signals and inductors
- Proper use of guard rings and substrate taps
- Separate supply domains

D. Su, ISSCC 2002  Tallis Blalack, BCTM 2002, Paper 12.1
Decoupling Capacitance
Motorola: CMOS Broadband Tuner
Substrate Noise Suppressing Regulation

- External Supply
- Bond Wire
- ESD Protection
- Parasitic Capacitance
- Regulator Pass Device
- 40mV
- Synthesizer / Large Digital Switching Circuit
- Minimize Inductive Connection to IC Substrate
- Substrate Noise Reduction Capacitor
- Output Charge Supply Capacitor
- Input
- < 100μV
- < 100μV

Tallis Blalack, BCTM 2002, Paper 12.1
Simulated Substrate Noise, No Regulation

- Low resistivity epi substrate modeled as single node
- Decoupling capacitance used to supply local charge
- Peak current across bond wires much lower
- Ringing on substrate reduced
- ~9x noise reduction
  - 81.7 mV to 9.37 mV
Simulated Substrate Noise with Regulation

- On-chip voltage regulator added
- Decoupling capacitance at input and output of regulator
- ~100x reduction of noise
  - 9.37 mV to 0.098 mV
- Minimized inductive connection to substrate
Motorola: CMOS Broadband Tuner

- Synthesizer generates 100 mA switching currents @ 12.5 MHz
- 50 – 860 MHz LNA
- 0.35 μm CMOS
  - heavily doped bulk
- 5 V supply
- 1.5 Watts
- 5 mm²
- 48 pin eTQFP

~25% of area to reduce substrate noise ~1000x

> 81.7 mV to 98 μV
On-chip RF Isolation Summary

IT DEPENDS on

- Technology
- Frequency
- Grounding scheme
- Guard rings
- Package
- Decoupling capacitance
- ...
Acknowledgements

The authors would like to thank:

• Takeshita san and Kato san of Sony
• Dave Redmond of Motorola
• Andreia Cathelin and Didier Belot of STMicroelectronics
• Paul van Zeijl of Ericsson
• David Su of Atheros
• Larry Connell of Motorola