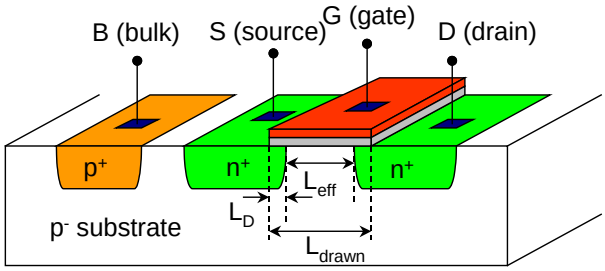
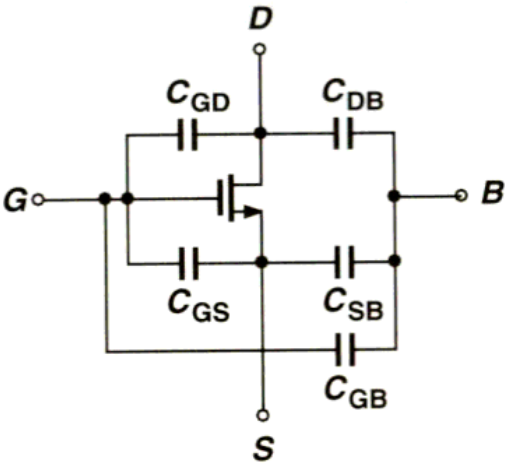
EE382M-14 CMOS Analog Integrated Circuit Design

Lecture 3, MOS Capacitances Small Signal Models, and Passive Components

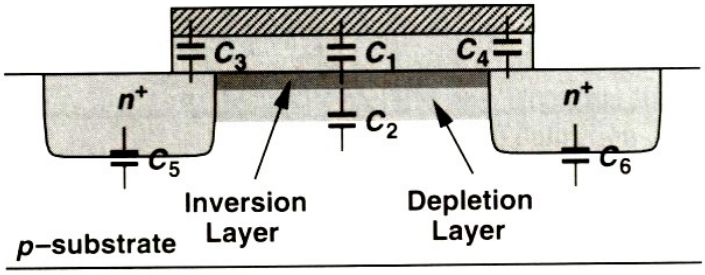
MOS Capacitances



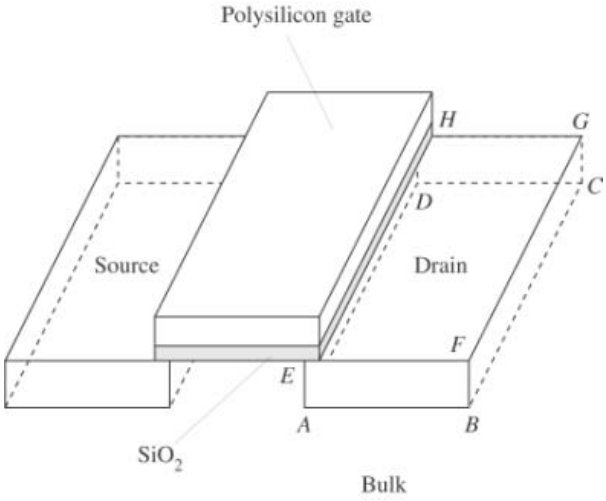


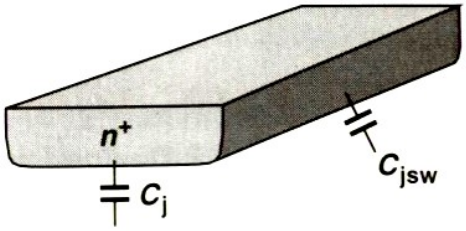
MOS transistor capacitance types:

- Depletion capacitance (pn junction capacitance)
- Gate-channel or gate-substrate capacitance
- Gate-source and gate-drain overlap capacitance



Junction Capacitance





$$C_{BX} = \frac{CJ \cdot AX}{\left(1 - \frac{V_{BX}}{PB}\right)^{MJ}} + \frac{CJSW \cdot PX}{\left(1 - \frac{V_{BX}}{PB}\right)^{MJSW}}$$

In the above equation, 'X' can be 'S' (source) or 'D' (drain). Or, we can rewrite,

$$C_{BS} = \frac{CJ \cdot AS}{\left(1 - \frac{V_{BS}}{PB}\right)^{MJ}} + \frac{CJSW \cdot PS}{\left(1 - \frac{V_{BS}}{PB}\right)^{MJSW}}$$

or

$$C_{BD} = \frac{CJ \cdot AD}{\left(1 - \frac{V_{BD}}{PB}\right)^{MJ}} + \frac{CJSW \cdot PD}{\left(1 - \frac{V_{BD}}{PB}\right)^{MJSW}}$$

CJ: source/drain bottom-plate junction capacitance per unit *area* at zero bias (unit: F/m^2). For example CJ can have a value of 0.6e-3 F/m^2.

CJSW: source/drain side-wall junction capacitance per unit *length* at zero bias (unit: F/m). An example value of CJSW can be 0.35e-11 F/m.

AX: 'X' can be 'S' or 'D'. AS, bottom-plate area of the source; AD, bottom-plate area of the drain (unit: m^2).

PX: 'X' can be 'S' or 'D'. PS, perimeter of the source, or PD, perimeter of the drain (unit: m).

PB: source/drain junction built-in potential (unit: V).

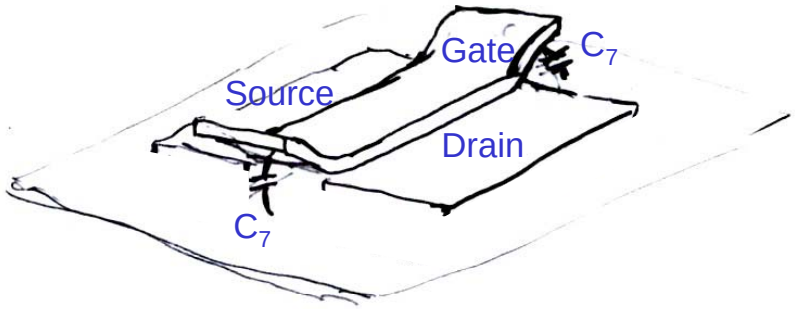
MJ: exponent of the source/drain bottom-plate junction capacitance. MJ may have a value as 0.5.

MJSW: exponent of the source/drain side-wall junction capacitance.

Gate-Channel and Gate-Substrate Capacitance

	Cut-off	Triode	Saturation
Gate-channel	0	$C_{ox}WL$	$2/3 \cdot C_{ox}WL$
Gate-substrate	$\frac{1}{\left(\frac{x_d}{\varepsilon_{si}WL}+\frac{1}{C_{ox}WL}\right)}+C_{GB,ov}$	$C_{GB,ov}$	$C_{GB,ov}$

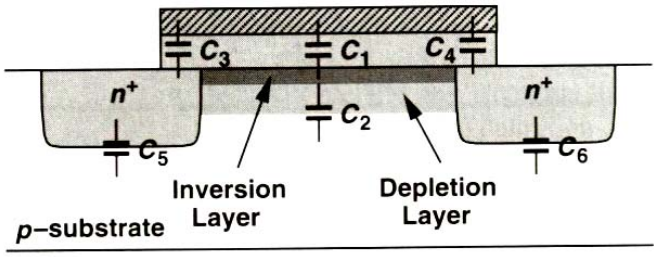
In the above table, $C_{GB,ov}$ is the overlap capacitance between gate and substrate, as shown in the following figure, $C_{GB,ov} = 2\ C_7$.



Gate-Source and Gate-Drain Capacitance

	Cut-off	Triode	Saturation
Gate-Source	$C_{GS,ov}$	$1/2 \cdot C_{ox}WL+C_{GS,ov}$	$2/3 \cdot C_{ox}WL+C_{GS,ov}$
Gate-Drain	$C_{GD,ov}$	$1/2 \cdot C_{ox}WL+C_{GD,ov}$	$C_{GD,ov}$

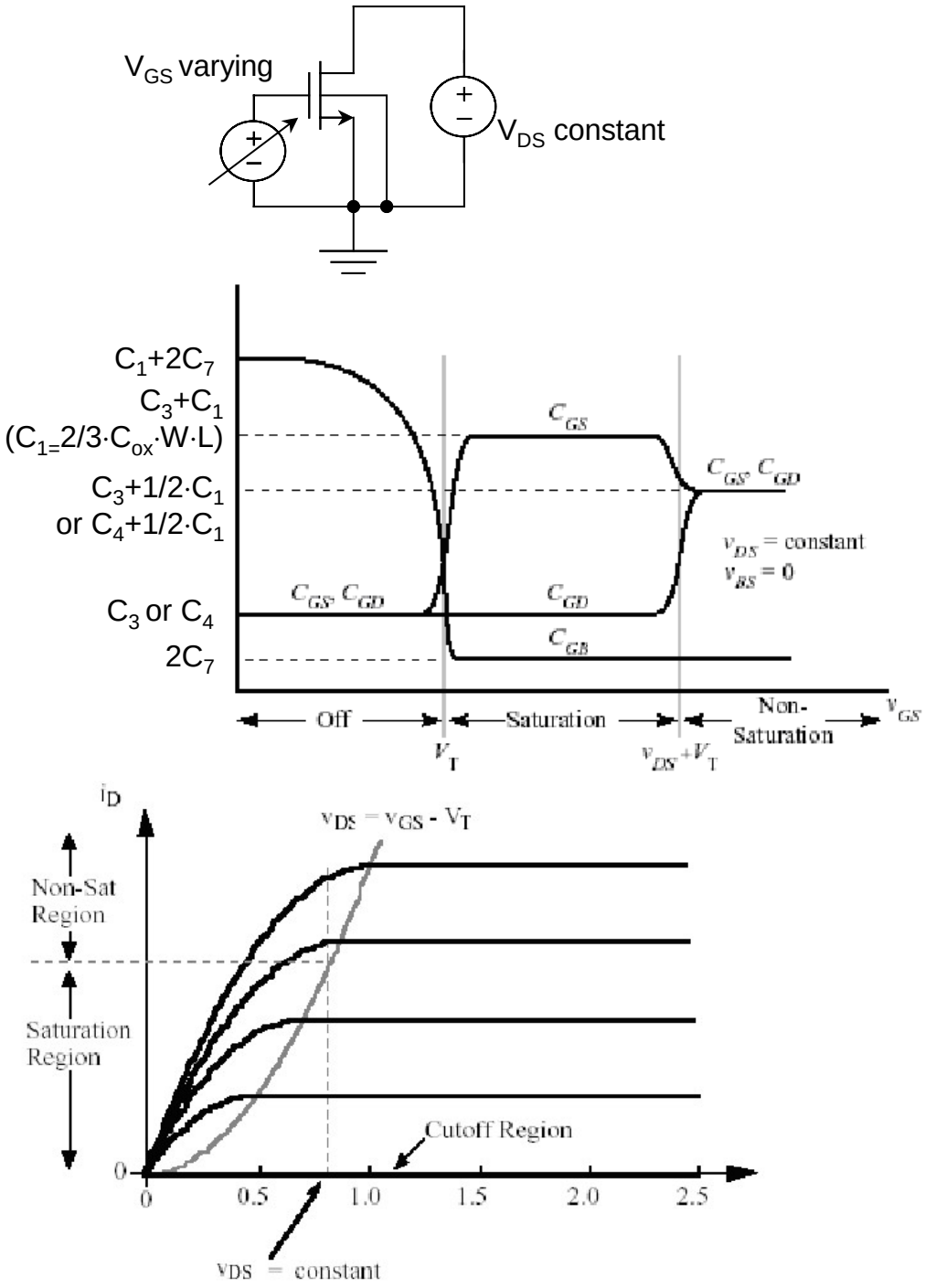
Gate-Source and Gate-Drain Overlap Capacitance, $C_{GS,ov}$ and $C_{GD,ov}$ (C3 and C4 in the following figure)



$$C_{GS,OV} = W \cdot CGSO$$
$$C_{GD,OV} = W \cdot CGDO$$

where CGSO and CGDO are the gate-source and gate-drain overlap capacitance per unit width (unit: F/m) in Spice Level 1 and Level 2 models. For example CGSO and CGDO can be 0.4e-9 F/m.

Variation of gate-source and gate-drain capacitance [allen02]

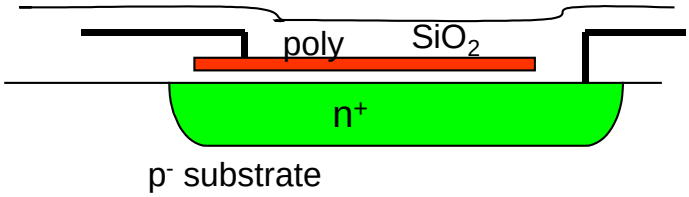


Passive Components

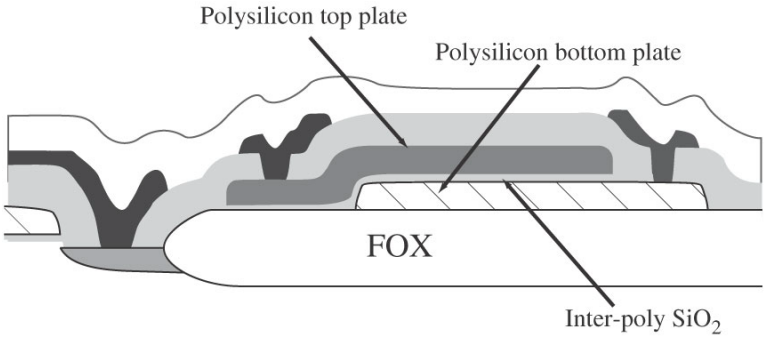
Capacitors [allen02]

Options

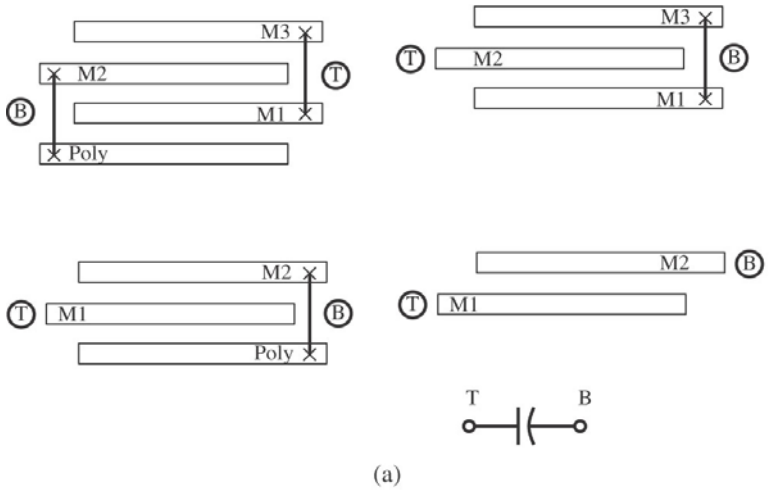
- poly-diffusion capacitor
- poly-poly capacitor
- metal-metal capacitor

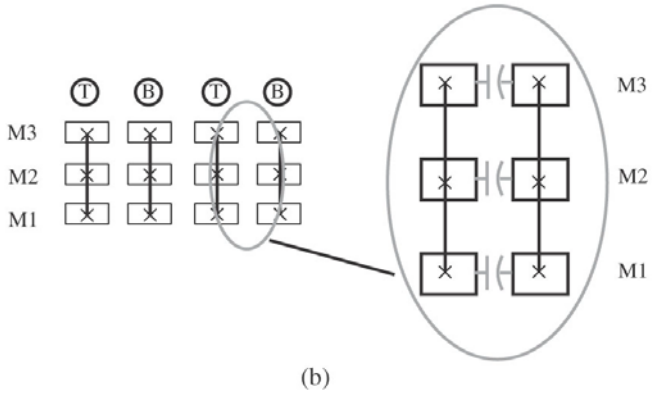


_____ capacitor

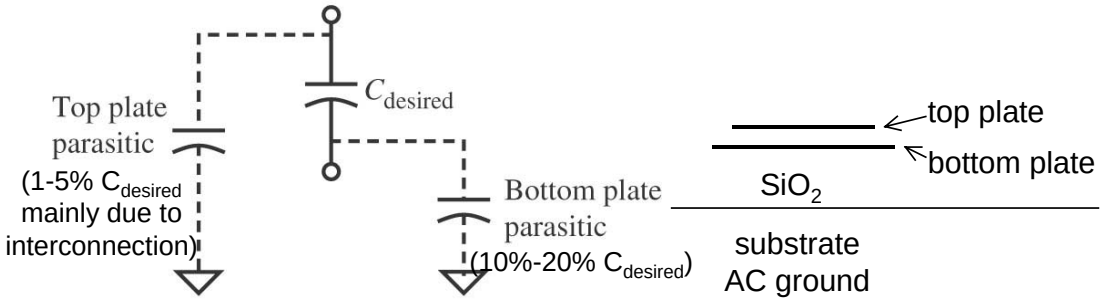


_____ capacitors





Various ways to implement capacitors using available interconnect layers, (a) vertical parallel plate structures, (b) horizontal parallel plate structures.



On chip capacitor equivalent diagram

Desired features of capacitors in analog circuits

- _____.
- Low voltage coefficient (high linearity)

- Low parasitic capacitance
- Low temperature dependence
- High capacitance per unit area

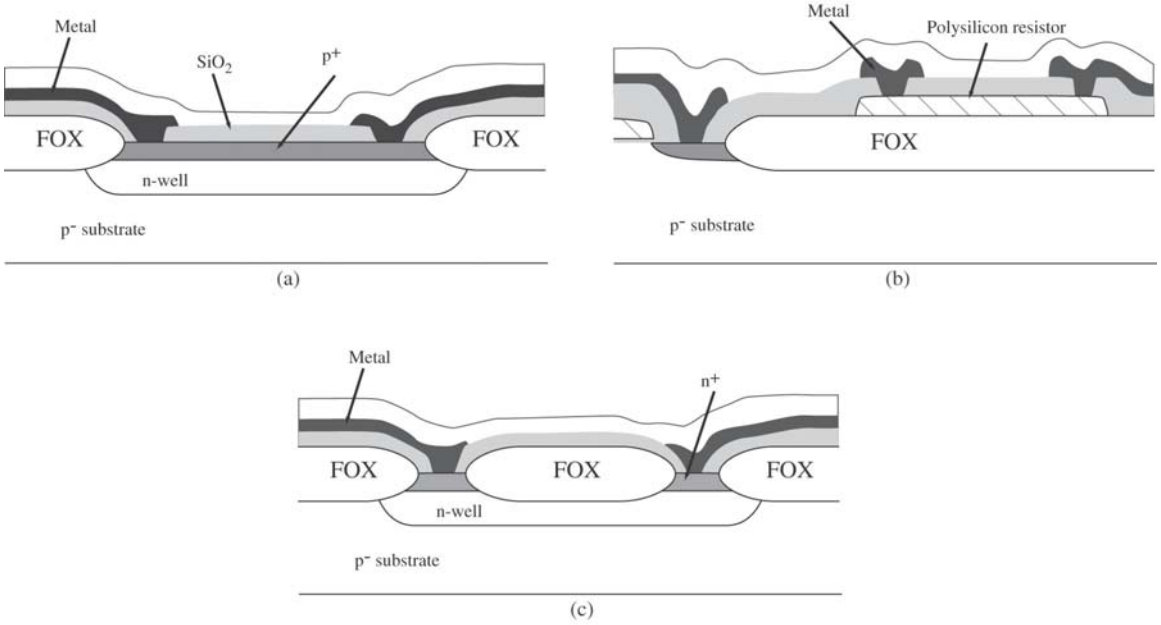
AMIS 0.5um process capacitance parameters

CAPACITANCE PARAMETERS	N+	P+	POLY	POLY2	M1	M2	M3	N_W	UNITS
Area (substrate)	430	725	85		32	17	11	40	aF/um^2
Area (N+active)			2457		36	17	12		aF/um^2
Area (P+active)			2365						aF/um^2
Area (poly)				873	57	17	10		aF/um^2
Area (poly2)					52				aF/um^2
Area (metal1)						36	14		aF/um^2
Area (metal2)							37		aF/um^2
Fringe (substrate)	328	272			78	60	42		aF/um
Fringe (poly)					64	40	29		aF/um
Fringe (metal1)						50	36		aF/um
Fringe (metal2)							53		aF/um
Overlap (N+active)			197						aF/um
Overlap (P+active)			229						aF/um

From http://www.mosis.org/cgi-bin/cgiwrap/umosis/swp/params/ami-c5/t49m-params.txt

Resistors

Poly resistors are frequently used in high performance analog circuits. Resistors of diffusion and well have large voltage coefficients.



On chip resistor options, (a) _____ resistor, (b) _____ (most frequently used) resistor, (c) _____ resistor

Desired features of resistors in analog circuits

- _____.
- Low voltage coefficient (high linearity)
- Low parasitic capacitance
- Low temperature dependence
- Suitable resistance per square

$$R = R_{contact} * 2 + R_{square} \frac{L}{W}$$

AMIS 0.5um process resistance parameters

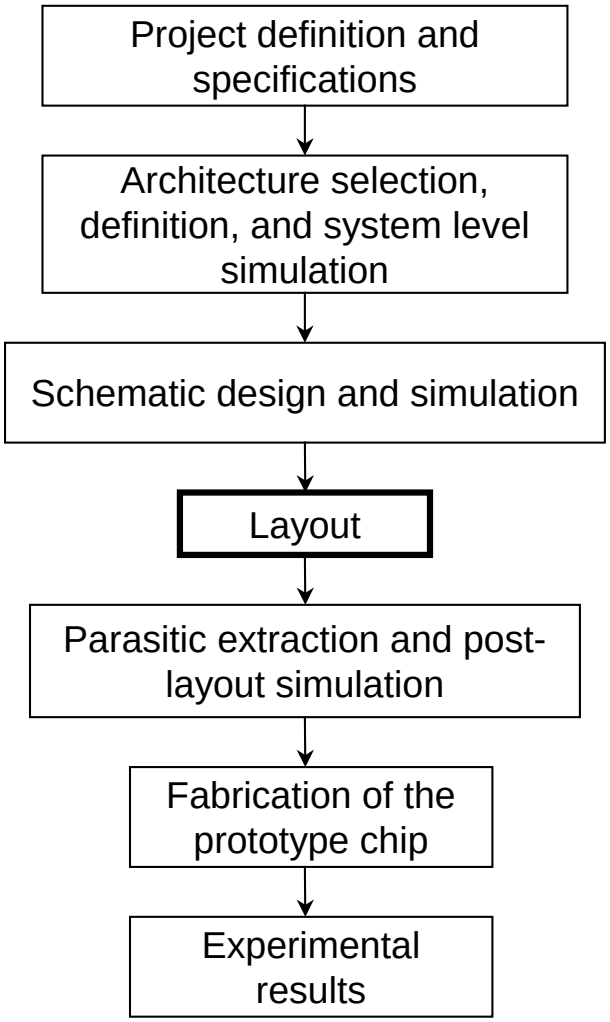
PROCESS PARAMETERS	N+	P+	POLY	PLY2_HR	POLY2	M1	M2	UNITS
Sheet Resistance	83.7	105.9	22.3	990	43.4	0.09	0.09	ohms/sq
Contact Resistance	67.2	152.9	16.0		29.1		0.84	ohms
Gate Oxide Thickness	141							angstrom

PROCESS PARAMETERS	M3	N\PLY	N_W	UNITS
Sheet Resistance	0.05	836	829	ohms/sq
Contact Resistance	0.85			ohms

From http://www.mosis.org/cgi-bin/cgiwrap/umosis/swp/params/ami-c5/t49m-params.txt

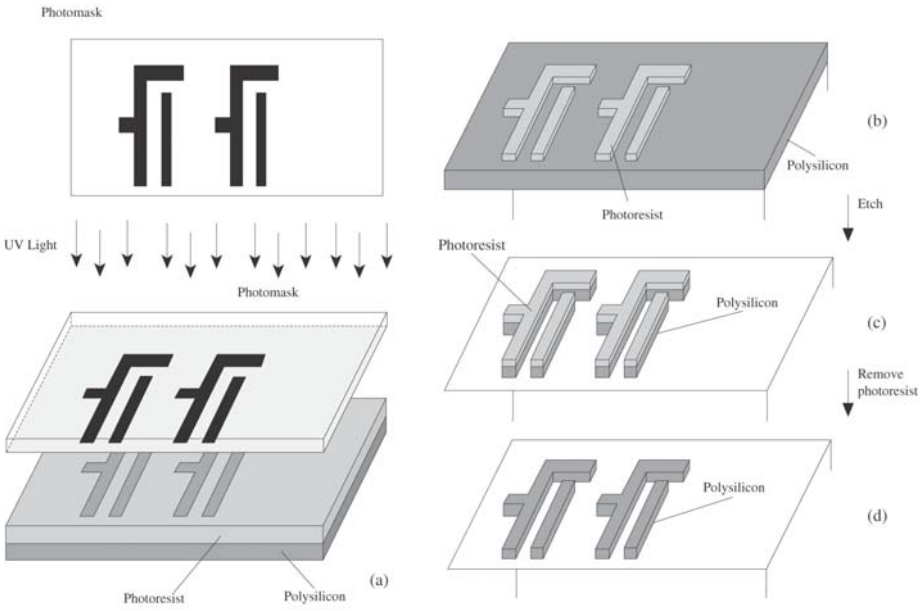
Layout of Analog Integrated Circuits

The design flow of analog integrated circuits

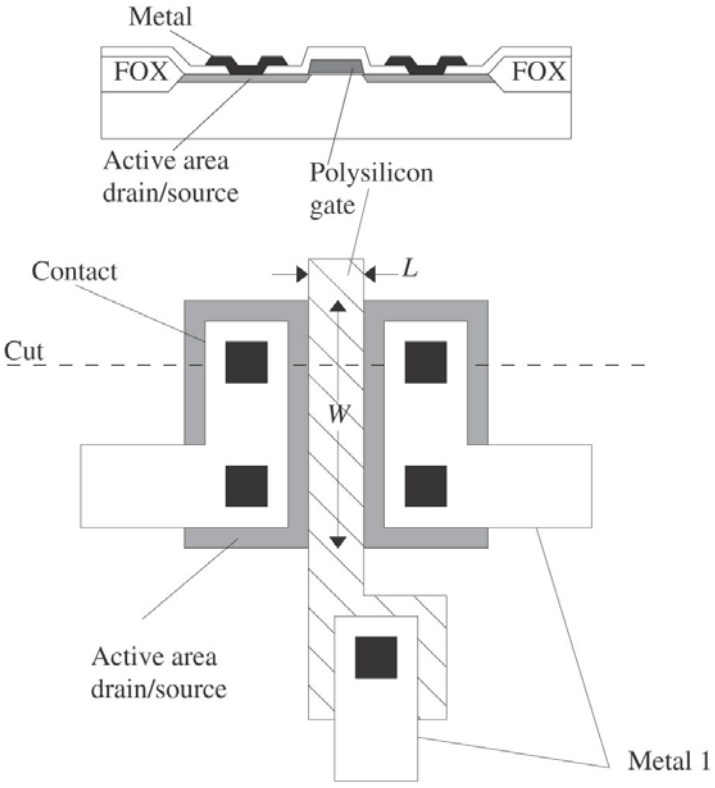


General layout considerations

The layout of integrated circuits defines the _____ that appear on the _____ used in fabrication.



Photomask and photolithography

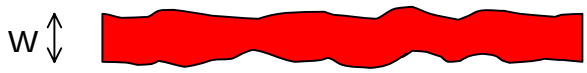


Layout of a MOS transistor

Layout rules or design rules

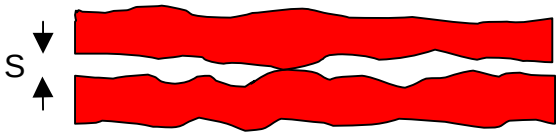
Layout rules or design rules are a set of rules that guarantee successful fabrication of integrated circuits despite various _____ in each step of the processing.

Minimum width



The width of the geometries defined on a mask must exceed a minimum value. For example, if a polysilicon rectangle is too narrow, it may suffer from a large local resistance or even break.

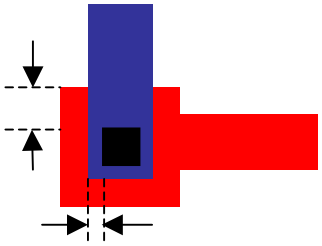
Minimum spacing



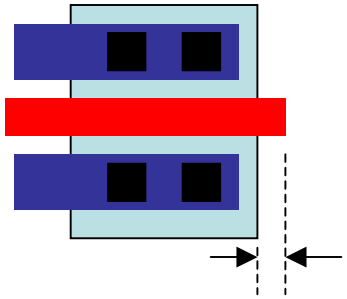
As an example, if 2 polysilicon lines are placed too close, they may be shorted.

Minimum enclosure

The n-well or the p+ implant must surround the transistor with sufficient margin to make sure that the device is contained within. Below is an example of enclosure rule for poly and metal surrounding a contact.



Minimum extension



As an example, the poly gate must have a minimum extension beyond the well to ensure that the transistor functions properly at the edge of well.

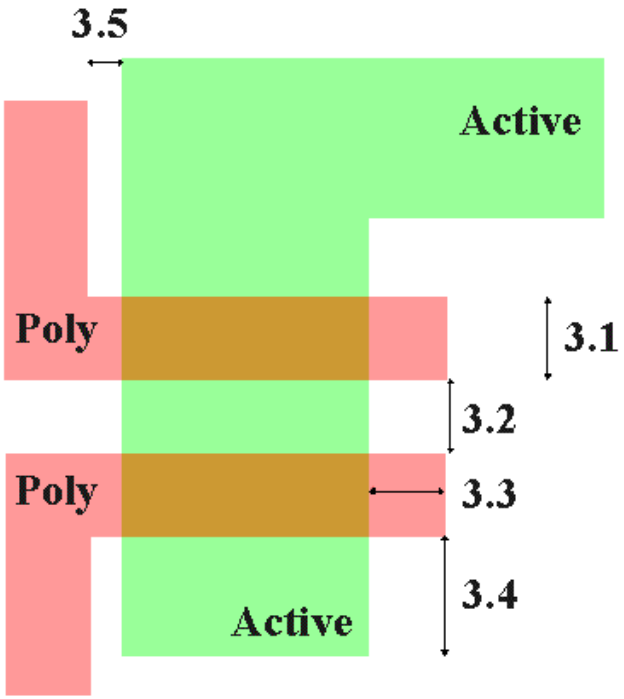
Please check the following webpage for MOSIS design rules,

http://www.mosis.org/Technical/Designrules/scmos/scmos-main.html

Example: design rules for poly layer

SCMOS Layout Rules - Poly

Rule	Description	Lambda		
		SCMOS	SUBM	DEEP
3.1	Minimum width	2	2	2
3.2	Minimum spacing over field	2	3	3
3.2.a	Minimum spacing over active	2	3	4
3.3	Minimum gate extension of active	2	2	2.5
3.4	Minimum active extension of poly	3	3	4
3.5	Minimum field poly to active	1	1	1



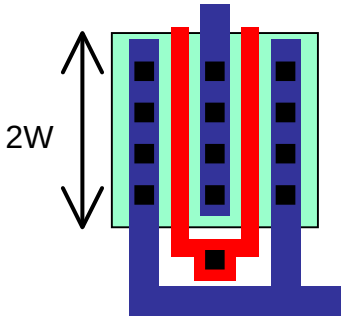
Design rules

Analog Layout Techniques

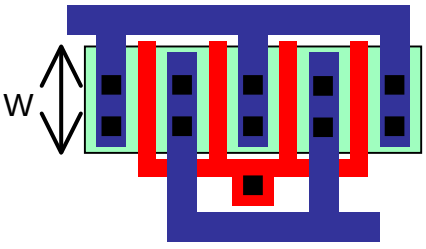
Multifinger transistors

For transistors that requires very large W/L ratio, a " folded " layout like figure (a) maybe not enough to reduce high gate resistance.

A layout like figure (b) is an improved version of figure (a) using multifinger transistor. The gate resistance is reduced by a factor of 4. While multifinger transistor reduces gate resistance, it raises source and drain capacitance, which introduces an trade-off.



(a)



(b)

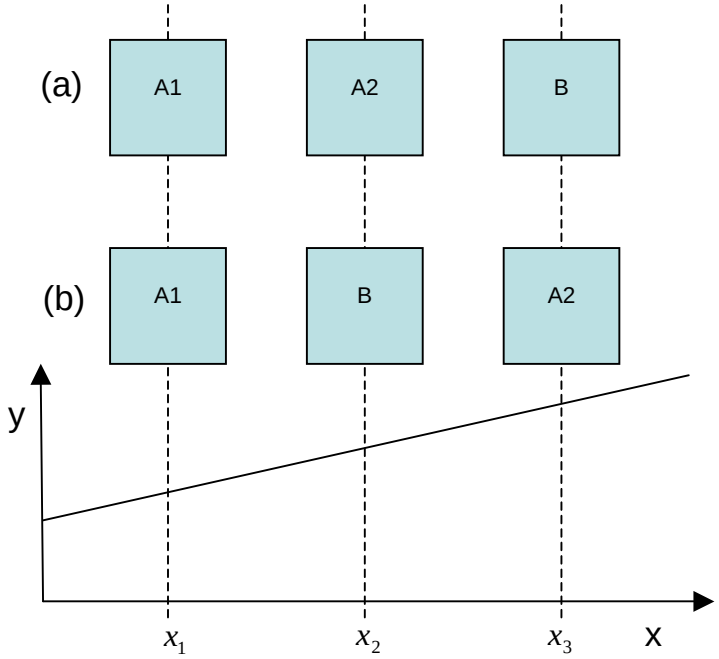
Symmetry and matching

1) Interdigitized (common centriod) layout

For process variation in local area, we can assume that the gradient of the variation is described as:

$$y = mx + b$$

Assume component A ,which is composed of units A1 and A2, should be twice the size of component B.



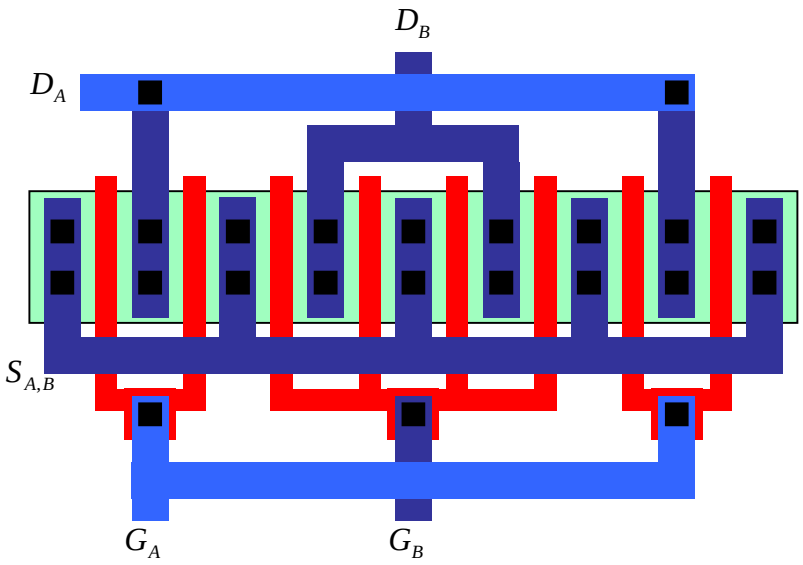
For a layout of (a) we have :

$$A1 = mx_1 + b$$
$$A2 = mx_2 + b$$
$$B = mx_3 + b$$
$$\frac{A1 + A2}{B} = \frac{m(x_1 + x_2) + 2b}{mx_3 + b} \neq 2$$

For a layout like (b) we have :

$$A1 = mx_1 + b$$
$$A2 = mx_3 + b$$
$$B = mx_2 + b$$
$$\frac{A1 + A2}{B} = \frac{m(x_1 + x_3) + 2b}{mx_2 + b} = 2$$

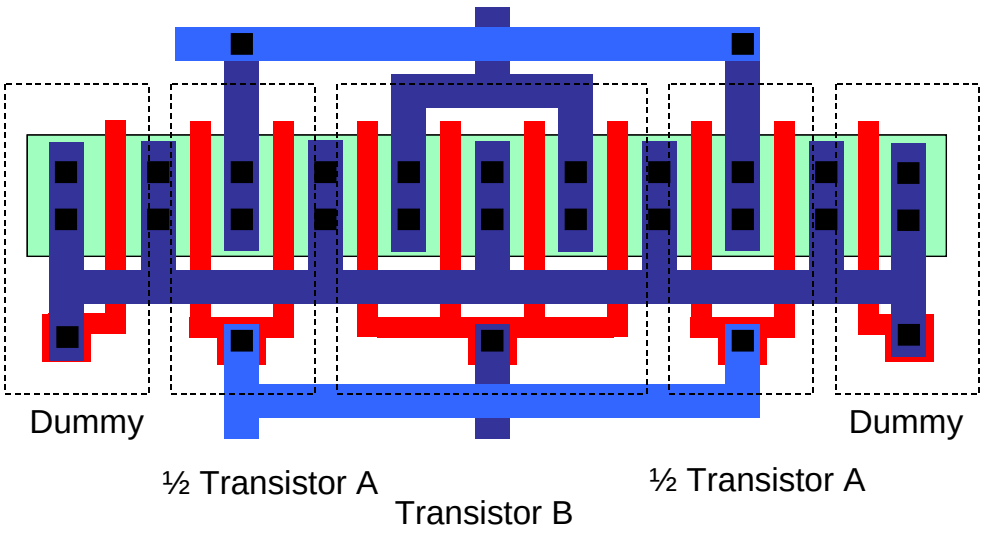
We call a layout like (b) a common-centroid layout.



An Example of common centroid layout

2) Using dummy transistors

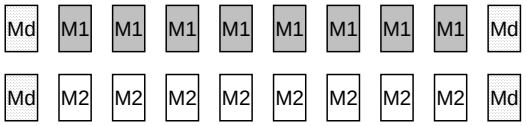
This is an improved version of the layout above. Two dummy transistors are added to the left and right sides. On the layout above, transistor A sees different ambient environment to the left and to the right. Dummy transistors improves the matching between transistor A and B by providing similar environment to the circuit that is on the boundary of a layout.



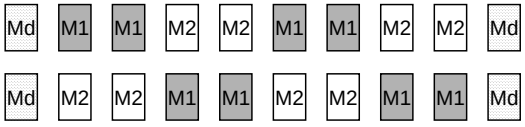
Example:

Which of the following layout patterns for two NMOS transistors (M1 and M2) can achieve the best matching with a linear gradient of process parameters (such as electron mobility $\mu 0$, and gate oxide thickness t_{ox}). Note that each of the small rectangle is a unit transistor, Mu. The interconnections between the Mu's are not drawn. Md's are dummy transistors which are grounded, and are not connected with M1 or M2.

A)

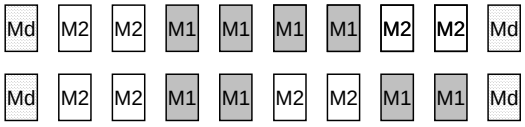


B)



C)

D)



E)

MOS Transistor Small Signal Models

NMOS transistor small signal model

For a MOS transistor, the drain current is a function of V_{GS}, V_{BS}, and V_{DS}.

$$I_D = \begin{cases} 0, & \text{(cut off)} \\ \frac{1}{2}K_p\left(\frac{W}{L}\right)(V_{GS}-V_T)^2(1+\lambda V_{DS}), & \text{(in saturation)} \\ K_p\left(\frac{W}{L}\right)\left[(V_{GS}-V_T)V_{DS}-\frac{V_{DS}^2}{2}\right], & \text{(in triode)} \end{cases}$$

where $K_p = \mu C_{ox} = \mu\frac{\varepsilon_{ox}}{t_{ox}}$ and $V_T = V_{T0}+\gamma(\sqrt{|2\phi_F|+V_{SB}}-\sqrt{|2\phi_F|})$.

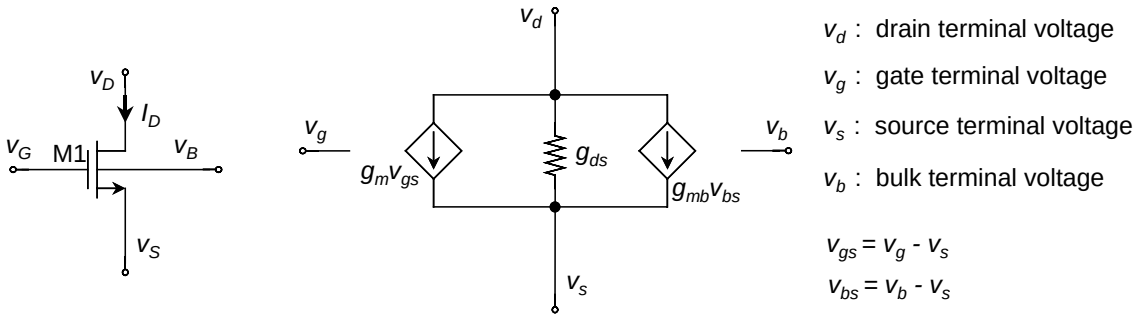
Or,

$$I_D(V_{GS},V_{BS},V_{DS}) = \begin{cases} 0, & \text{(cut off)} \\ \frac{1}{2}K_p\left(\frac{W}{L}\right)\left\{V_{GS}-\left[V_{T0}+\gamma(\sqrt{|2\phi_F|+V_{SB}}-\sqrt{|2\phi_F|})\right]\right\}^2(1+\lambda V_{DS}), & \text{(in saturation)} \\ K_p\left(\frac{W}{L}\right)\left[\left\{V_{GS}-\left[V_{T0}+\gamma(\sqrt{|2\phi_F|+V_{SB}}-\sqrt{|2\phi_F|})\right]\right\}V_{DS}-\frac{V_{DS}^2}{2}\right], & \text{(in triode)} \end{cases}$$

Thus,

$$\Delta I_D = \frac{\partial I_D}{\partial V_{GS}}\Delta V_{GS}+\frac{\partial I_D}{\partial V_{BS}}\Delta V_{BS}+\frac{\partial I_D}{\partial V_{DS}}\Delta V_{DS}$$

we define g_m as $\frac{\partial I_D}{\partial V_{GS}}$, g_{mb} as $\frac{\partial I_D}{\partial V_{BS}}$, and g_{ds} as $\frac{\partial I_D}{\partial V_{DS}}$.



Symbol Small signal model

Here v_b is shortened from v_{bulk}. Some other times, v_b means v_{bias}.

If we include the pn junctions and MOS capacitances, we have

Note that, g_o is another name of g_{ds}.

Saturation region (strong inversion): $V_{DS} > V_{GS} - V_T$, or $V_D > V_G - V_T$

Parameter	Considering $(1+\lambda V_{DS})$	Assuming $1+\lambda V_{DS} = 1$ in some steps
I_D	$\frac{1}{2}K_P\left(\frac{W}{L}\right)(V_{GS}-V_T)^2(1+\lambda V_{DS})$	$\frac{1}{2}K_P\left(\frac{W}{L}\right)(V_{GS}-V_T)^2$
g_m	$\left.\frac{\partial I_D}{\partial V_{GS}}\right\|_{VDS \text{ and } VBS \text{ keep constant}}$	

	$K_P\left(\frac{W}{L}\right)(V_{GS}-V_T)(1+\lambda V_{DS})$	$K_P\left(\frac{W}{L}\right)(V_{GS}-V_T)$
	$\sqrt{2I_D K_P\left(\frac{W}{L}\right)(1+\lambda V_{DS})}$	$\sqrt{2I_D K_P\left(\frac{W}{L}\right)}$
	$\frac{2I_D}{V_{GS}-V_T}$	$\frac{2I_D}{V_{GS}-V_T}$
g_{mb}	$\left.\frac{\partial I_D}{\partial V_{BS}}\right\|_{VGS \text{ and } VDS \text{ keep constant}} = \frac{\partial I_D}{\partial V_T}\frac{\partial V_T}{\partial V_{BS}}\Bigg\|_{VGS \text{ and } VDS \text{ keep constant}}$	
	ηg_m where $\eta = -\frac{\partial V_T}{\partial V_{BS}} = \frac{\gamma}{2\sqrt{\lvert 2\phi_F \rvert + V_{SB}}}$	
g_{ds}	$\left.\frac{\partial I_D}{\partial V_{DS}}\right\|_{VGS \text{ and } VBS \text{ keep constant}}$	
	$\frac{1}{2}K_P\left(\frac{W}{L}\right)(V_{GS}-V_T)^2\lambda$	N/A
	$\frac{\lambda I_D}{1+\lambda V_{DS}}$	λI_D

Triode region (strong inversion): $V_{DS} < V_{GS} - V_T$, or $V_D < V_G - V_T$

Parameter	Considering $(1+\lambda V_{DS})$ *	Assuming $1+\lambda V_{DS}=1$ in some steps
I_D	$K_p\left(\frac{W}{L}\right)\left[(V_{GS}-V_T)V_{DS}-\frac{V_{DS}^2}{2}\right](1+\lambda V_{DS})$	$K_p\left(\frac{W}{L}\right)\left[(V_{GS}-V_T)V_{DS}-\frac{V_{DS}^2}{2}\right]$
g_m	$\left.\frac{\partial I_D}{\partial V_{GS}}\right\|_{VDS \text{ and } VBS \text{ keep constant}}$	
	$K_P\left(\frac{W}{L}\right)V_{DS}(1+\lambda V_{DS})$	$K_P\left(\frac{W}{L}\right)V_{DS}$
g_{mb}	$\left.\frac{\partial I_D}{\partial V_{BS}}\right\|_{VGS \text{ and } VDS \text{ keep constant}} = \frac{\partial I_D}{\partial V_T}\frac{\partial V_T}{\partial V_{BS}}\Bigg\|_{VGS \text{ and } VDS \text{ keep constant}}$	
	ηg_m where $\eta = -\frac{\partial V_T}{\partial V_{BS}} = \frac{\gamma}{2\sqrt{\lvert 2\phi_F \rvert + V_{SB}}}$	
g_{ds}	$\left.\frac{\partial I_D}{\partial V_{DS}}\right\|_{VGS \text{ and } VBS \text{ keep constant}}$	

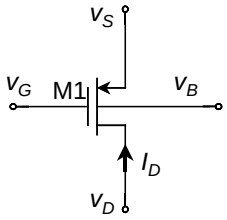
	$K_P\left(\frac{W}{L}\right)\{(V_{GS}-V_T-V_{DS})$ $+\lambda\left[(V_{GS}-V_T)V_{DS}-\frac{V_{DS}^2}{2}\right]\}$ (rarely used)	$K_P\left(\frac{W}{L}\right)(V_{GS}-V_T-V_{DS})$

* $(1+\lambda V_{DS})$ is added in the equation $K_p\left(\frac{W}{L}\right)\left[(V_{GS}-V_T)V_{DS}-\frac{V_{DS}^2}{2}\right](1+\lambda V_{DS})$ to bridge the equations in triode and saturation regions.

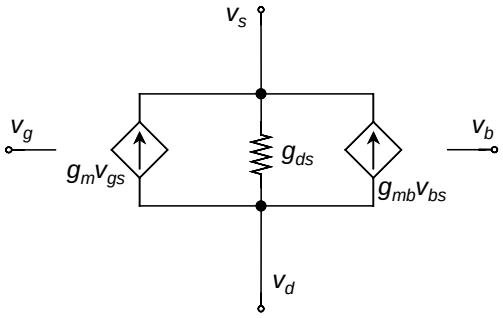
Note that $K_p=\mu C_{ox}=\mu\frac{\varepsilon_{ox}}{t_{ox}}$ and $V_T=V_{T0}+\gamma(\sqrt{|2\phi_F|+V_{SB}}-\sqrt{|2\phi_F|})$

$(V_{GS}-V_T)$ has different names in different books, V_{OV} (over drive voltage), V_{ON}, V_{dsat} (or $V_{ds(sat)}$, D-S saturation voltage). We mix using all of these terms.

PMOS transistor small signal model



Symbol



Small signal model

v_d : drain terminal voltage

v_g : gate terminal voltage

v_s : source terminal voltage

v_b : bulk terminal voltage

$v_{gs} = v_g - v_s$

$v_{bs} = v_b - v_s$

You may notice that we use the same small signal model for both PMOS and NMOS transistors.

We assume for both NMOS and PMOS transistors, the reference direction of the drain current is the direction that current flows into the transistor from drain terminal.

Please pay attention to the signs of in SPICE model parameters for NMOS and PMOS transistors.

Parameter	V_T	K_P	λ
NMOS	+	+	+
PMOS	–	–	+

For convenience, we use the absolute values of V_T and K_P of PMOS transistors to avoid confusion, i.e., we use $|V_T|$ and $|K_P|$.

Saturation region (strong inversion): $V_{SD} > V_{SG} - |V_T|$, or $V_D < V_G + |V_T|$

Parameter	Considering $(1+\lambda V_{SD})$	Assuming $1+\lambda V_{SD}=1$ in some steps
I_D	$-\frac{1}{2}\lvert K_P\rvert\left(\frac{W}{L}\right)(V_{SG}-\lvert V_T\rvert)^2(1+\lambda V_{SD})$	$-\frac{1}{2}\lvert K_P\rvert\left(\frac{W}{L}\right)(V_{SG}-\lvert V_T\rvert)^2$
g_m	$\left.\frac{\partial I_D}{\partial V_{GS}}\right\rvert_{VDS \text{ and } VBS \text{ keep constant}}$	
	$\lvert K_P\rvert\left(\frac{W}{L}\right)(V_{SG}-\lvert V_T\rvert)(1+\lambda V_{SD})$	$\lvert K_P\rvert\left(\frac{W}{L}\right)(V_{SG}-\lvert V_T\rvert)$
	$\sqrt{2\lvert I_D\rvert\lvert K_P\rvert\left(\frac{W}{L}\right)(1+\lambda V_{SD})}$	$\sqrt{2\lvert I_D\rvert\lvert K_P\rvert\left(\frac{W}{L}\right)}$
	$\frac{2\lvert I_D\rvert}{V_{SG}-\lvert V_T\rvert}$	$\frac{2\lvert I_D\rvert}{V_{SG}-\lvert V_T\rvert}$
g_{mb}	$\left.\frac{\partial I_D}{\partial V_{BS}}\right\rvert_{VGS \text{ and } VDS \text{ keep constant}} = \frac{\partial I_D}{\partial V_T}\frac{\partial V_T}{\partial V_{BS}}\Big\rvert_{VGS \text{ and } VDS \text{ keep constant}}$	
	ηg_m where $\eta = -\frac{\partial\lvert V_T\rvert}{\partial V_{BS}} = \frac{\gamma}{2\sqrt{\lvert 2\phi_F\rvert + V_{BS}}}$	
g_{ds}	$\left.\frac{\partial I_D}{\partial V_{DS}}\right\rvert_{VGS \text{ and } VBS \text{ keep constant}}$	
	$\frac{1}{2}\lvert K_P\rvert\left(\frac{W}{L}\right)(V_{SG}-\lvert V_T\rvert)^2\lambda$	N/A
	$\frac{\lambda\lvert I_D\rvert}{1+\lambda V_{SD}}$	$\lambda\lvert I_D\rvert$

Triode region (strong inversion): $V_{SD} < V_{SG} - |V_T|$, or $V_D > V_G + |V_T|$

Parameter	Considering $(1+\lambda V_{SD})$ *	Assuming $1+\lambda V_{SD}=1$ in some steps
I_D	$-\lvert K_p\rvert\left(\frac{W}{L}\right)\left[(V_{SG}-\lvert V_T\rvert)V_{SD}-\frac{V_{SD}^2}{2}\right]\times(1+\lambda V_{SD})$	$-\lvert K_p\rvert\left(\frac{W}{L}\right)\left[(V_{SG}-\lvert V_T\rvert)V_{SD}-\frac{V_{SD}^2}{2}\right]$

g_m	$\left.\frac{\partial I_D}{\partial V_{GS}}\right\|_{VDS \text{ and } VBS \text{ keep constant}}$	
	$\|K_P\|\left(\frac{W}{L}\right)V_{SD}(1+\lambda V_{SD})$	$\|K_P\|\left(\frac{W}{L}\right)V_{SD}$
g_{mb}	$\left.\frac{\partial I_D}{\partial V_{BS}}\right\|_{VGS \text{ and } VDS \text{ keep constant}} = \frac{\partial I_D}{\partial \|V_T\|}\left.\frac{\partial \|V_T\|}{\partial V_{BS}}\right\|_{VGS \text{ and } VDS \text{ keep constant}}$	
	ηg_m where $\eta = -\frac{\partial \|V_T\|}{\partial V_{BS}} = \frac{\gamma}{2\sqrt{\|2\phi_F\|+V_{BS}}}$	
g_{ds}	$\left.\frac{\partial I_D}{\partial V_{DS}}\right\|_{VGS \text{ and } VBS \text{ keep constant}}$	
	$\|K_P\|\left(\frac{W}{L}\right)\{(V_{SG}-\|V_T\|-V_{SD}) + \lambda\left[(V_{SG}-\|V_T\|)V_{SD}-\frac{V_{SD}^2}{2}\right]\}$ (rarely used)	$\|K_P\|\left(\frac{W}{L}\right)(V_{SG}-\|V_T\|-V_{SD})$

* $(1+\lambda V_{SD})$ is added in the equation $-|K_p|\left(\frac{W}{L}\right)\left[(V_{SG}-|V_T|)V_{SD}-\frac{V_{SD}^2}{2}\right](1+\lambda V_{SD})$ to bridge the equations in triode and saturation regions.

Note that, for PMOS transistor, $K_p = -\mu C_{ox} = -\mu\frac{\varepsilon_{ox}}{t_{ox}}$ and

$-V_T = -V_{T0}+\gamma(\sqrt{|2\phi_F|+V_{BS}}-\sqrt{|2\phi_F|})$ (or $V_T = V_{T0}-\gamma(\sqrt{|2\phi_F|+V_{BS}}-\sqrt{|2\phi_F|})$

References

[allen02] P. Allen and D. Holberg, "CMOS Analog Circuit Design", 2nd Ed., Oxford University Press, 2002.

[razavi01] B. Razavi, "Design of Analog CMOS Integrated Circuits", McGraw Hill, 2001.