SEMI-THERM®
The 32nd annual IEEE SEMI-THERM Symposium
Double Tree Hotel, San Jose, 14 March 2016

Short Course 4

Transient Measurements to Extract Resistances and Material Properties with hands-on demonstrations

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Mentor Graphics®

Basic concepts: R_{th}, Z_{th}, Ψ

What thermal metric and why? R_{th}

- A semiconductor device package can be well characterized for **steady-state operation** by its *thermal resistance*
  - The thermal resistance is a number which tells us how many degrees of junction temperature elevation is caused if a unit dissipation applied to the device
  - Power packages have large, exposed cooling tabs supporting heat-sunk thermal management solutions: thermal resistance as a metric is not problematic
    - There is a major, *dominant heat-flow path* from the junction to this cooling surface, resulting in an *essentially 1D* heat-flow
    - The *junction-to-case* thermal resistance (R_{thJC} or Θ_{JC}) is a usual characteristic of such packages
- Thermal resistance is a thermal metric used
  - To characterize "goodness" of a package
    - Should allow fair comparison between different vendors' products
  - Support simple system level thermal design
- Can be measured by simple tools as well as can be derived from transient measurements

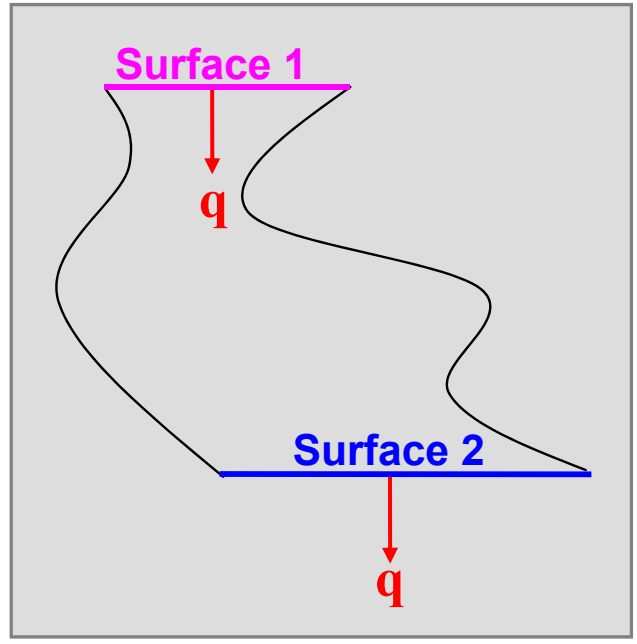
What thermal metric and why? Z_{th}

- For the **dynamic properties**, the *thermal impedance* is the right characteristic:
  - The usual representation of the thermal impedance is the ***junction temperature transient*** obtained a response to a unit-height power step at the junction
  - The thermal impedance carries *all information about the heat-flow path* such as
    - **thermal capacitance/resistance distribution** along the heat-flow path
      - Through this structural analysis is possible such as detection die attach problems and/or delamination/degradation of other thermal interfaces
    - effective thermal impedance in dynamic mode of device operation
      - PWM dimmed DC LEDs, AC driven LEDs, switching mode circuits (IGBTs)
- The thermal impedance is a unique characteristic of a package but can be represented in different forms
  - Conventional $Z_{th}(t)$ diagrams
  - Structure functions
  - Dynamic (transient) compact thermal network models
  - Complex locus in frequency domain
  - Pulsed thermal resistance diagrams
- Thermal resistance is derived from thermal impedance; both require the amount of physical measurement time

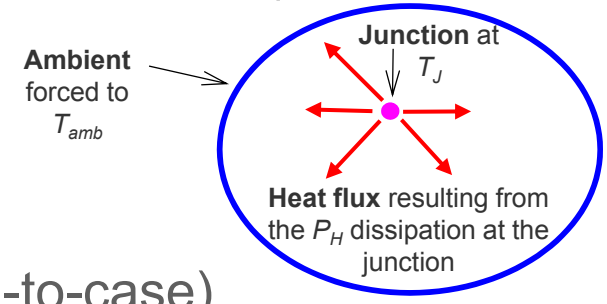
Definition of thermal resistance?

Required conditions to be able to define R_{th} between two points in space:

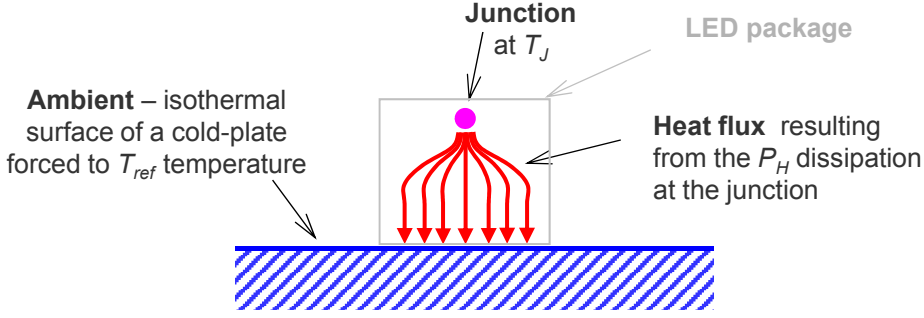
1. surfaces must be isothermal
2. the entire heat-flux **q** entering the heat-flow path at **Surface 1** must leave at **Surface 2**



- Real life situations: the above conditions are well met:
  - R_{thJA} (junction-to-ambient)



  - R_{thJC} (junction-to-case)



Same conditions apply also for *driving point* thermal impedances…

A few words about thermal resistance

- Original definition in the JEDEC JESD51-1 document

2. MEASUREMENT BASICS

The thermal resistance of a semiconductor device is generally defined as:

$$R_{JX} = \frac{T_J - T_x}{P_H}$$

where $R_{\theta JX}$ = thermal resistance from device junction to the specific environment (alternative symbol is θ_{JX}) [°C/W]
T_J = device junction temperature in the steady state test condition [°C]
T_X = reference temperature for the specific environment [°C]
P_H = power dissipated in the device [W]

- Classically, for Si semiconductor diodes: $R_{th} = \Delta T_J / (I_F \times V_F)$ (1a)
- For LEDs, consider the radiant flux: $R_{th\text{-}r} = \Delta T_J / (I_F \times V_F - P_{opt})$ (1b)

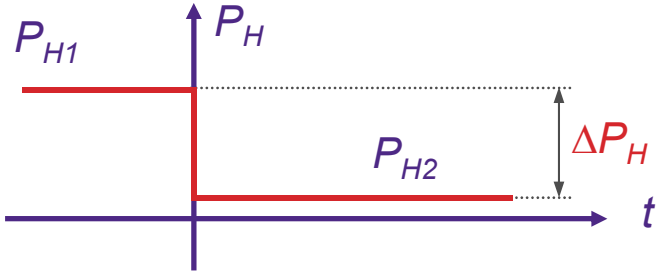
Junction temperature – performance indicator

- Calculation: $T_J = R_{thJ\text{-}X} \cdot P_H + T_X$ (2)
  - $R_{thJ\text{-}X}$ *junction-to-reference_X thermal resistance* supplied by the LED vendor
  - P_H *heating power* measured/calculated by the user
  - T_X *reference temperature* (un)specified by the LED user
- Used in the design process to decide if the foreseen cooling is sufficient or not...
  - in case of LEDs, prediction of "hot lumens" is also required

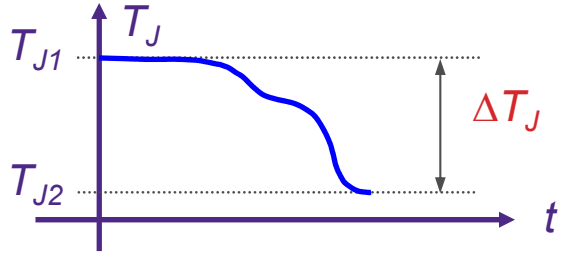
Differential formulation of the thermal resistance

$$R_{thJ-X} = \frac{T_J - T_X}{P_H} = \frac{[\Delta T_J]_X}{P_H}$$

Instead of spatial difference (temperature values at junction and reference point) temporal difference of the junction temperature can be used

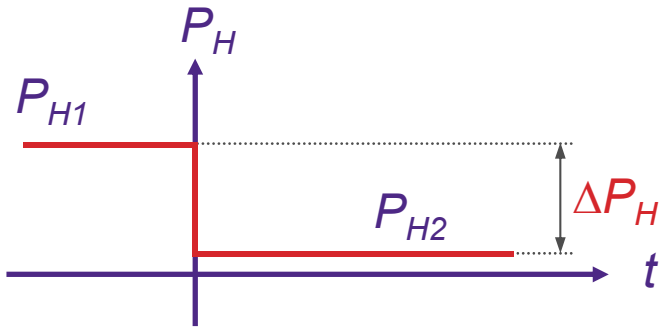


$$R_{thJ-X} = \frac{\Delta T_J(\infty)}{\Delta P_H}$$

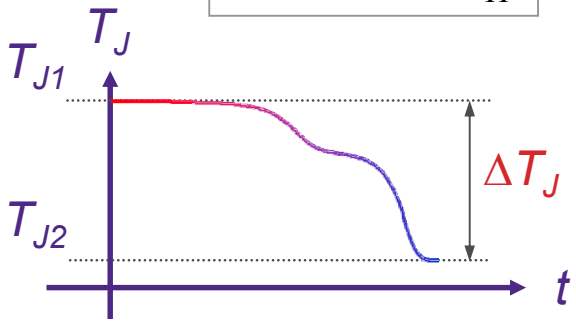


Differential formulation of the thermal resistance

- Alternate formulation: instead of spatial difference, we can also calculate with a ***temporal difference*** of the junction temperature (temp. transient):



$$R_{thJ-X} = \frac{\Delta T_J}{\Delta P_H}$$



$R_{th\ J\text{-}X}(t) = \Delta T_J(t) / \Delta P_H$ is called **Z_{th} curve**

$$T_{J1} = R_{th\ J\text{-}X} \cdot P_{H1} + T_X \quad (4a)$$

$$T_{J2} = R_{th\ J\text{-}X} \cdot P_{H2} + T_X \quad (4b)$$

$$T_{J2} - T_{J1} = R_{th\ J\text{-}X} \cdot (P_{H2} - P_{H1}) \quad (5)$$

Let $T_{J1}=T_J(t_1)$ and $T_{J2}=T_J(t_2)$:

$$R_{th\ J\text{-}X} = [T_J(t_2) - T_J(t_1)] / (P_{H2} - P_{H1}) \quad (6)$$

$$\boldsymbol{R_{th\ J\text{-}X}(t) = \Delta T_J(t) / \Delta P_H} \quad (7)$$

If t_1=0 and t_2=∞ ➔ $R_{th\ J\text{-}X} = \Delta T_J / \Delta P_H$

If P_{H2} = 0, then $T_{J2} = T_X$

The JEDEC thermal testing standards

Why to use standards?

- Our goals by using standards is to make sure that what we do is
  - Commonly understood by others
    - ➔ standards are publicly available by anybody
  - Is repeatable by others
    - ➔ standards can be implemented by anybody
  - Is compatible with what others do
    - ➔ if most vendors / end-users apply the same standards, results can be compared

- Measurement standards
  - Provide definitions of terms/quantities/metrics
  - Define test methods and procedures
  - Define test environments
  - Define data reporting

- Standard thermal tests reflect characteristics of test devices and conditions, not real-life applications
  - One has inherently to simplify conditions compared to real-life, otherwise the goals (common understanding & reproducibility) can not be guaranteed

Standards make measurements reproducible

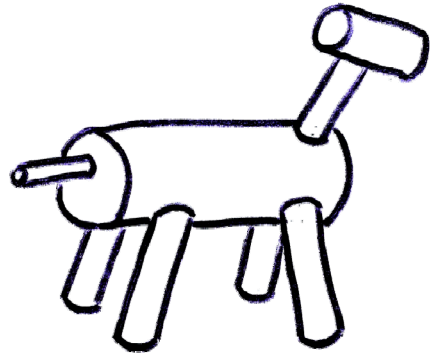
- Real life conditions must be simplified for standardized measurements
  - Good standards provide metrics which are close to real life conditions
  - Deviation from real-life conditions must be on the "safe" side

- Example for simplification of real life conditions

Real life horse

Too many individual, particular details
- color
- sex, muscles, teeth, etc

"Standard" horse



No individual details, but major characteristics of a real horse maintained
- has got four legs,
- has got a body, a neck, a head and a tail
- weight and form factor close to an average horse

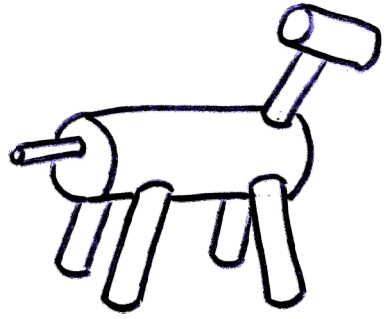
Original standard horse example from Bruce Guenin, chairman of the JEDEC JC15 Committee on standardization of thermal characterization of packaged semiconductor devices

Example from electronics cooling: power transistor

- How test conditions of power transistors can be standardized?

Real life horse

"Standard" horse

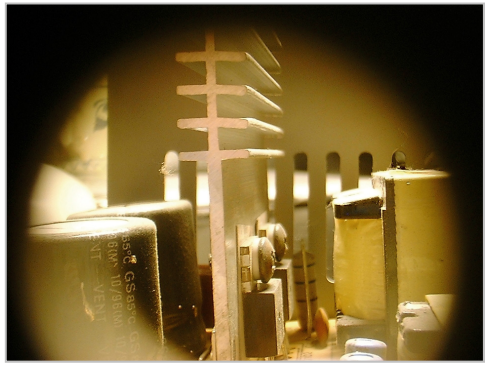


Implementation of the "Standard" horse

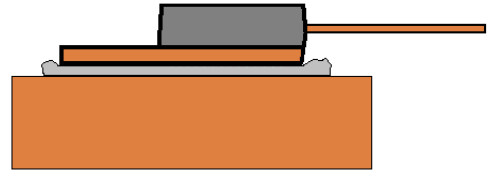
Standard features

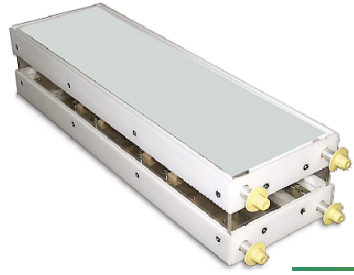
Additional features

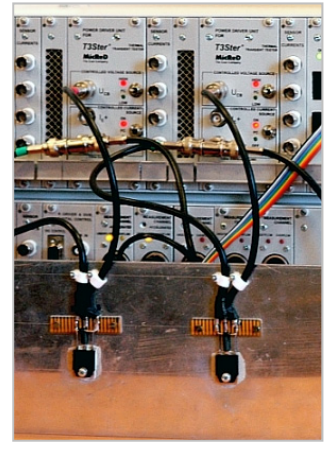
Real life application environment of **power transistors**: attached to a forced air cooled heat-sink



Standard test condition of **power transistors**: attached to a liquid cooled cold plate



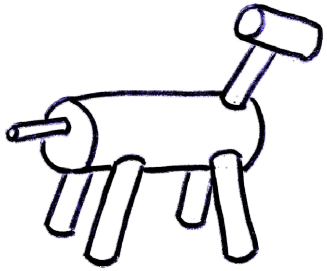




JEDEC thermal characterization standards

- Classical standards: JESD51- series of documents

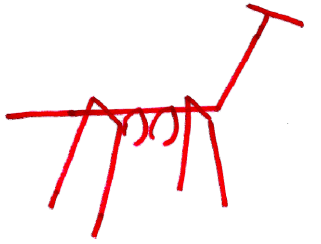
"JEDEC standard" horse



"JEDEC standard STATIC horse": JESD51-* series (1,2,3,4, etc) provide
- terms and definitions
- basic test methods (electrical test methods: static / dynamic)
- test environments (natural convection, forced air) and test boards
- data reporting guidelines

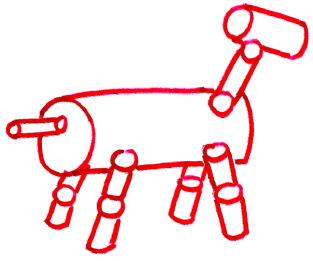
JESD51 – overview document

- Some "new" JEDEC thermal standards:

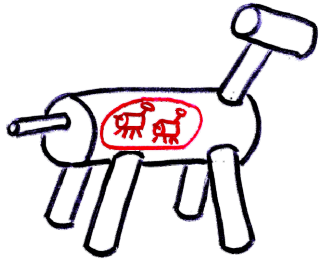


"JEDEC standard horse models": JESD15-* series for thermal compact modeling of packages
- compact modeling overview
- 2R and DELPHI models

Work on standard model library file format in progress



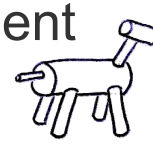
"JEDEC standard DYNAMIC horse": JESD51-14 – the first thermal transient testing standard using structure functions
- new standard for junction-to-case thermal resistance measurement
- defines a cold plate as test environment
- defines thermal transient measurement and structure function analysis as test method



Extension of JESD51-* series standards to account for multi-chip packages
- JESD51-3x documents extend definitions of environmental conditions and test boards for multi-die packages

List of JEDEC thermal characterization standards

- Below we give the comprehensive list of JEDEC thermal measurement and modeling standards:

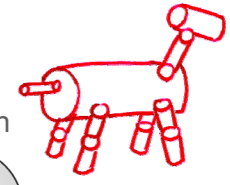


Classical set of standards for steady-state measurements:

- JESD51 **Methodology** for the Thermal Measurement of Component Packages (Single Semiconductor Device) (1995)
- JESD51-1 Integrated Circuits Thermal Measurement Method - Electrical **Test Method** (Single Semiconductor Device) (1995)
- JESD51-2A Integrated Circuits Thermal Test Method **Environmental Conditions** - Natural Convection (Still Air) (2008)
- JESD51-3 Low Effective Thermal Conductivity ***Test Board*** for Leaded Surface Mount Packages (1996)
- JESD51-4 **Thermal Test Chip Guideline** (Wire Bond Type Chip) (1997)
- JESD51-5 Extension of Thermal ***Test Board*** Standards for Packages with Direct Thermal Attachment Mechanisms (1999)
- JESD51-6 Integrated Circuit Thermal Test Method **Environmental Conditions** - Forced Convection (Moving Air) (1999)
- JESD51-7 High Effective Thermal Conductivity ***Test Board*** for Leaded Surface Mount Packages (1999)
- JESD51-8 Integrated Circuit Thermal Test Method **Environmental Conditions** - Junction-to-Board (1999)
- JESD51-9 ***Test Boards*** for Area Array Surface Mount Package Thermal Measurements (2000)
- JESD51-10 ***Test Boards*** for Through-Hole Perimeter Leaded Package Thermal Measurements (2000)
- JESD51-11 ***Test Boards*** for Through-Hole Area Array Leaded Package Thermal Measurements (2001)
- JESD51-12 **Guidelines for Reporting** and Using Electronic Package Thermal Information (2005)
- JESD51-13 Glossary of **Thermal Measurement Terms and Definitions** (2009)

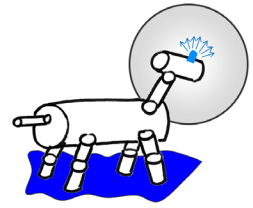
The first transient measurement standard:

- JESD51-14 **Transient Dual Interface Test Method** for the Measurement of the Thermal Resistance Junction to Case of Semiconductor Devices with Heat Flow Trough a Single Path **(2010)**



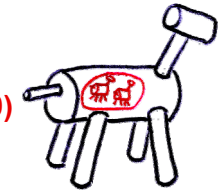
LED thermal testing standards:

- JESD51-5x **Anew subgroup of thermal testing standards aimed at power LEDs (2012)**



Extension of existing standards to multi-chip packages:

- JESD51-31 Thermal Test Environment Modifications for **Multi-Chip Packages (2008)**
- JESD51-32 Extension to JESD51 Thermal Test Board Standards to Accomodate **Multi-Chip Packages (2010)**

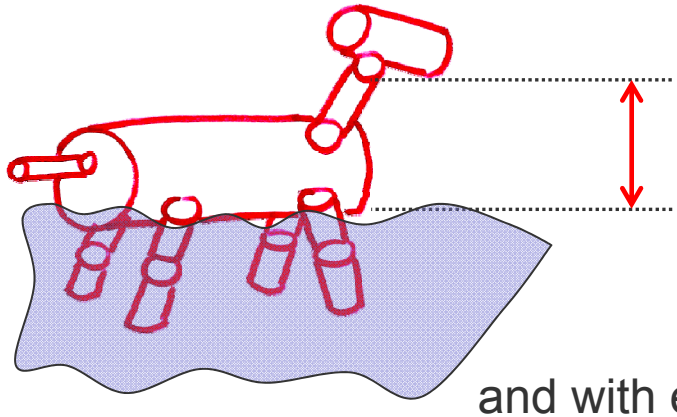


Compact modeling guidelines:

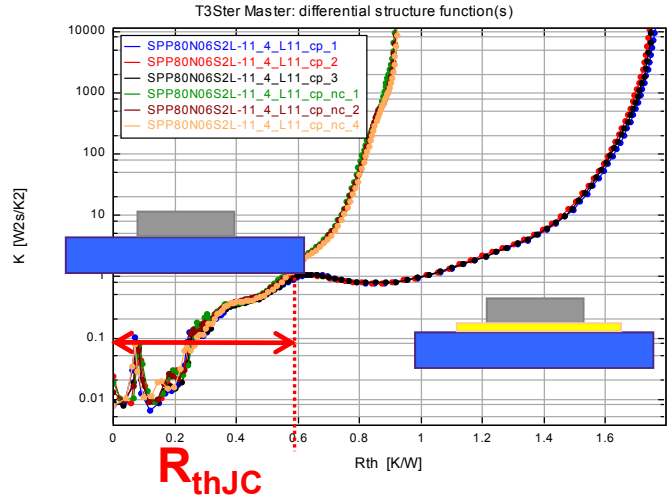
- JESD15-1 Compact Thermal Model Overview **(2008)**
- JESD15-2 **Terms and Definitions** for Modeling Standards (not yet launched)
- JESD15-3 Two-Resistor Compact **Thermal Model Guideline (2008)**
- JESD15-4 DELPHI Compact **Thermal Model Guideline (2008)**

New standard "horses" – R_{thJC} with transient (2010)

- JESD51-14: R_{thJC} measurement with the dual thermal interface method
  - Measure twice: without

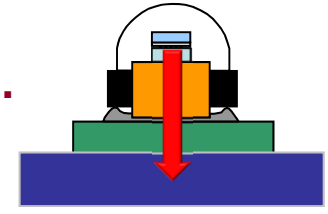


and with extra layer



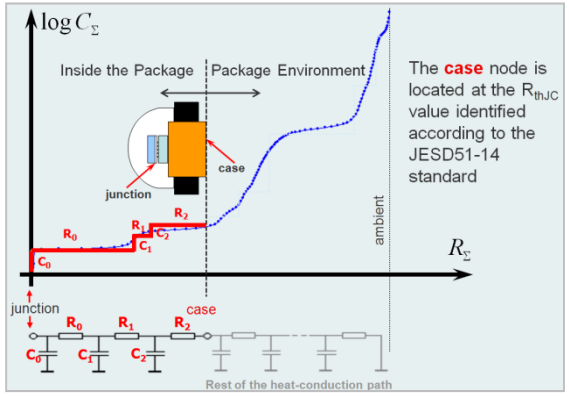
  - Location of deviation with respect to the junction defines R_{thJC}

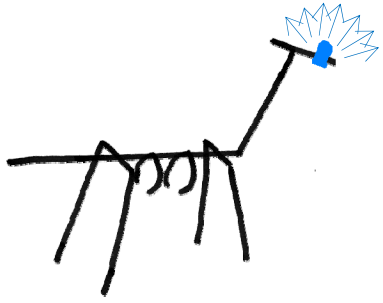
- Published in November 2010
- Applicable to power semiconductor device packages with an exposed cooling surface and a single heat-flow path
- **This condition is valid power LEDs as well, thus**
- **JESD51-14 well applicable to LEDs provided that, ….**

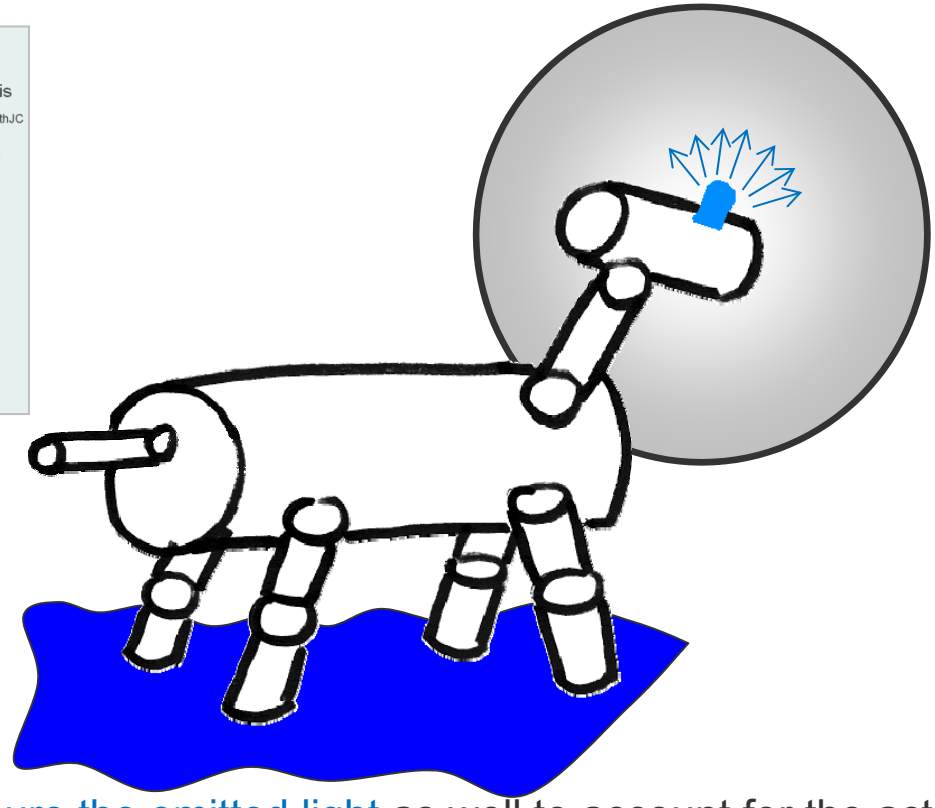


New standard "horses" – LED testing (2012)

- JESD51-50, 51, 52, 53 series LED thermal testing guidelines







Measure the emitted light as well to account for the actual heating
Measure on cold-plate to assure thermal steady-state for light measurements

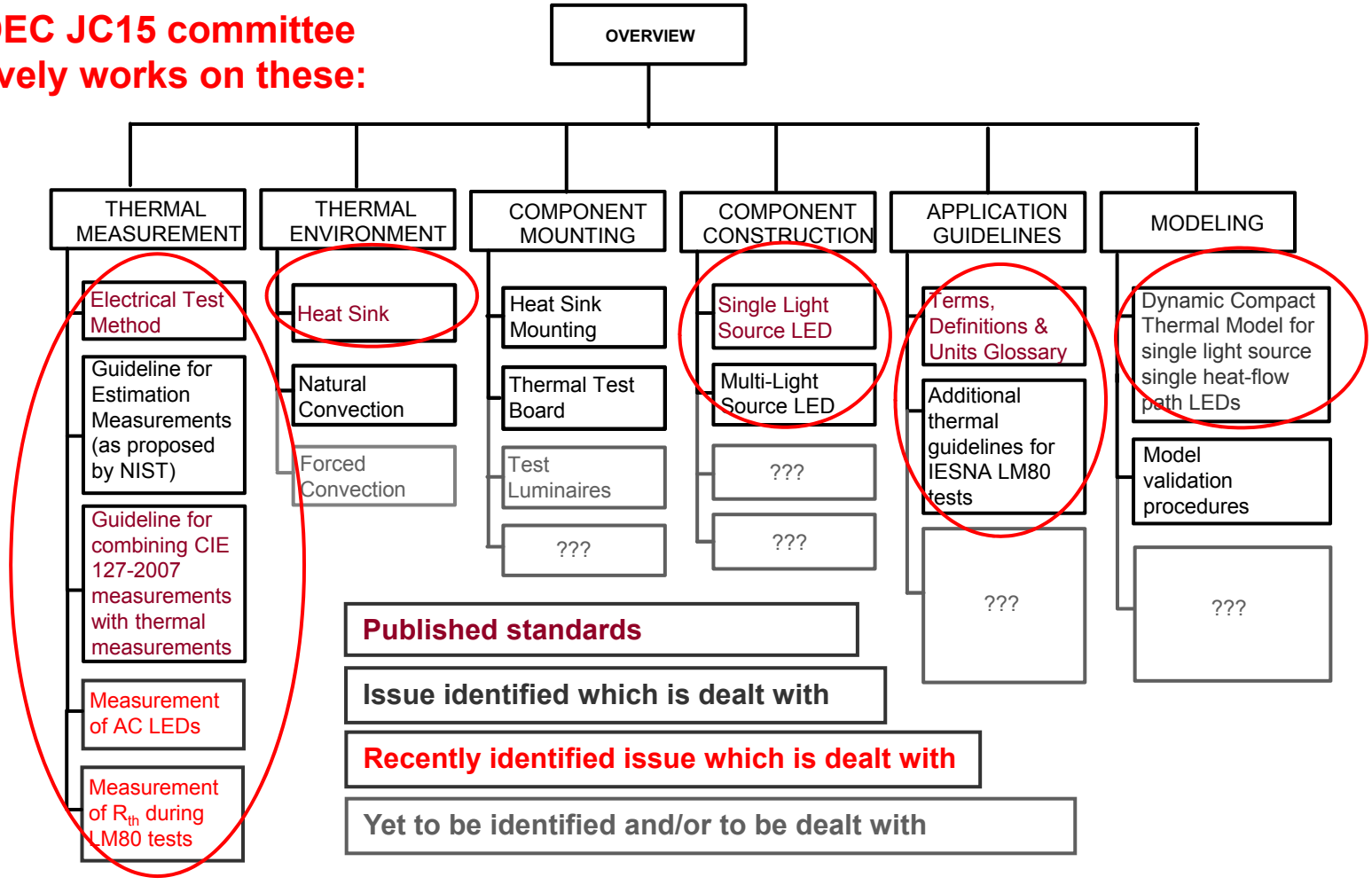
- This combined with a JESD51-14 compliant R_{thJC} measurement allows test based compact thermal modeling of power LED packages

Will be discussed later today…

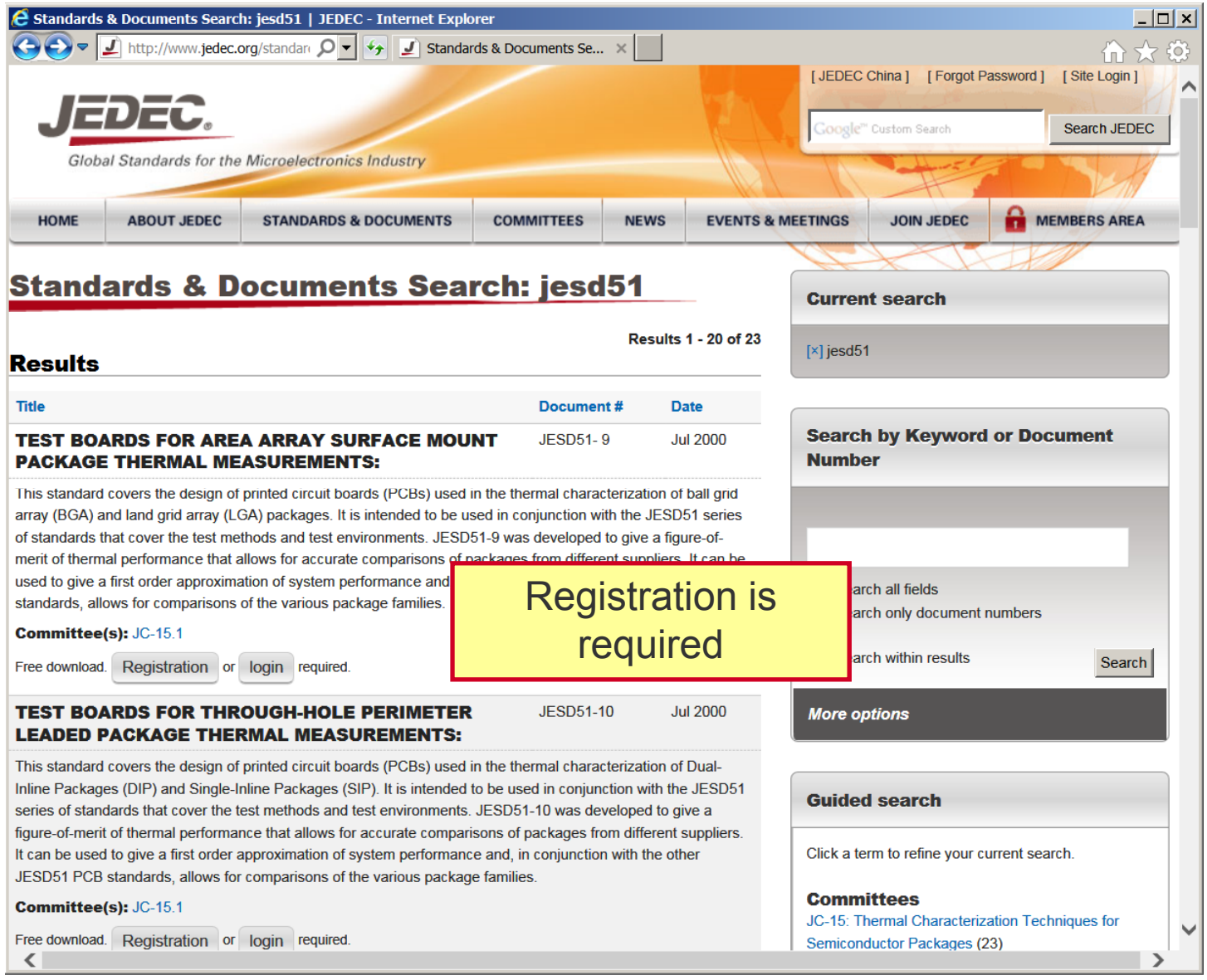
Approach of the JEDEC JC15 committee

- JESD51-50: LED thermal testing overview document

JEDEC JC15 committee actively works on these:



Standards are downloadable from www.jedec.org:



Some examples

- Glossary of terms and definitions

3 Terms and definitions (cont'd)

heating pulse width: the length of time electrical power is applied to the device-under-test to cause the junction temperature to rise.

heating voltage: the voltage across the DUT during the application of HEATING CURRENT.

heat sink: an external object in contact with component package for purposes of removing heat from the component.

junction temperature: the temperature of the operating portion of a semiconductor device.

K Factor: the quotient of junction temperature change to temperature sensitive parameter change in linear region of temperature sensitive parameter - temperature relationship.

K Factor calibration: the measurement and data reduction process that results in values of K factor for the semiconductor device.

measurement current: the current applied to the device-under-test for the measurement of the temperature sensitive parameter.

Some examples

- Guidelines of reporting thermal test data

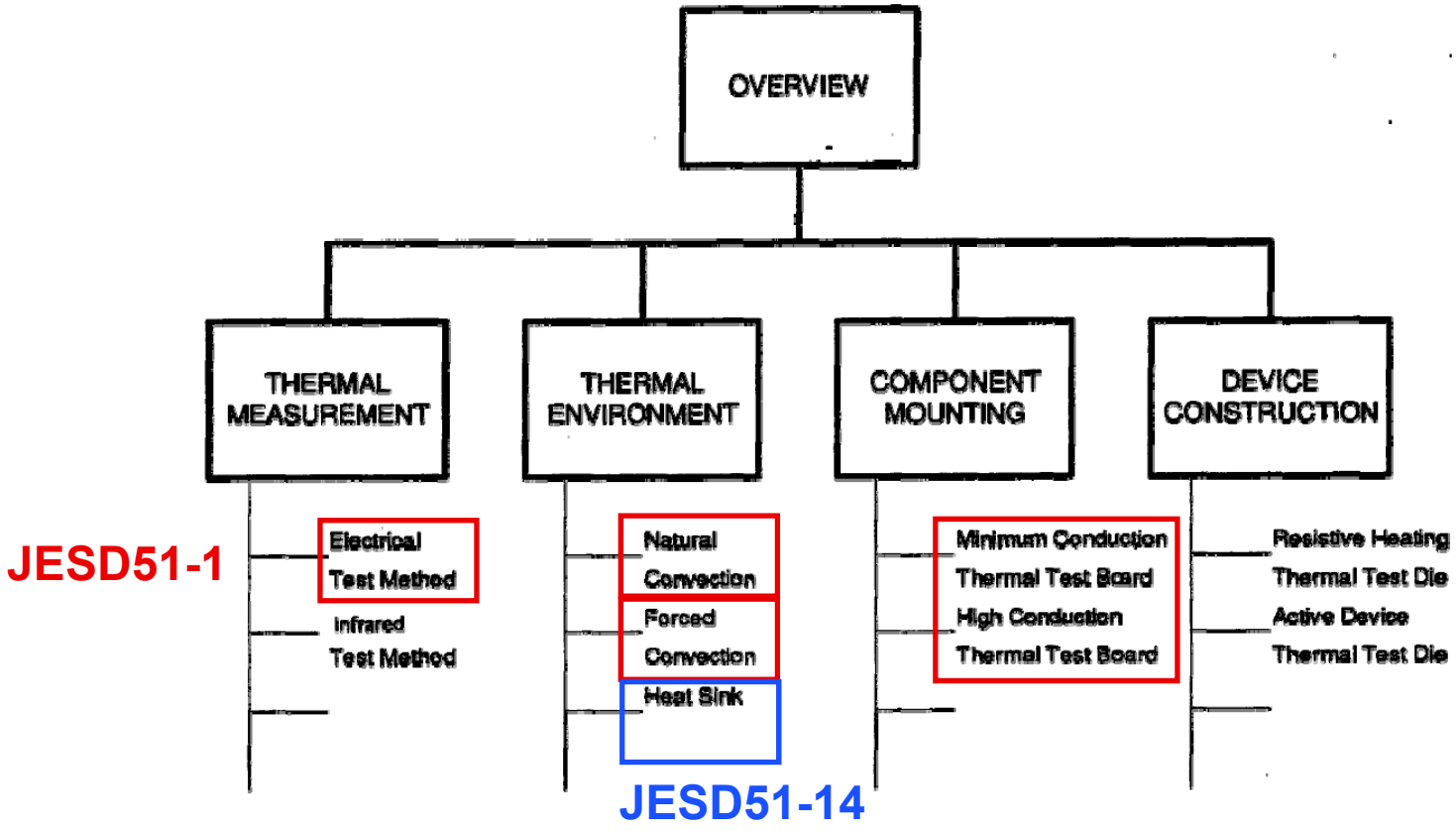
4 Reporting electronic package thermal results (cont'd)

Table 1 — JESD51 Thermal measurement standards by category

ENVIRONMENT[1]	CHIP	BOARD[4]	MEASUREMENT METHOD
• Natural Convection (Still Air), one cubic foot enclosure, θ_{JA}, Ψ_{JT} [3] [2] • Forced Convection (Moving Air), wind tunnel, θ_{JMA}, Ψ_{JT}, Ψ_{JB} [7] • Junction-to-Board, θ_{JB} [9] • Junction-to-Case, θ_{JCx} [3]	• Thermal Test Chip – Wire Bond Type [5] • Thermal Test Chip – Flip Chip Type (not yet available; refer to [5] for applicable information) • Active Die or Thermal Test Die [2]	• Low Effective Thermal Conductivity (1s board), Leaded Surface Mount Packages [4,6[5]] • High Effective Thermal Conductivity (2s2p board), Leaded Surface Mount Packages [8,6[4]] • Area Array Surface Mount Packages (1s and 2s2p boards) [10] • Through-Hole Perimeter Leaded Packages (1s and 2s2p boards) [11] • Through-Hole Area Array Leaded Packages (1s and 2s2p boards) [12]	• Static Mode or Dynamic Mode; Active Die or Thermal Test Die [2]

The JESD51 standard – overview document

- The thermal testing standards follow a modular structure:



Each group will have one or more applicable documents to reflect different thermal measurement requirements. Because environmental conditions, component mounting approaches and device construction techniques and processes will change as technology changes, additional documents will be added to these groups as the needs arise and standards established. As appropriate, each of

The JESD51-1 electrical test method

- **Direct measurement of a single temperature:**
  average temperature, good time resolution
  - **Electrical test method – to measure junction temperature**:
    - Temperature measured by the change of a **temperature sensitive parameter** of the semiconductor (TSP) device (e.g. diode forward voltage, MOSFET threshold voltage)
    - Measures the junction temperature through an electrical signal of the TSP
    - Needs calibration
    - Two test methods: static and dynamic test method
  - **Thermocouples**
    - Large, error due to alternate heat-flow via the thermocouple itself
    - Used typically to measure / monitor environmental conditions
- **Thermal transient measurements are based on the electrical test method**
  - **smart implementation of the JESD51-1 *static test method***
  - **completed with structure function analysis adds extra value: *insight into the details of the heat-flow path***

A few words about the thermal resistance

- Original definition in the JEDEC JESD51-1 document

2. MEASUREMENT BASICS

The thermal resistance of a semiconductor device is generally defined as:

$$R_{JX} = \frac{T_J - T_X}{P_H} \quad (1)$$

where $R_{\theta JX}$ = thermal resistance from device junction to the specific environment (alternative symbol is θ_{JX}) [°C/W]
T_J = device junction temperature in the steady state test condition [°C]
T_X = reference temperature for the specific environment [°C]
P_H = power dissipated in the device [W]

The device junction temperature in the test condition can be determined by:

$$T_J = T_{J0} + \Delta T_J \quad (2)$$

where T_{J0} = initial device junction temperature before heater power is applied [°C]
ΔT_J = change in junction temperature due to heater power application [°C]

The Electrical Test Method (ETM), described herein, makes use of a temperature-sensitive parameter (TSP) to sense the change in temperature of the junction operating area due to the application of electrical power to the device-under-test (DUT). In equation terms,

$$\Delta T_J = K \times \Delta TSP \quad (3)$$

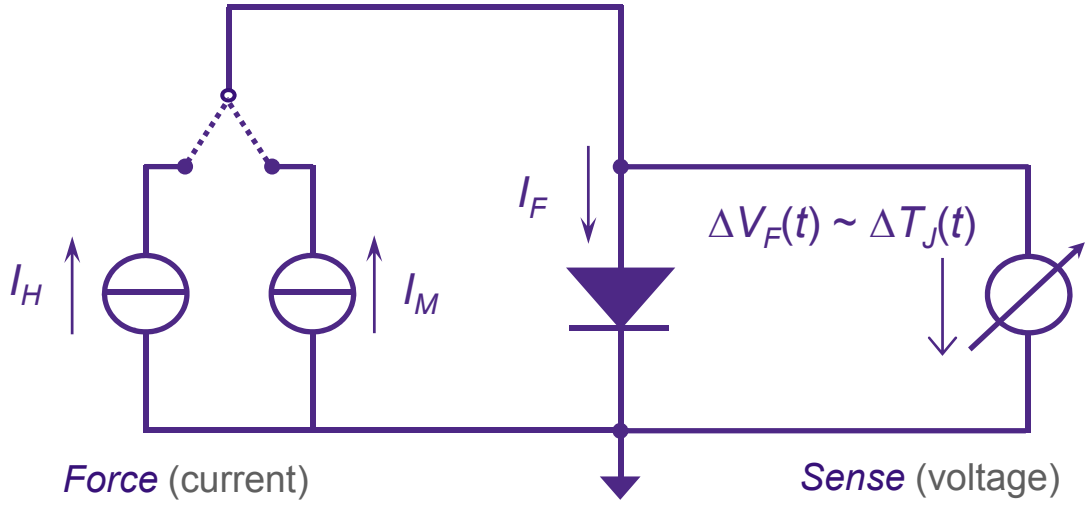
where ΔTSP = change in temperature-sensitive parameter value [mV]
K = constant defining relationship between changes in T_J and TSP [°C/mV]

How do we know $\Delta T_J(t)$?

- PN junctions' forward voltage under forced current condition can be used as a very accurate thermometer
- The change of the forward voltage (TSP – temperature sensitive parameter) should be carefully calibrated against the change of the temperature (see JEDEC JESD51-1 and MIL-STD-750D)
  - In the calibration process the S_{VF} temperature sensitivity of the forward voltage is obtained

$$V_F(I_M, t) = V_{Fi}(I_M) + S_{VF} \cdot [T_J(t) - T_J(0)]$$

S_{VF} = 1/K



- Forward voltage change due to temperature change is measured using a 4 wire setup (Kelvin setup)

The static test method

- According to the JESD51-1 document two test methods are defined: dynamic test method and static test method
- **Static test method or** *continuous measurement*:
  - Switch on heating at the junction
    - Wait for the steady state be reached (when junction is hot)
    - Measure the junction temperature and identify the heating power
  - Switch off the heating
    - Wait for the steady state be reached (when junction is cool)
    - Measure the junction temperature

  Assumption of the standard:
    - At cold steady-state 0 power is applied ➔ junction temperature is equal to the temperature of the ambient (reference environment)

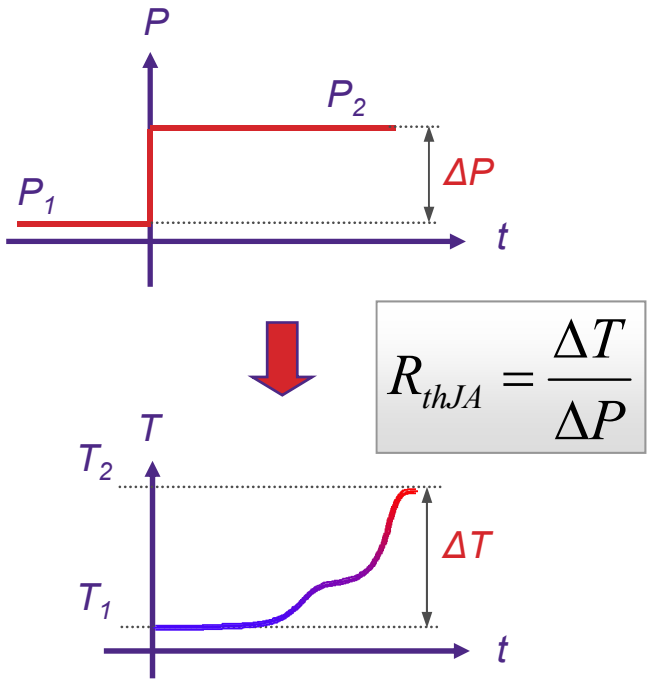
    As we shall see, this assumption is not really needed
- Extension of the basic static test method: **real transients**
  - Measure the actual change of the junction temperature after the power is switched off (or on) continuously, resulting in a real junction temperature transient
  - Completely differential approach in which switching off or on the power is symmetrical
  - Measurement is followed by mathematical post processing resulting in structure functions and other descriptive functions

The principle of the extended static test method

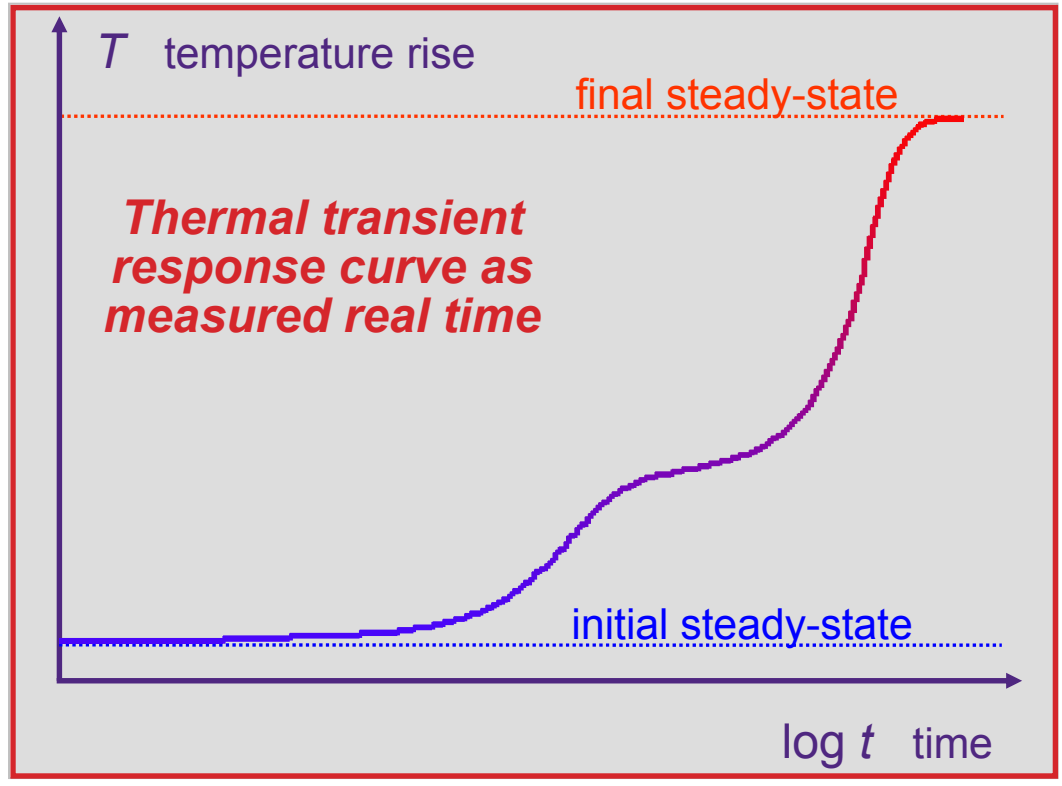
- Due to switching the power, temperature changes:

  Switch the power on (or off) in steady state and wait for the other steady state to occur.

  While waiting for reaching the other steady-state, ***measure (record) the real transient*** *continuously, as it takes place.*



$$R_{thJA} = \frac{\Delta T}{\Delta P}$$



Measurement of $\Delta T_J(t)$ continuously "on-the-fly":

- ***This test method is less problematic:*** the JESD51-1 document does not prescribe detailed procedures to avoid problems
- In the static test method ***only one switching*** takes place:
  - switch ON the power: *capture a heating transient – continuously*
  - switch OFF the power: *capture a cooling transient – continuously*
- After changing the heating power in a step-wise manner ***no further switching takes place***
  - no problems related to t_{MD} selection – no measurement delay is needed

2.2 COOLING TIME CONSIDERATIONS

JESD51-1 document

COOLING TIME considerations are NOT applicable to the Static Mode of testing because the monitoring of the temperature-sensitive parameter occurs on a continuous basis while the heating power is applied to the DUT.

  - the only concern is the possible electrical transient at t=0+

Essentials of the JESD51-1 electrical test method

How do we know $\Delta T_J(t)$?

- PN junctions' forward voltage under forced current condition can be used as a very accurate thermometer
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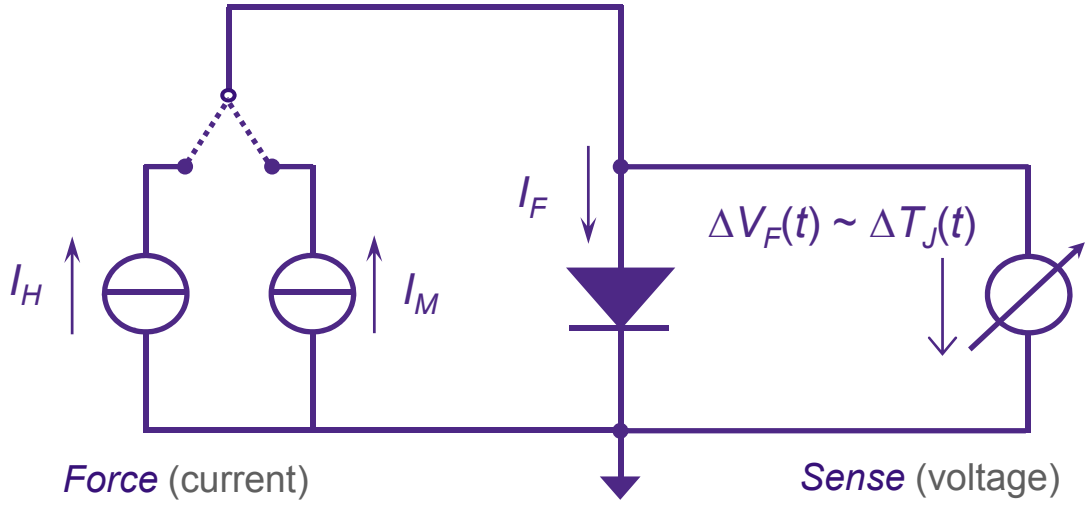
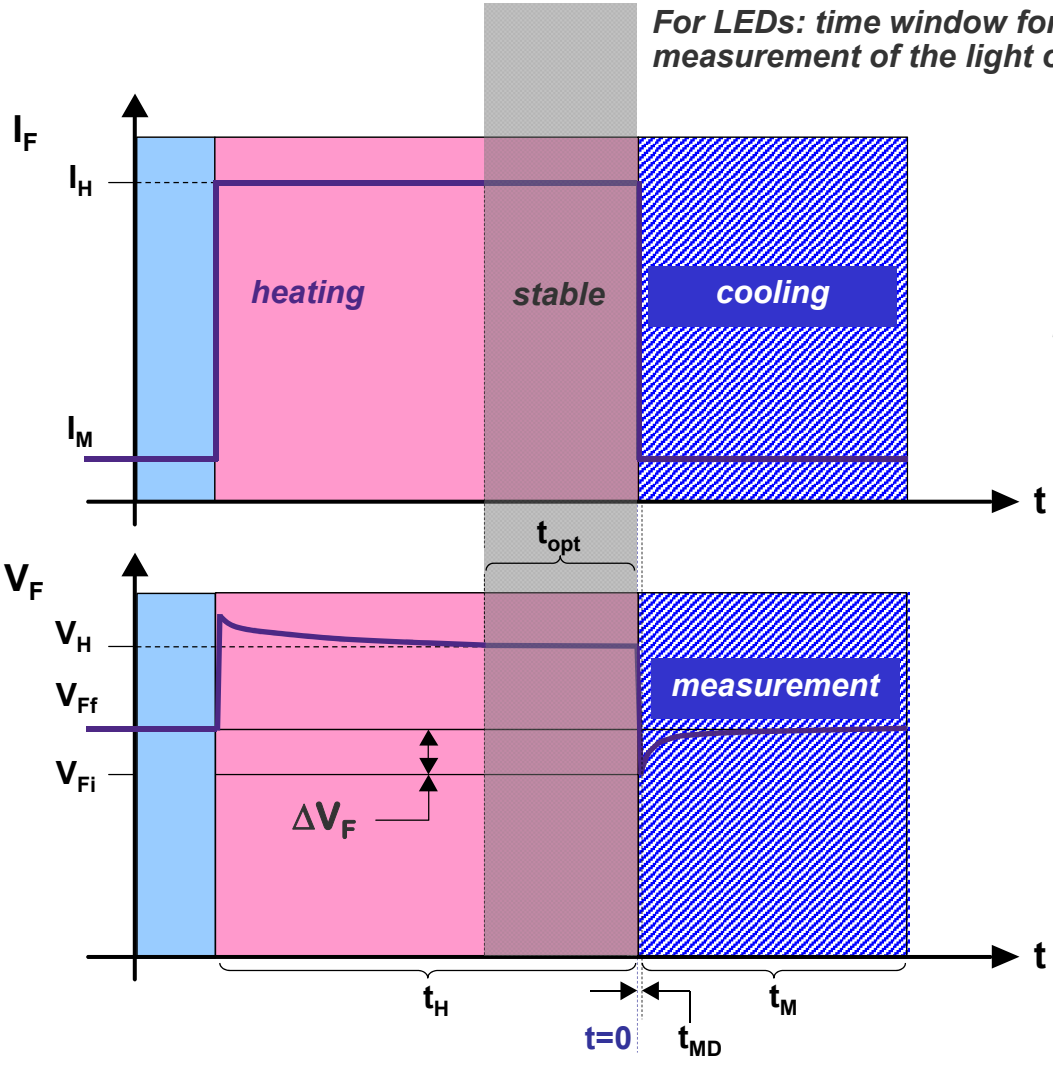
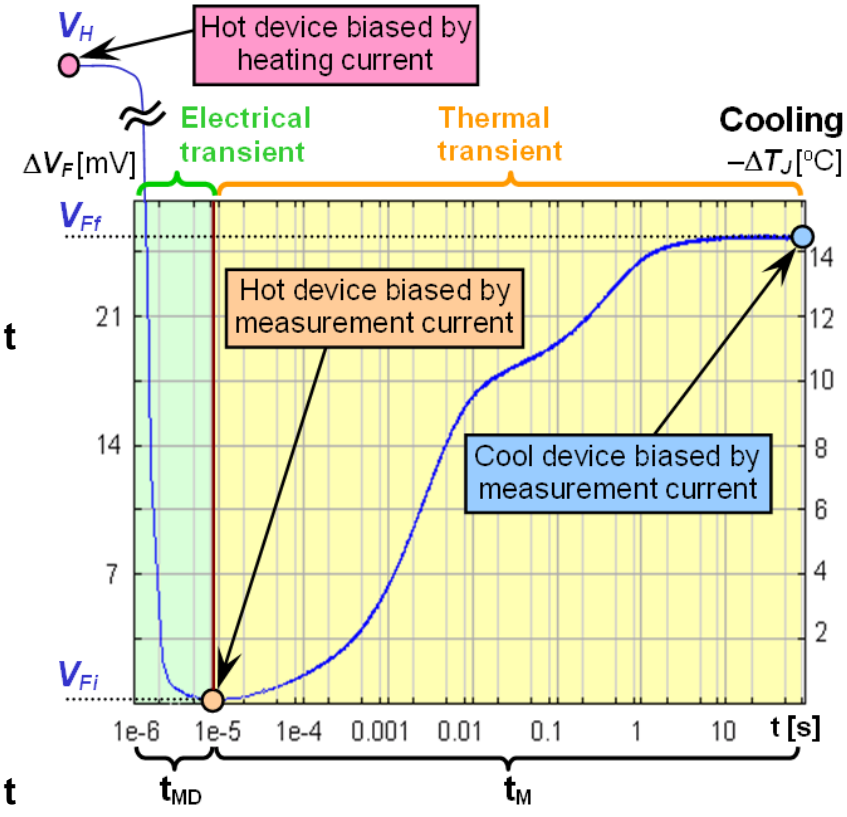


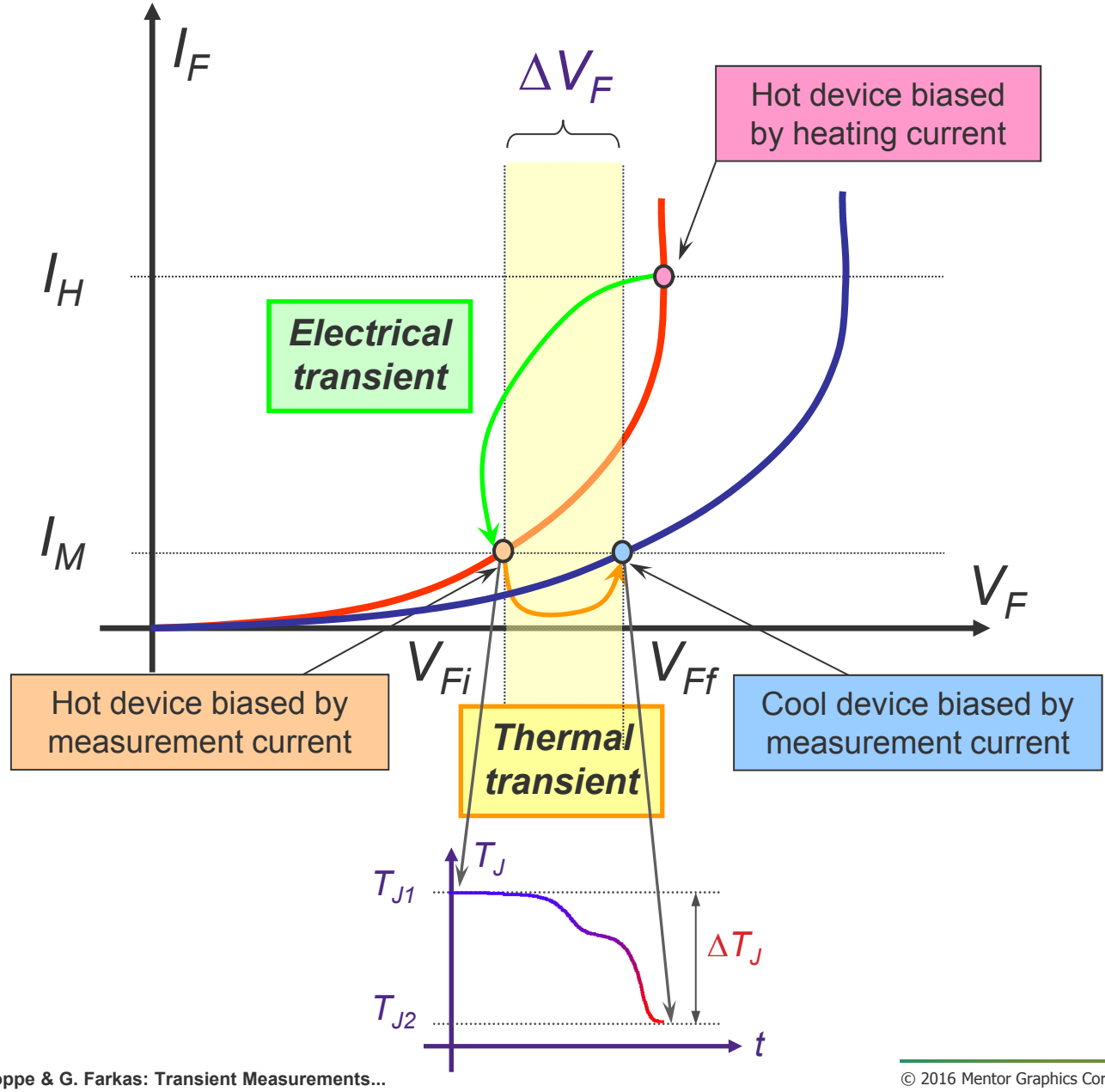
- Forward voltage change due to temperature change is measured using a 4 wire setup (Kelvin setup)

The measurement waveforms



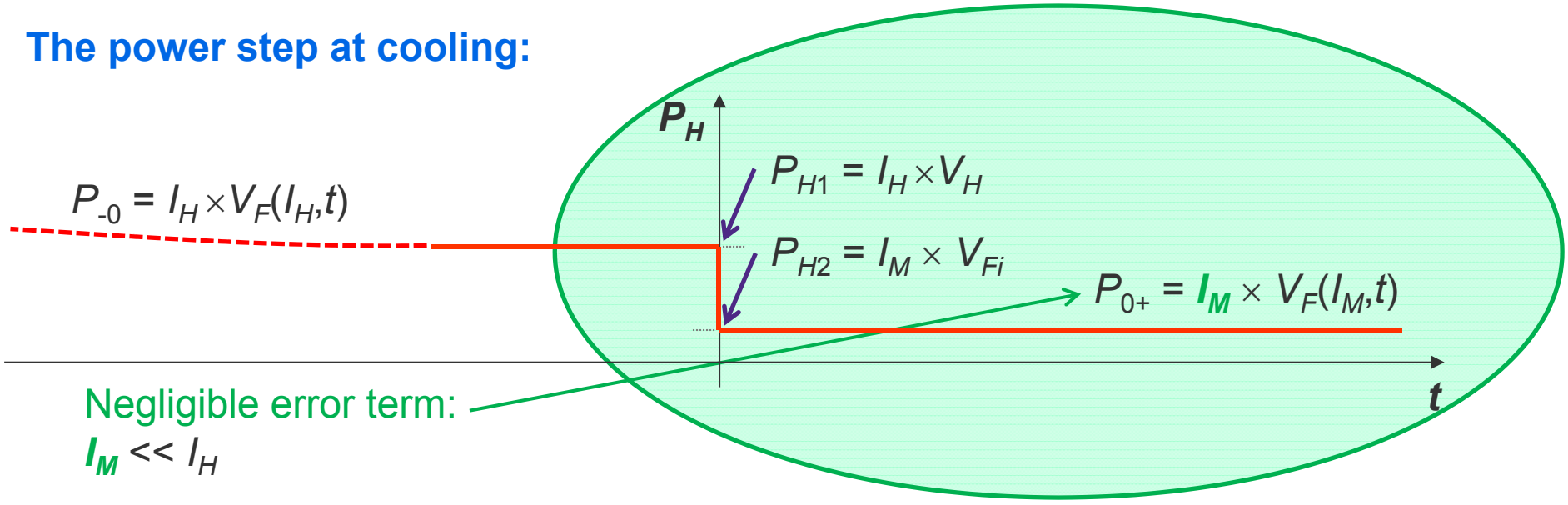


The transient processes in the I-V characteristic:



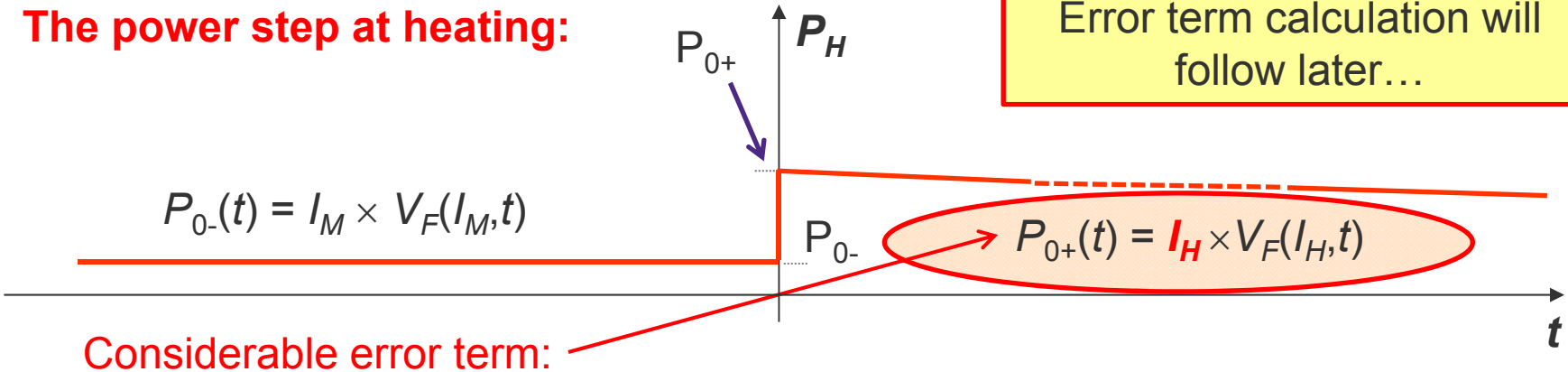
Heating vs. cooling?

The power step at cooling:



Negligible error term:
$I_M << I_H$

The power step at heating:



Considerable error term:
$I_H >> I_M$

Error term calculation will follow later…

A few words about thermal resistance again

- Original definition in the JEDEC JESD51-1 document

2. MEASUREMENT BASICS

The thermal resistance of a semiconductor device is generally defined as:

$$R_{JX} = \frac{T_J - T_x}{P_H}$$

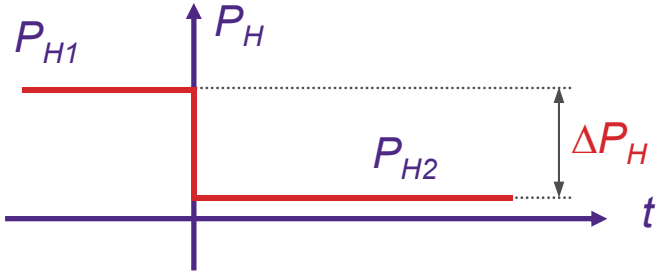
where $R_{\theta JX}$ = thermal resistance from device junction to the specific environment (alternative symbol is θ_{JX}) [°C/W]
T_J = device junction temperature in the steady state test condition [°C]
T_X = reference temperature for the specific environment [°C]
P_H = power dissipated in the device [W]

- Rearrange the equation

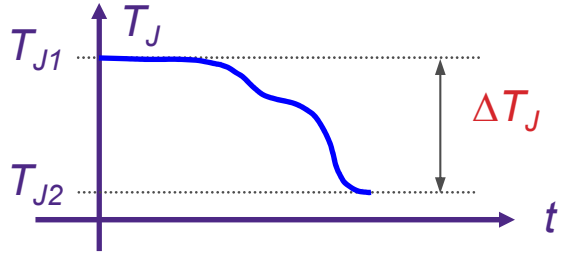
$$T_J = R_{th\ J\text{-}X} \cdot P_H + T_X$$

Differential formulation of the thermal resistance

Instead of spatial difference (temperature values at junction and reference point) temporal difference of the junction temperature can be used



$$R_{thJ-X} = \frac{\Delta T_J(\infty)}{\Delta P_H}$$



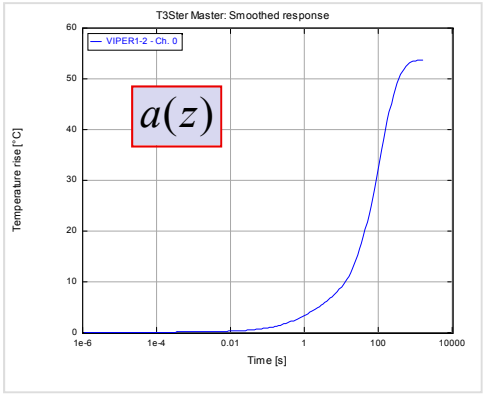
Differential formulation of the thermal resistance

- Instead of spatial difference, we can calculate with a ***temporal difference*** of the junction temperature (temp. transient)

- The TSP change is also measured in a differential mode
  - Traceability and calibration problems reduced to minimum, see later
  - In our implementation the complete calibration curve can also be used instead of a single K-factor value

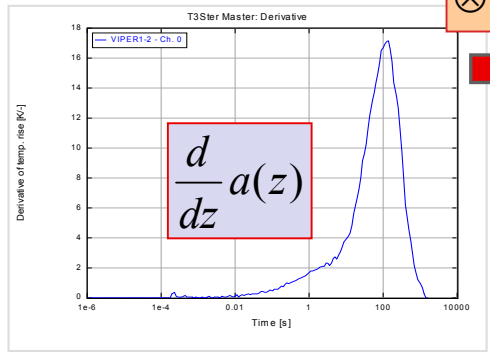
- No need for thermocouple based measurements if the thermal metric of interest is in the main heat-flow path (see: R_{thJC})

Converting Z_{th} curves to *structure functions*



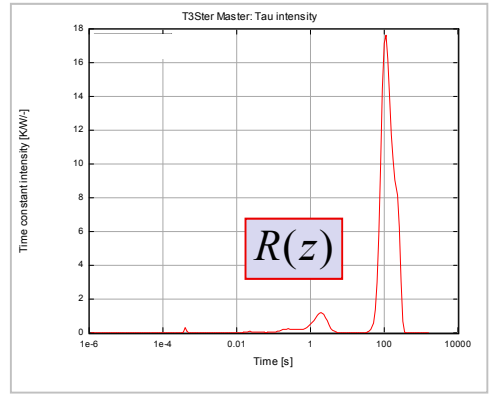
Measured thermal impedance curve

$\frac{d}{dz}$ Numerical derivation



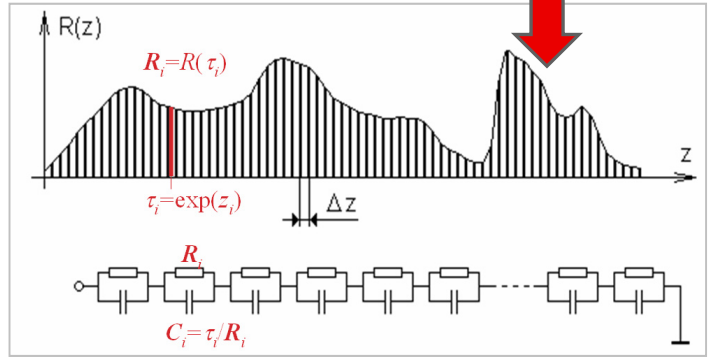
Derivative of the thermal impedance curve

$\otimes^{-1} w_z(z)$ Numerical deconvolution

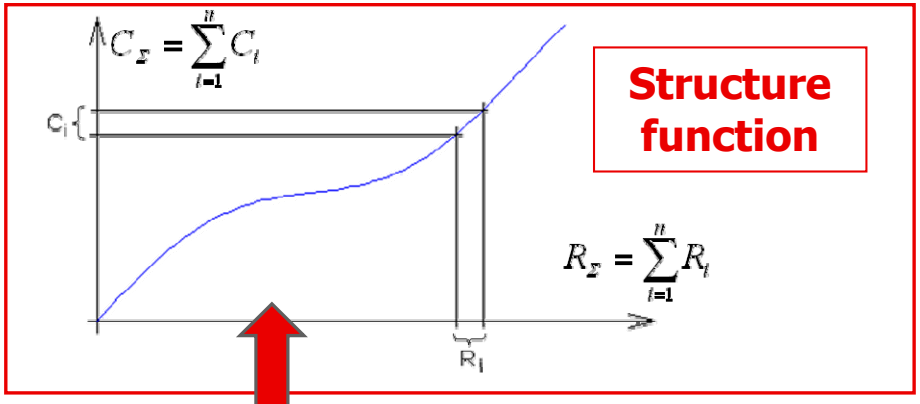


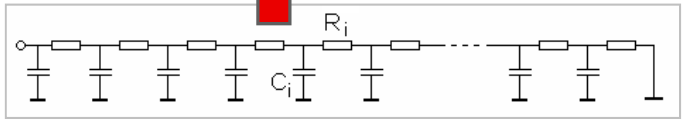
Time-constant spectrum

Discretization



Foster model of the impedance



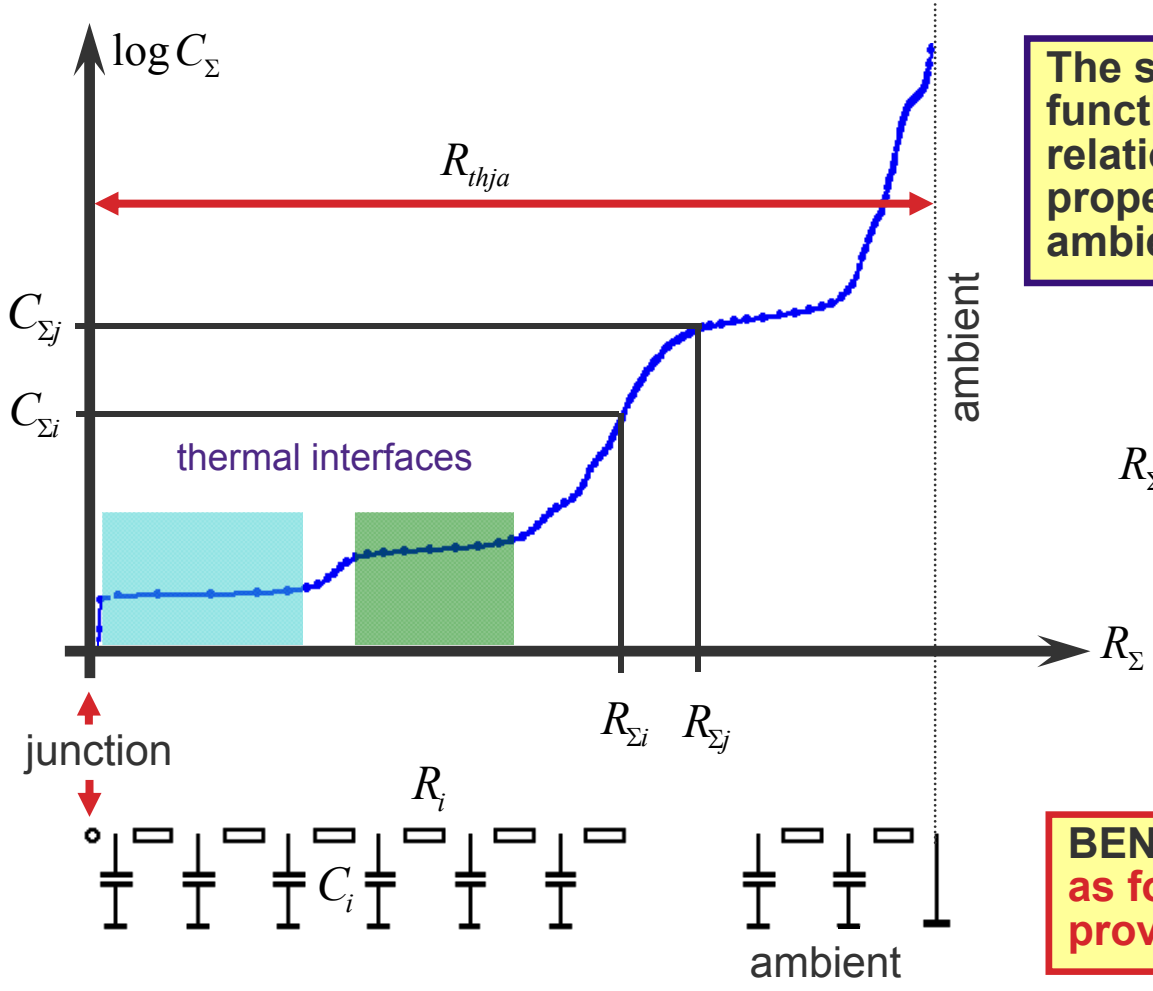


Cauer model of the impedance

Transformation

The Structure Function

The *structure function* is the ***graphical representation*** of the ***network model of the thermal impedance*** of the junction-to-ambient heat-flow path.



The shape of the structure function is in a one-to-one relationship with the properties of the junction-to-ambient heat-flow path.

$$R_{\Sigma n} = \sum_{i=1}^{n} R_i \qquad C_{\Sigma n} = \sum_{i=1}^{n} C_i$$

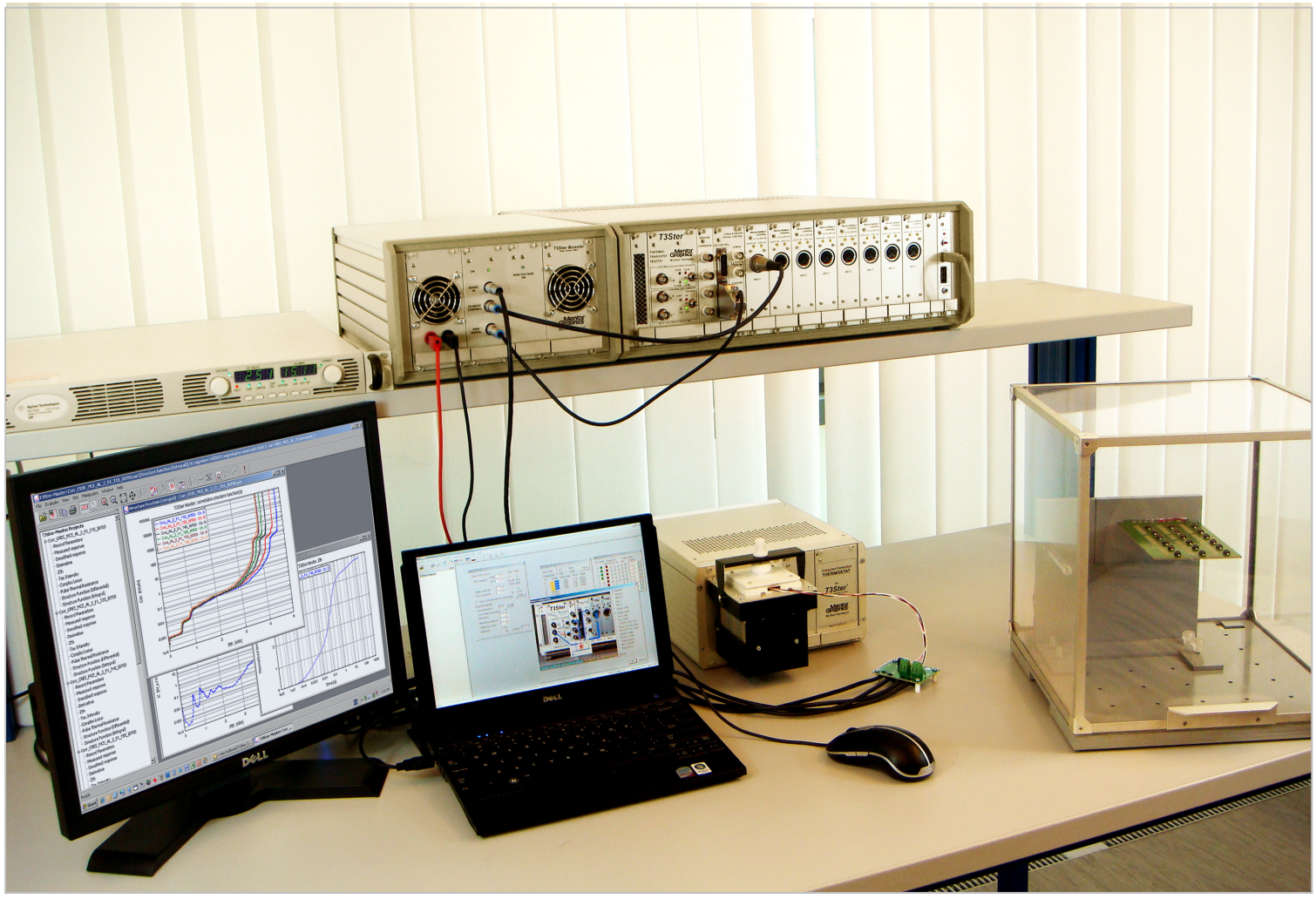
BENEFIT: same testing time as for steady-state, but provides much details…

The *structure function* illustrates the **way how heat flows though a package.**

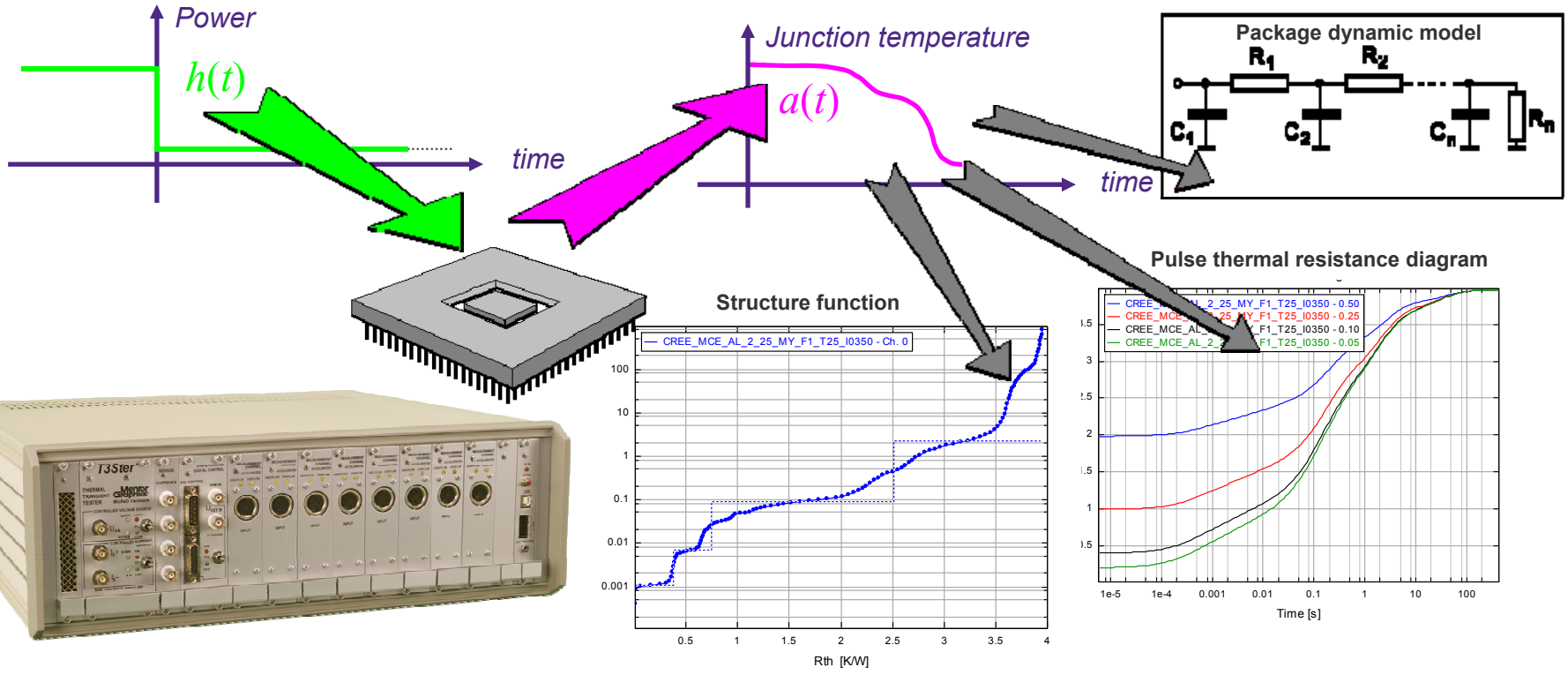
Mentor Graphics MicReD implementation: T3Ster

- The JEDEC JESD51-1 static test method is implemented by the **T3Ster** equipment (thermal transient tester) and its measurement software
  - real-time measurement of actual junction temperature transients either in heating mode or in cooling mode
    - for diodes cooling mode is recommended (since higher accuracy available this way)
    - for transistors, thermal test dies with separate heaters and sensors both heating and cooling modes are recommended
  - K-factor calibration is provided
- Measured transients are post-processed by the **T3Ster Master** software, providing
  - structure functions and
  - other alternate representations of the measured thermal impedance such as
    - complex loci
    - time-constant spectra
    - pulsed thermal resistance diagrams
    - dynamic compact thermal network models

Mentor Graphics MicReD implementation: T3Ster



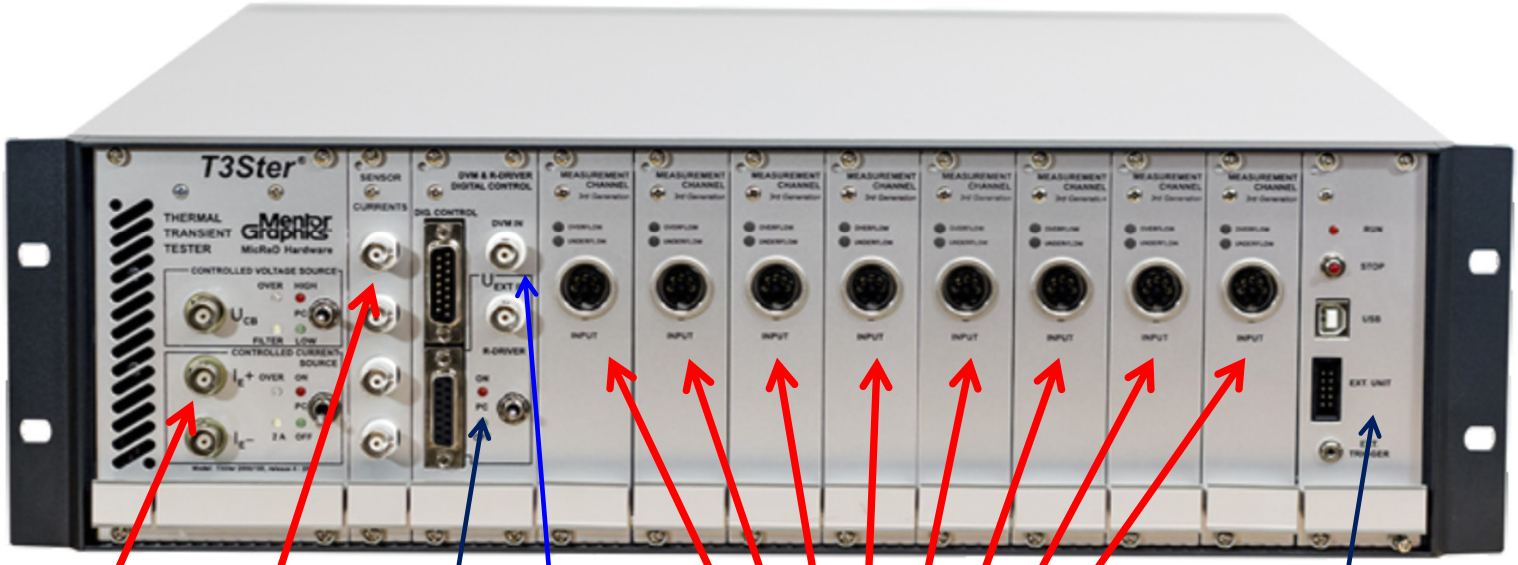
Summary of thermal transient testing using T3Ster



- The $h(t)$ step-wise change in heating is applied at the junction (abrupt switching)
- The $a(t)$ temperature response at the junction is being measured (unit-step response function) while linearity is assumed
- All available information is extracted from $a(t)$ using sophisticated mathematical procedures
  - structure function, derivative of structure function
  - compact dynamic thermal models
  - pulsed thermal resistance / complex locus (frequency domain representation)

Some basics of the equipment used

- Mentor Graphics MicReD T3Ster



Heating current source

Measuring current sources

switch for external I_H source

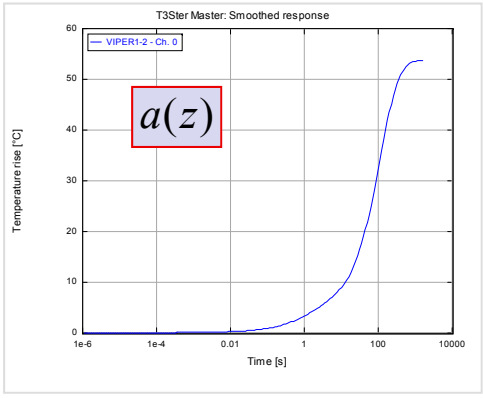
DVM unit

Measuring channels

external interfaces

The structure functions

How Do We Get Them in the *T3Ster* software?



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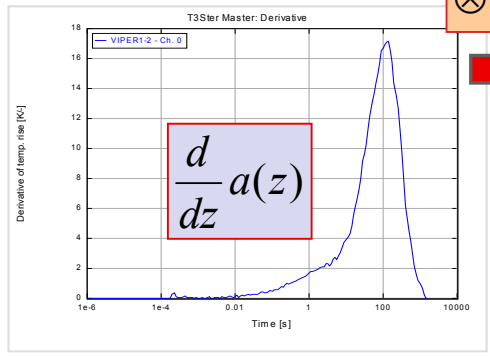

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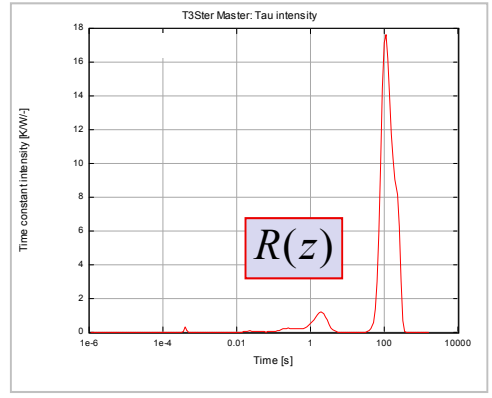
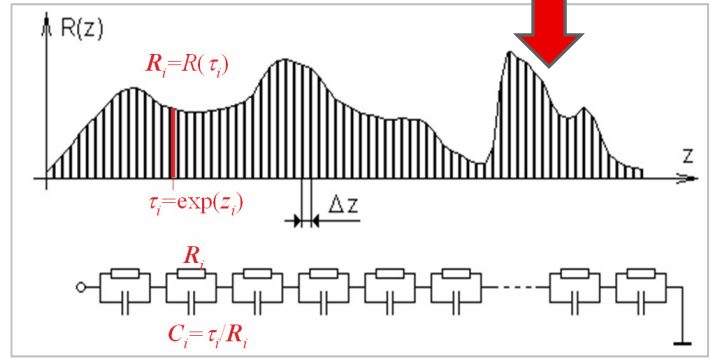


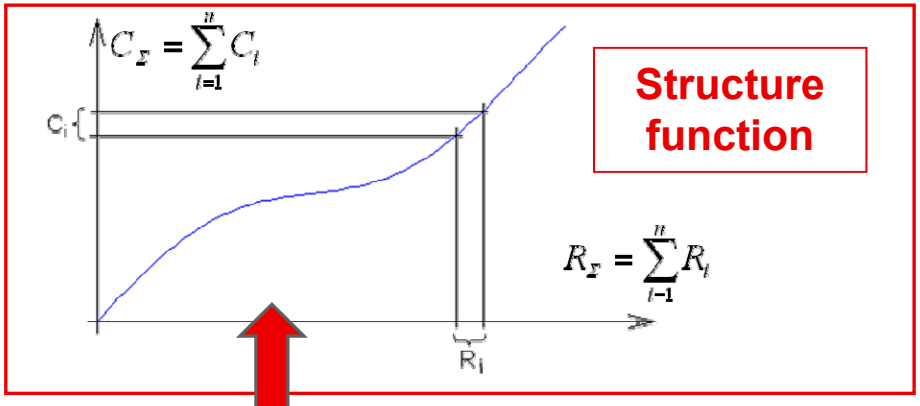
Time-constant spectrum

Discretization



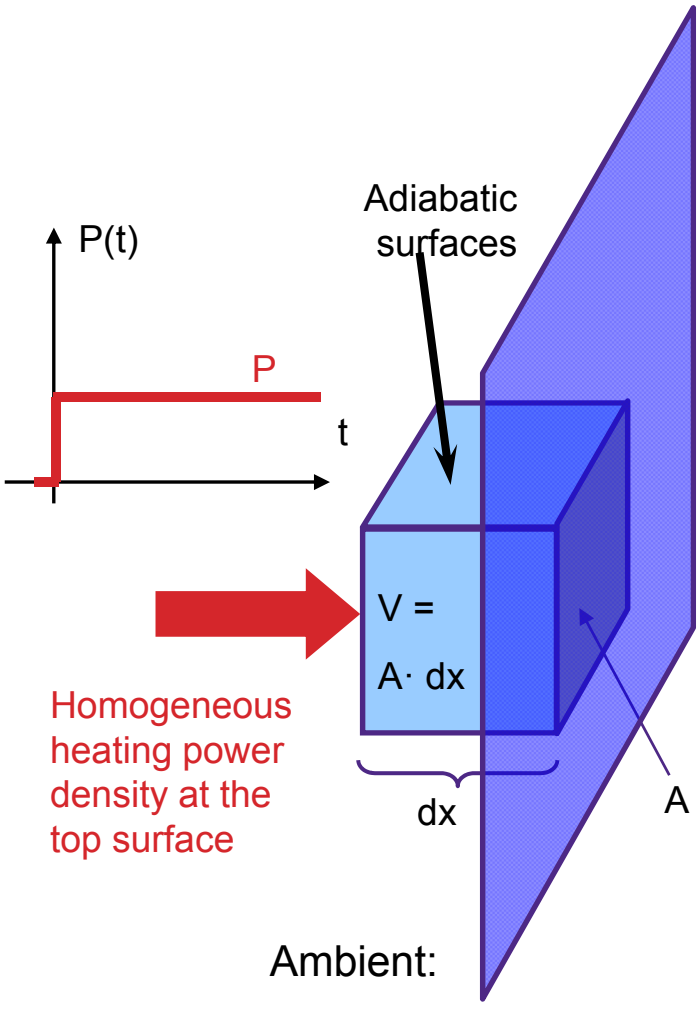
Foster model of the impedance

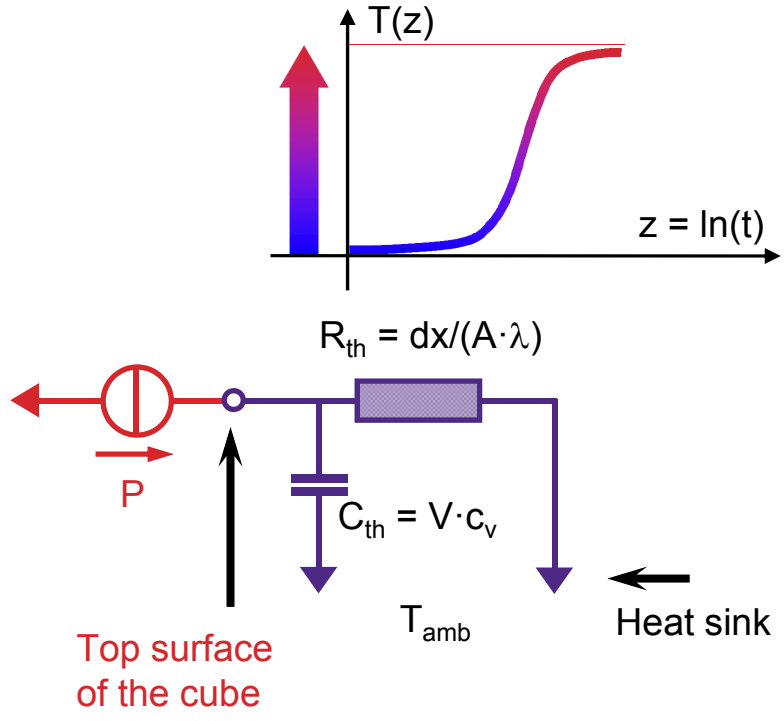
Transformation



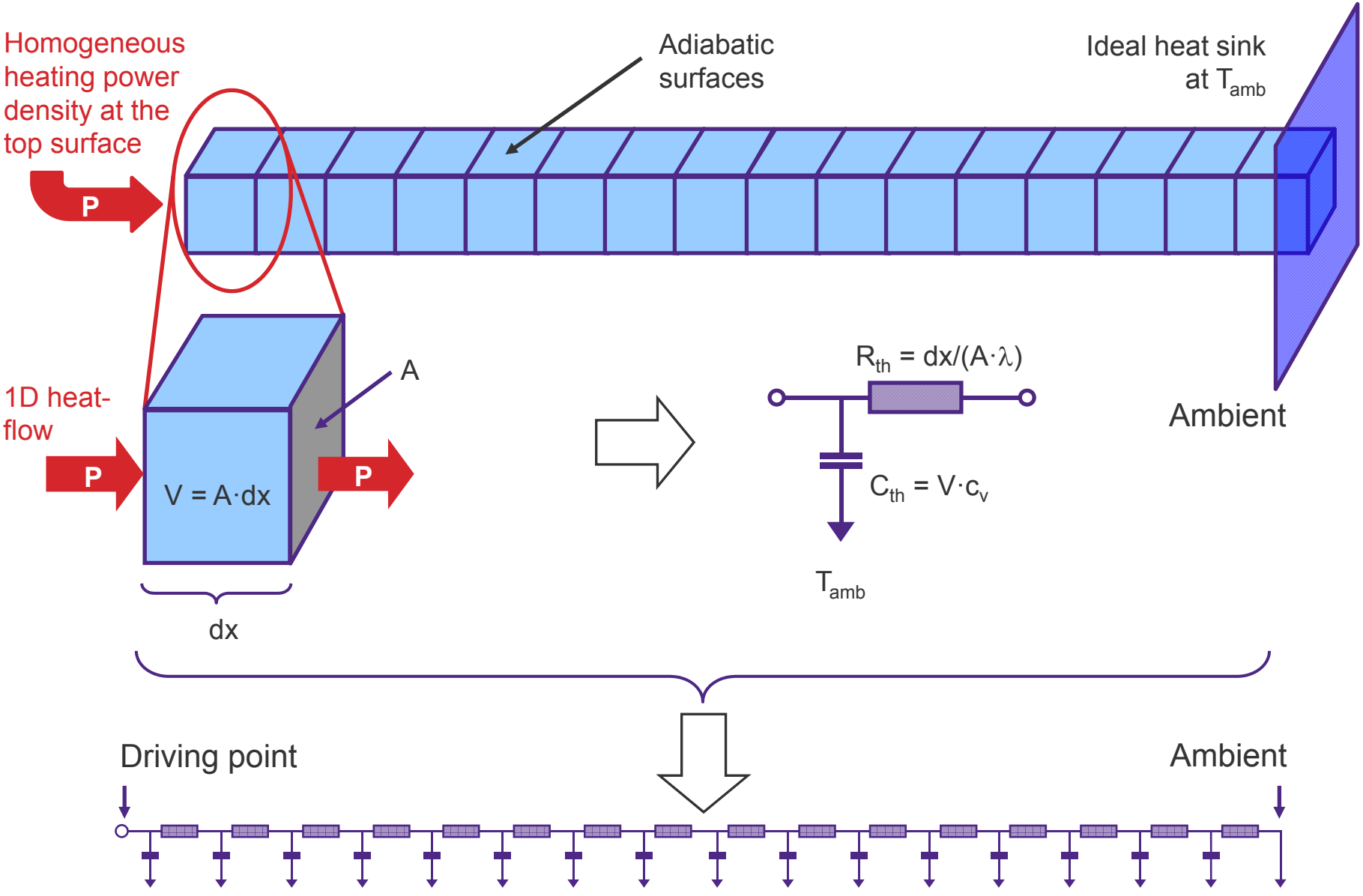
Cauer model of the impedance

Introduction to the structure functions





Introduction to the structure functions



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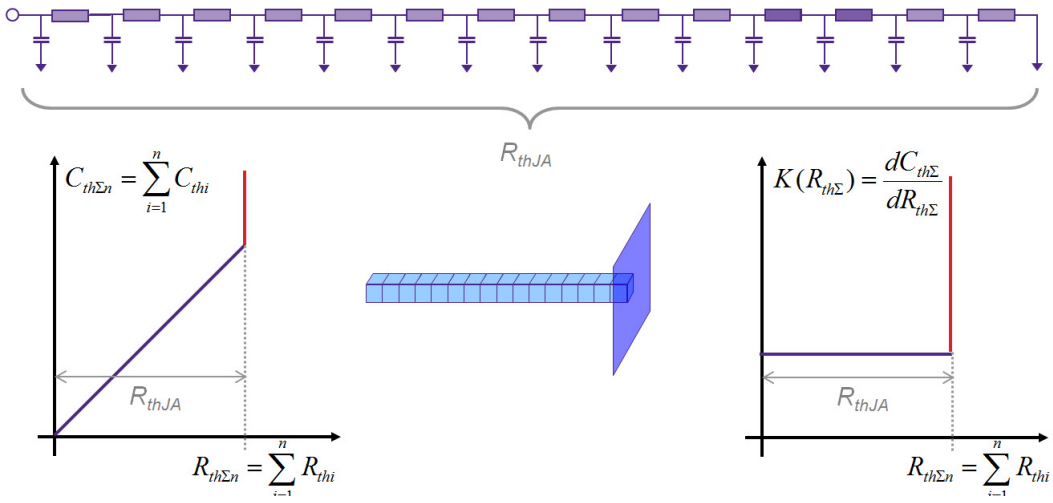
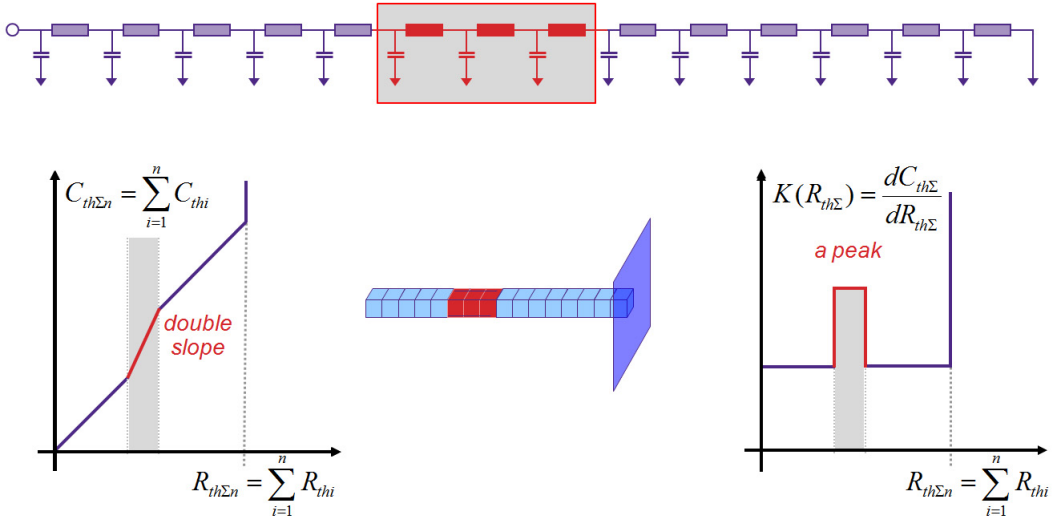


Structure function **Derivative of structure function**

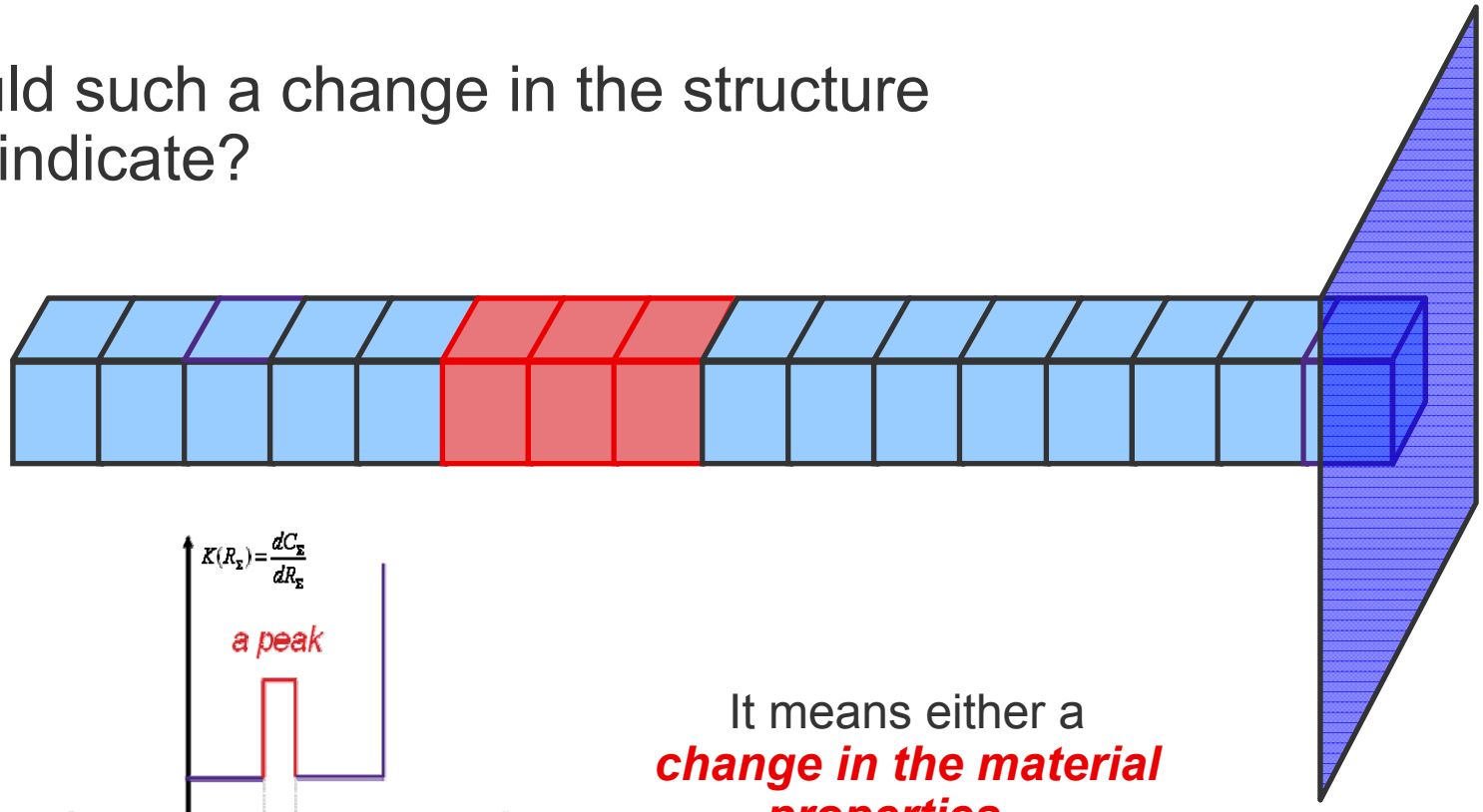


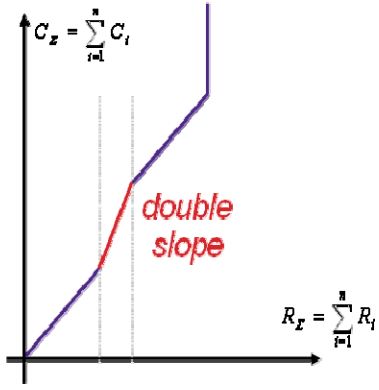
Structure function **Derivative of structure function**

Structural or material property changes are clearly indicated both by the cumulative and the differential structure functions

Introduction to the structure functions

What would such a change in the structure functions indicate?

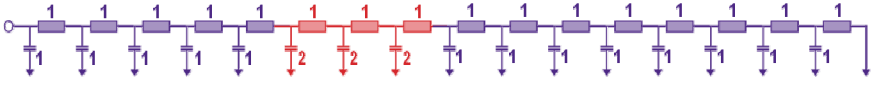




Structure function

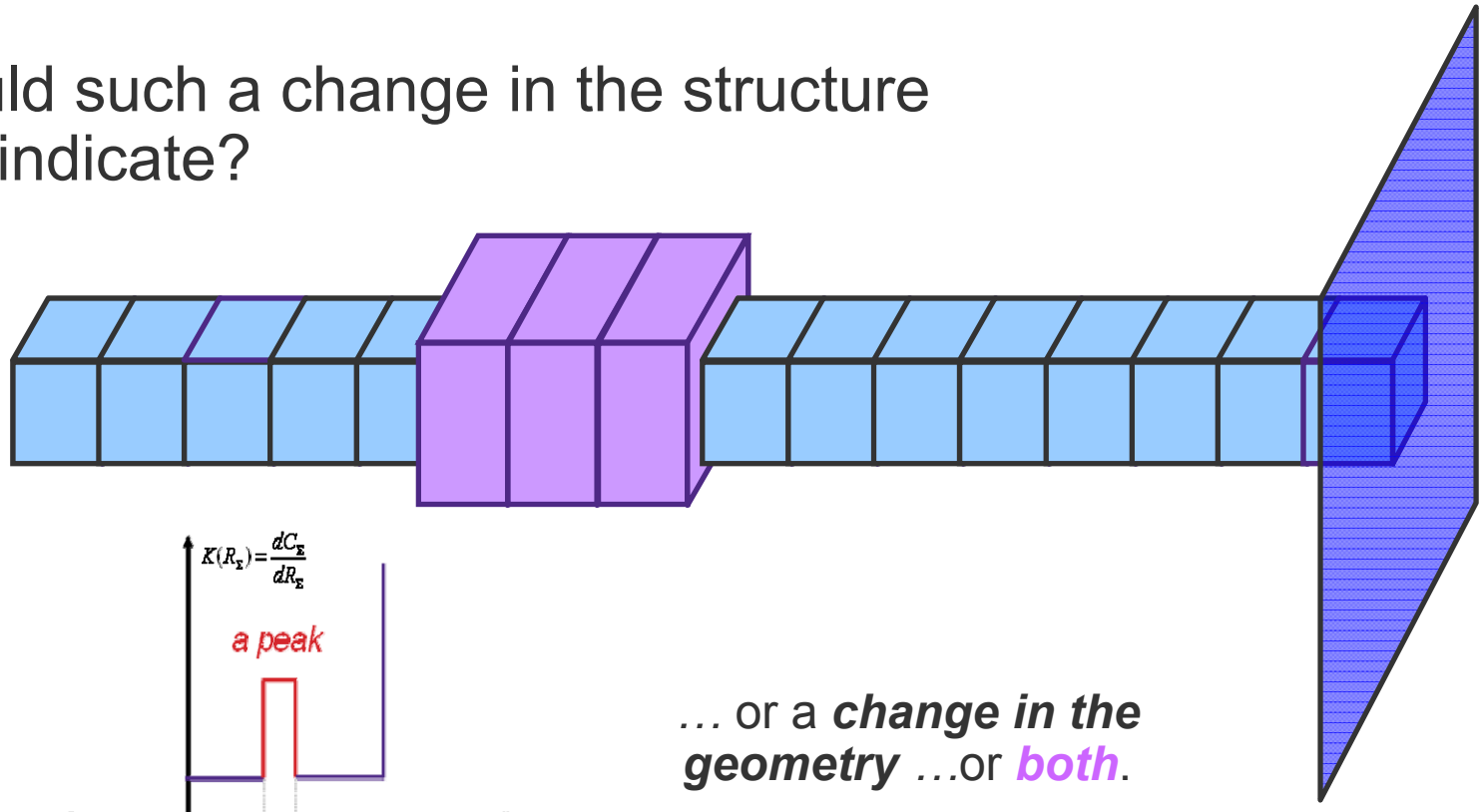
Derivative of structure function

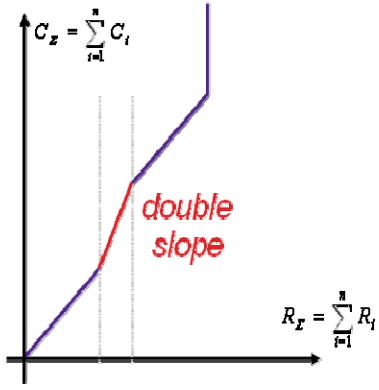
It means either a ***change in the material properties…***



Introduction to the structure functions

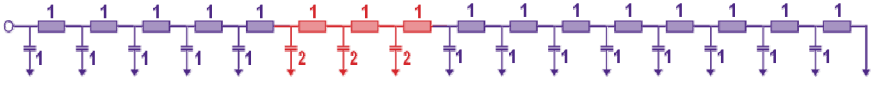
What would such a change in the structure functions indicate?





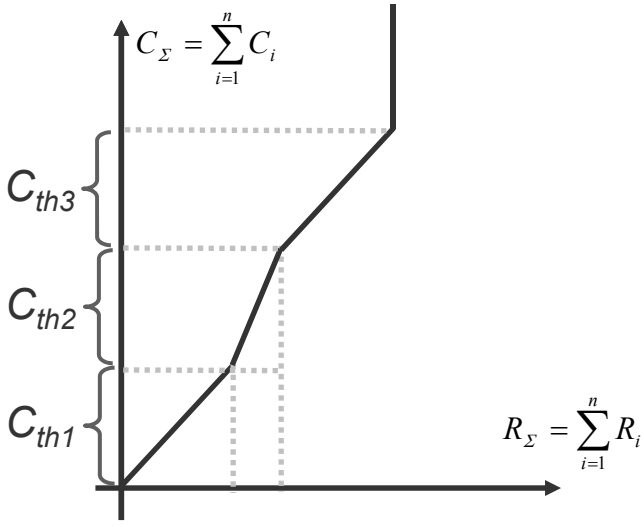
Structure function **Derivative of structure function**

… or a ***change in the geometry*** …or ***both***.



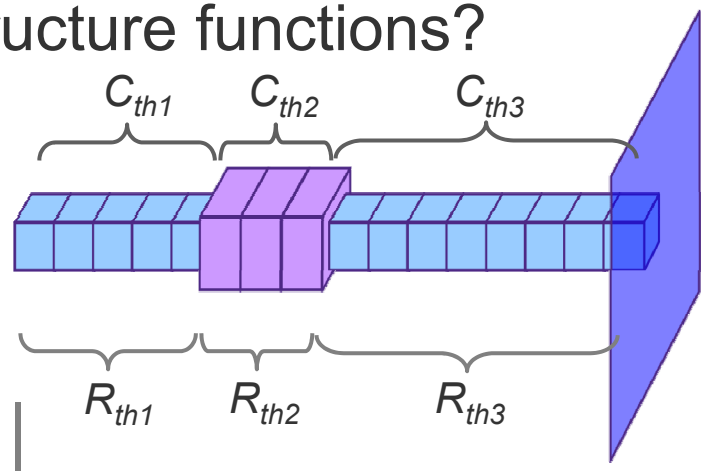
Introduction to the structure functions

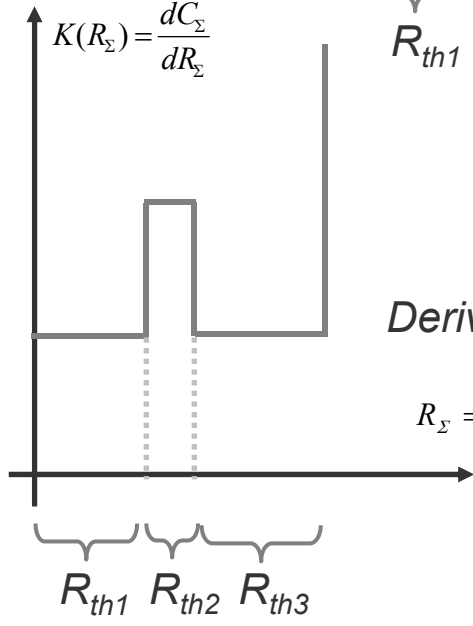
What values can we read from the structure functions?



Structure function

Thermal capacitance values can be read





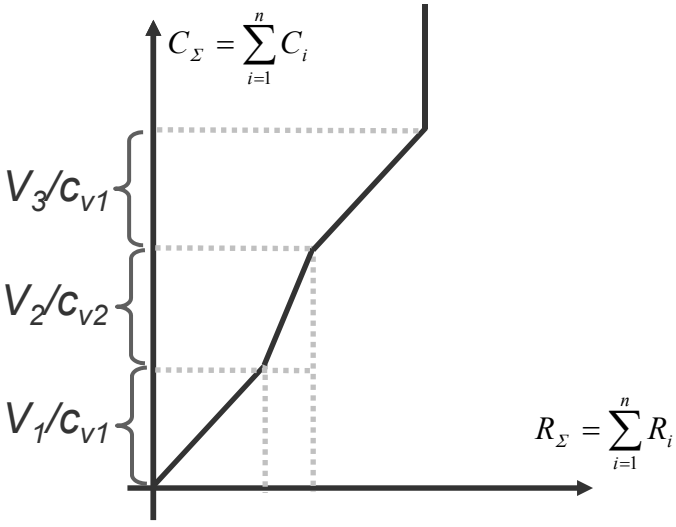
Derivative of the structure function

$R_\Sigma = \sum_{i=1}^{n} R_i$

Partial thermal resistance values can be read

Introduction to the structure functions

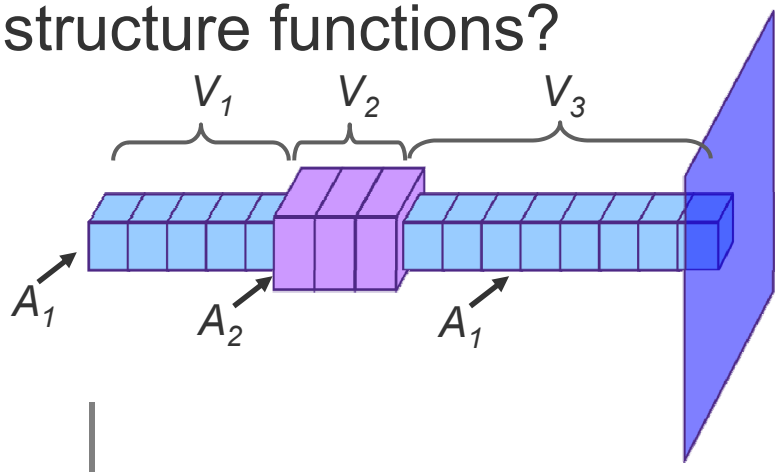
What values can we read from the structure functions?

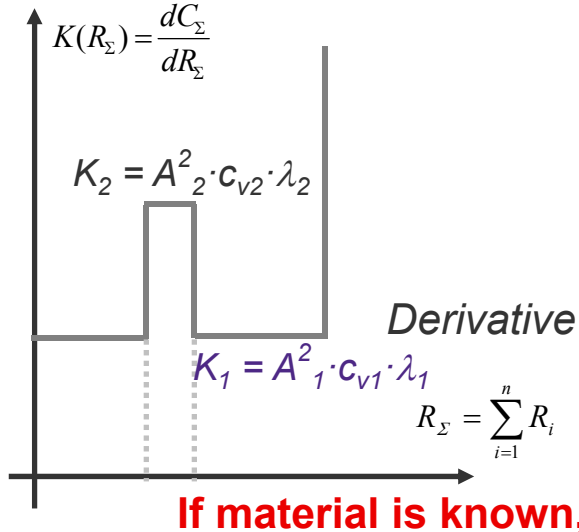


Structure function

If material is known, volume can be identified.

If volume is known, volumetric thermal capacitance can be identified.





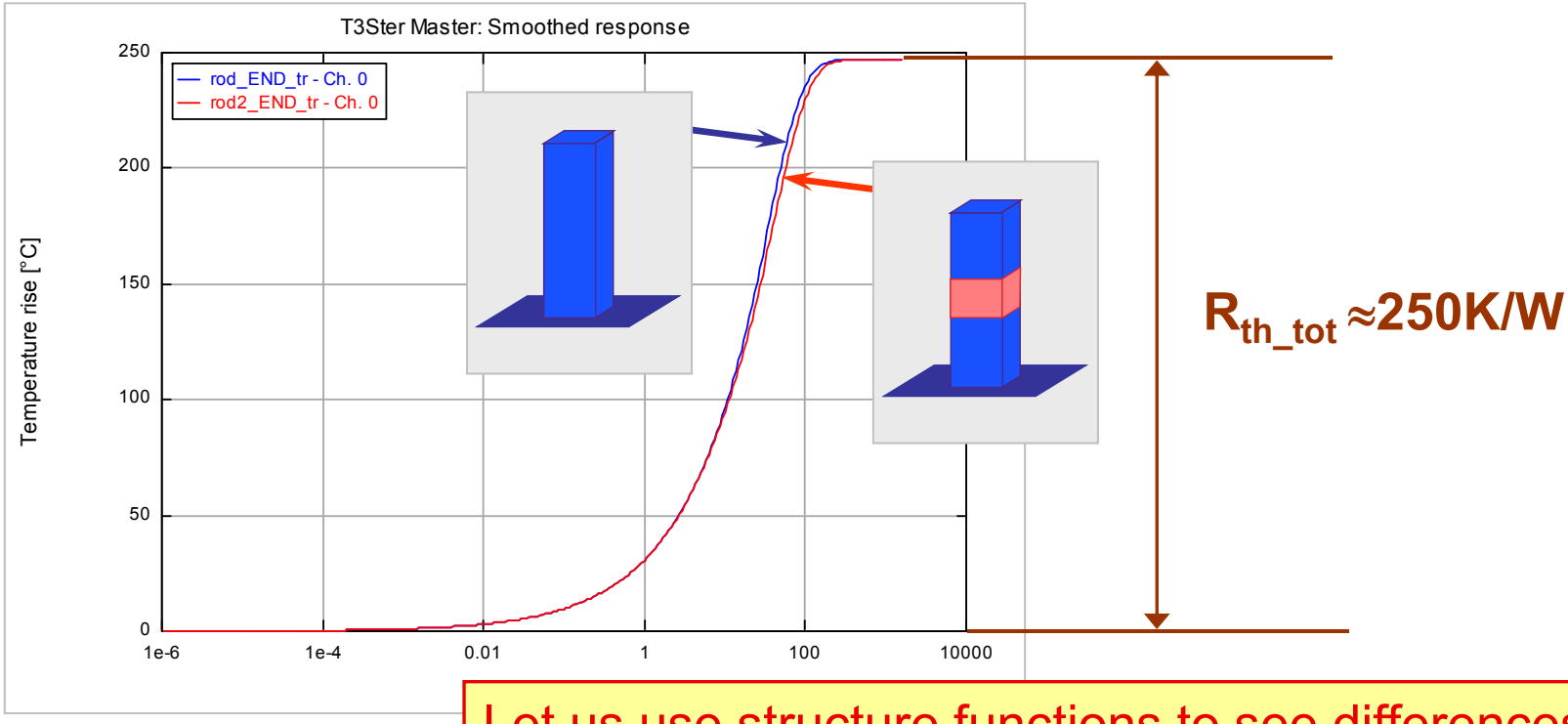
Derivative of the structure function

If material is known, cross-sectional area can be identified.

If cross-sectional area is known, material parameters ($c_v \cdot \lambda$) can be identified.

Simulation Experiment for Rods

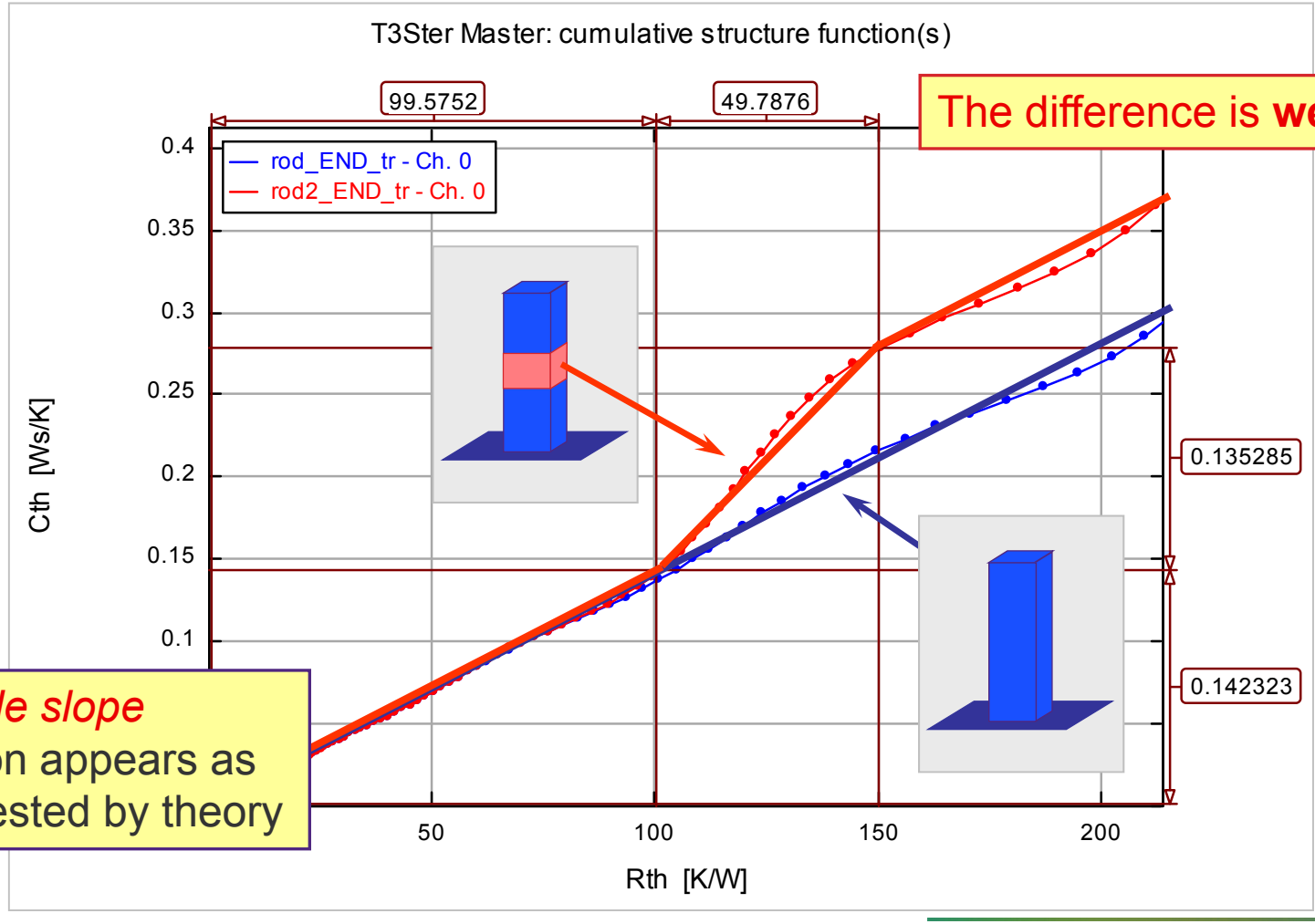
- A Cu rod of 1x1mm^2 cross-sectional area and 100mm length was simulated (λ=402 W/mK, C_v=3.4e6W/m^{3}K) $\Rightarrow$ $R_{th\_tot} \approx 250$ K/W
- **Change applied:** 40mm normal Cu, 20mm with double C_v value, 40mm normal Cu



Let us use structure functions to see differences!

Simulation Experiment for Rods

- The same results in structure functions:

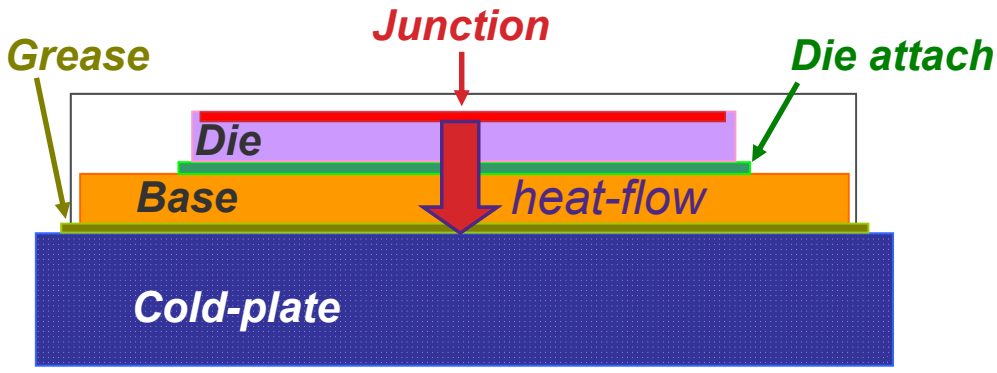


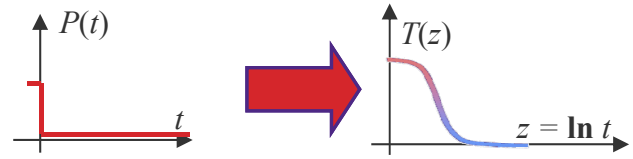
The difference is **well seen**

Double slope section appears as suggested by theory

Structural / network model of the heat-flow path

The Structure Function

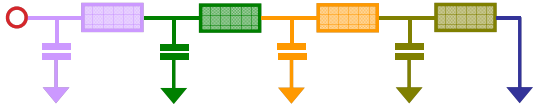


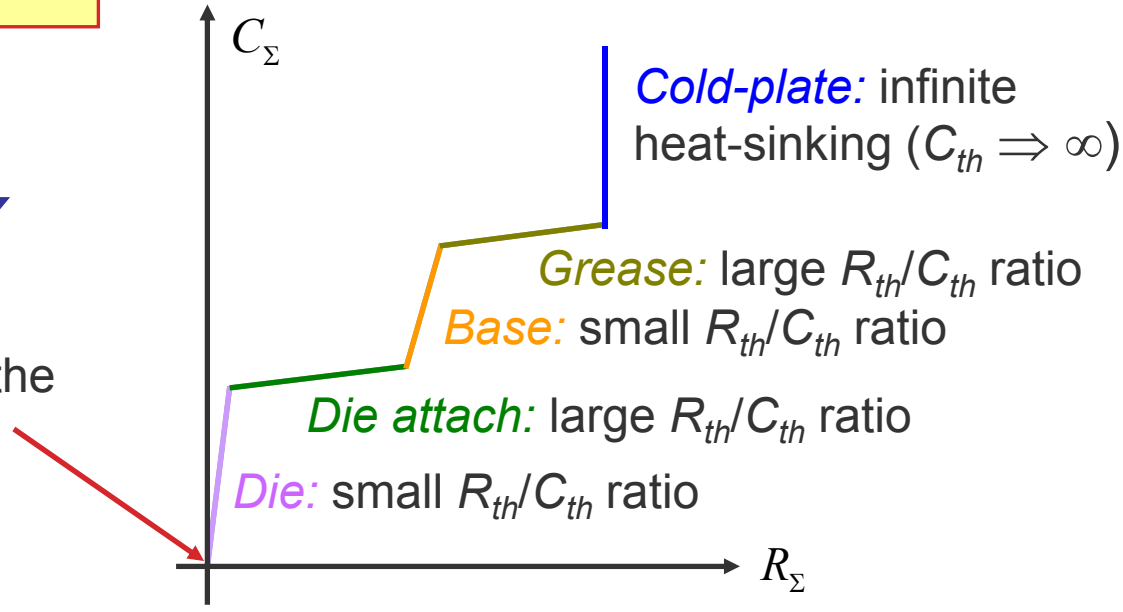


*We measure the **thermal transient at the junction**...*

*...and we convert it into the **cumulative structure function and a compact model:***

Allows structural analysis and modeling…



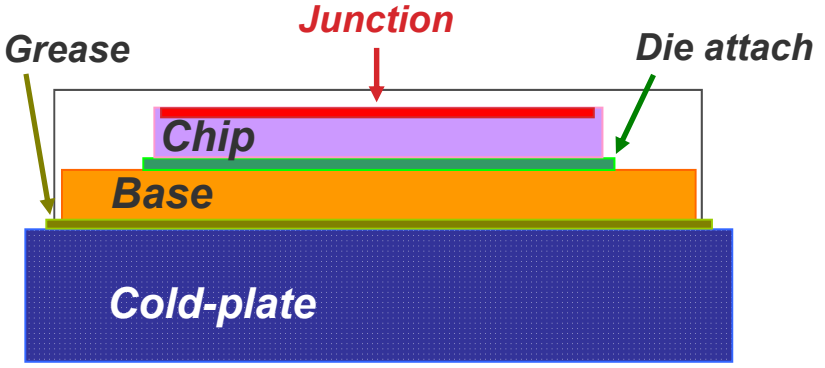


Junction: is always in the origin

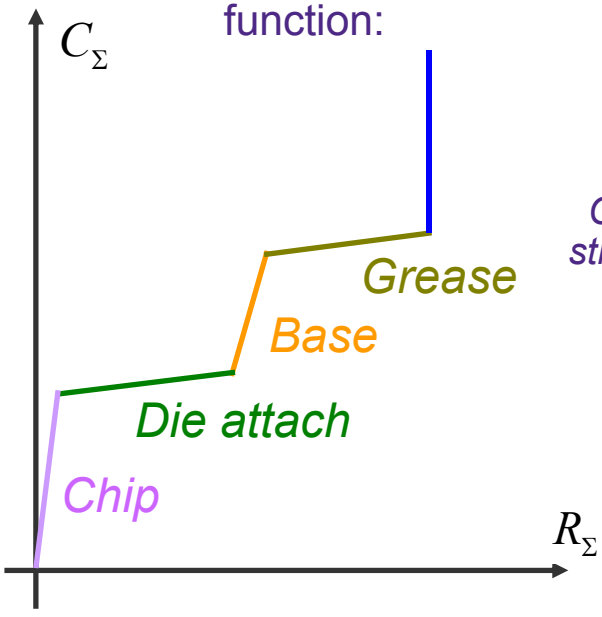
Application in QA (failure analysis)

The Structure Function

Reference device with good DA

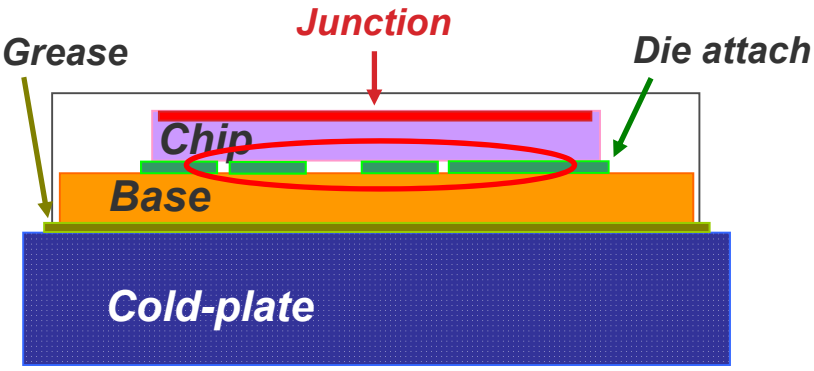


Identify its structure function:

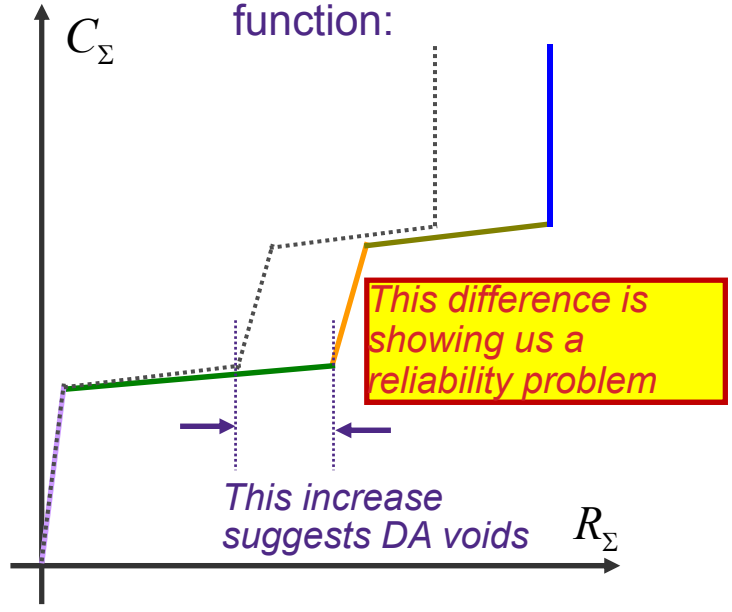


Copy the reference structure function into this plot

Unknown device with suspected DA voids



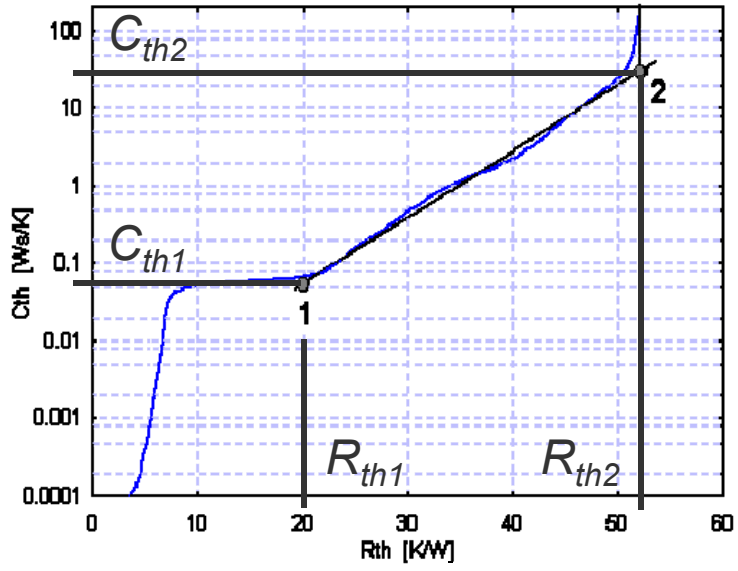
Identify its structure function:



Features of Structure Functions

- For certain types of 1D spreading, analytical formulae can be given
- For "ideal" cases structure functions can be given even by analytical formulae
  - for a rod: $C_\Sigma = const \cdot R_\Sigma$
  - for radial spreading in a disc of w thickness and λ thermal conductivity:

$$\lambda w = \frac{1}{4\pi} \frac{\ln(C_{th2} / C_{th1})}{R_{th2} - R_{th1}}$$



How to select measurement current?
TSP calibration

How to select the I_M measurement current?

- Guidelines in the JEDEC JESD51-1 document basically apply to the **"dynamic" test method**
  - large enough to obtain reliable forward voltage reading (avoiding e.g. surface leakage effects)
  - small enough to avoid possible self-heating effect
    - Large difference between I_H and I_M currents allows easier ΔV_F reading with less accurate test equipment – not an issue for Mentor Graphics MicReD T3Ster equipment
    - Self-heating is not an issue in Mentor Graphics MicReD's differential approach

temperature dependent variability between diodes of the same construction and size) the current is rarely chosen below 100 µA and is usually 1 mA. The upper limit on I_M is determined by self-heating effects, which in turn are a function of the diode geometry.

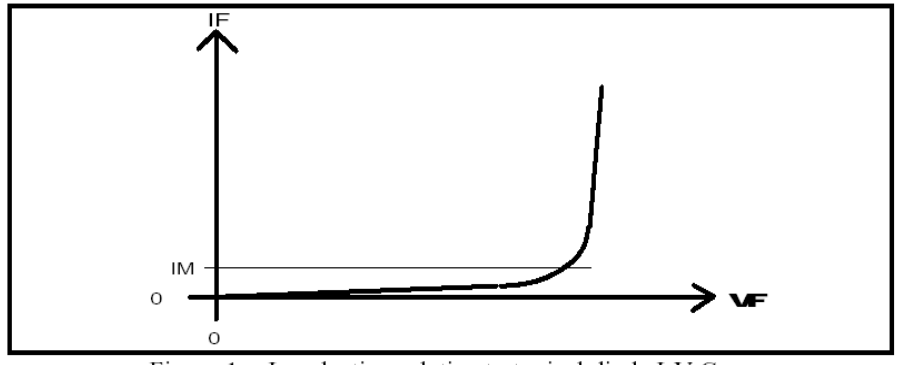
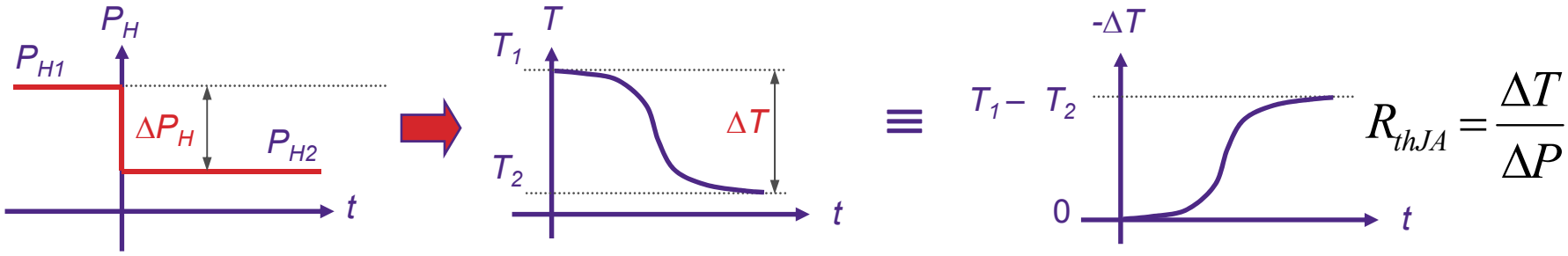


Figure 1. - I_M selection relative to typical diode I-V Curve

The measurement current (sensor current) must be chosen such that we remain in the "knee" of the diode characteristic.

How to select the I_M measurement current?

- Recall the "static" test method



$$\Delta P_H(t+) = (I_H - I_M) \cdot V_{F0} + I_M \cdot \Delta V_F(t+)$$

Error < 1% ⇒ negligible

I_M=100 mA **I_H=500 mA**

V_{F0}=800 mV ΔT=50°C K=0.5 °C/mV ⇒ ΔV_F=0.5 · 50=25 mV

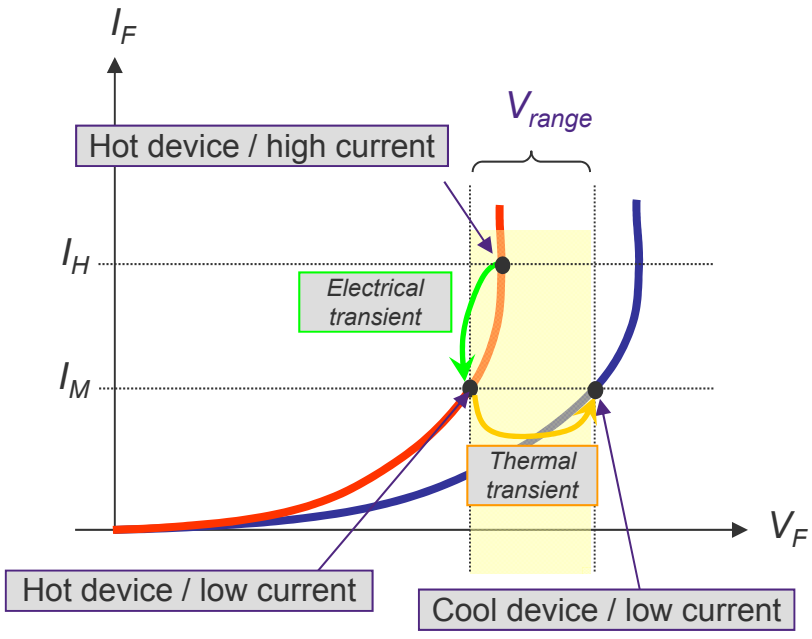
ΔP_H = (0.5-0.1)·0.8 W= **320 mW** $I_M \cdot \Delta V_F$ = 0.1·0.025 W = **2.5 mW**

- Self-heating due to I_M is a myth; power error term caused by 100 mA current is below 1%

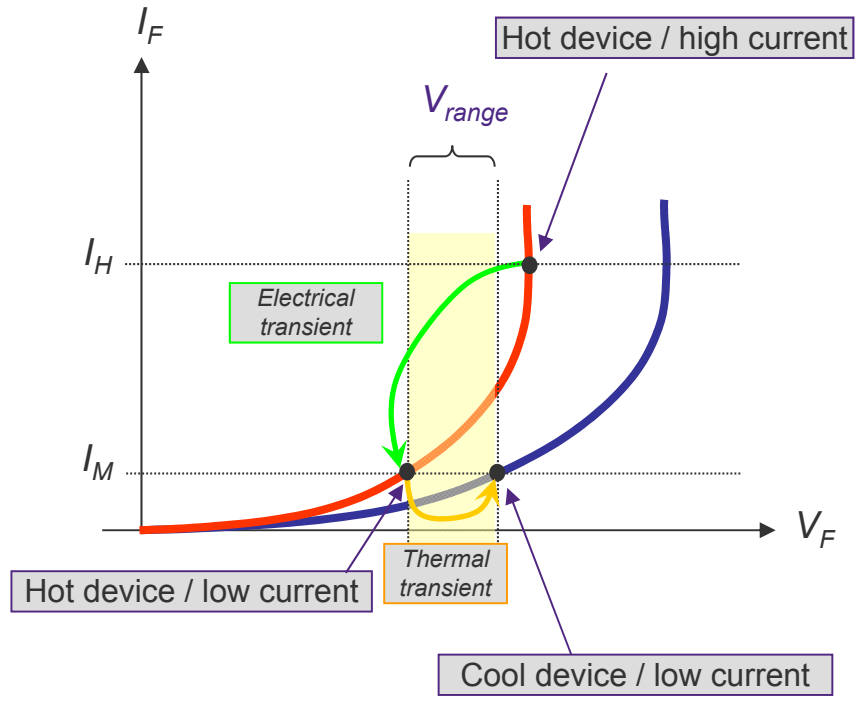
How to select the I_M measurement current?

- Recall the *static* test method:
  Higher I_M current provides advantages:
  - less disturbing electrical transients

High I_M



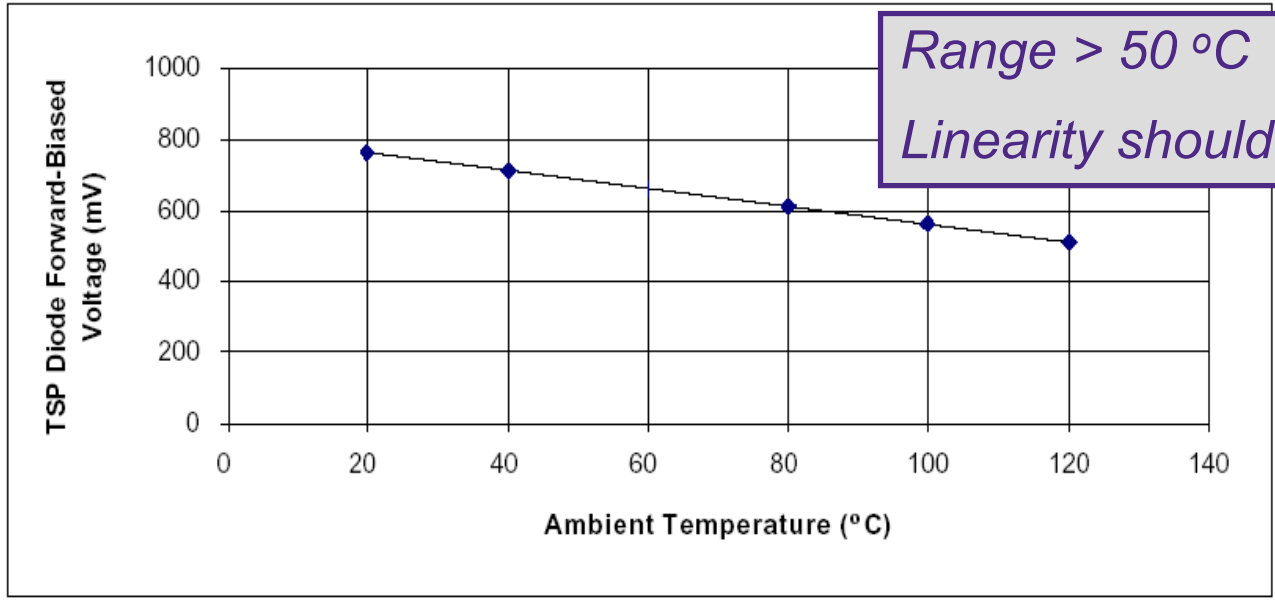
Small I_M



Higher I_M – smaller electrical transient

K-factor calibration according to JESD51-1

- Calibration should take place by applying the same I_M current as during the tests



Range > 50 °C

Linearity should be checked

Figure 11. Typical V_F - T_A curve for temperature-sensing diode forward biased with I_M.

$$\Delta T = \Delta V_F \cdot K$$

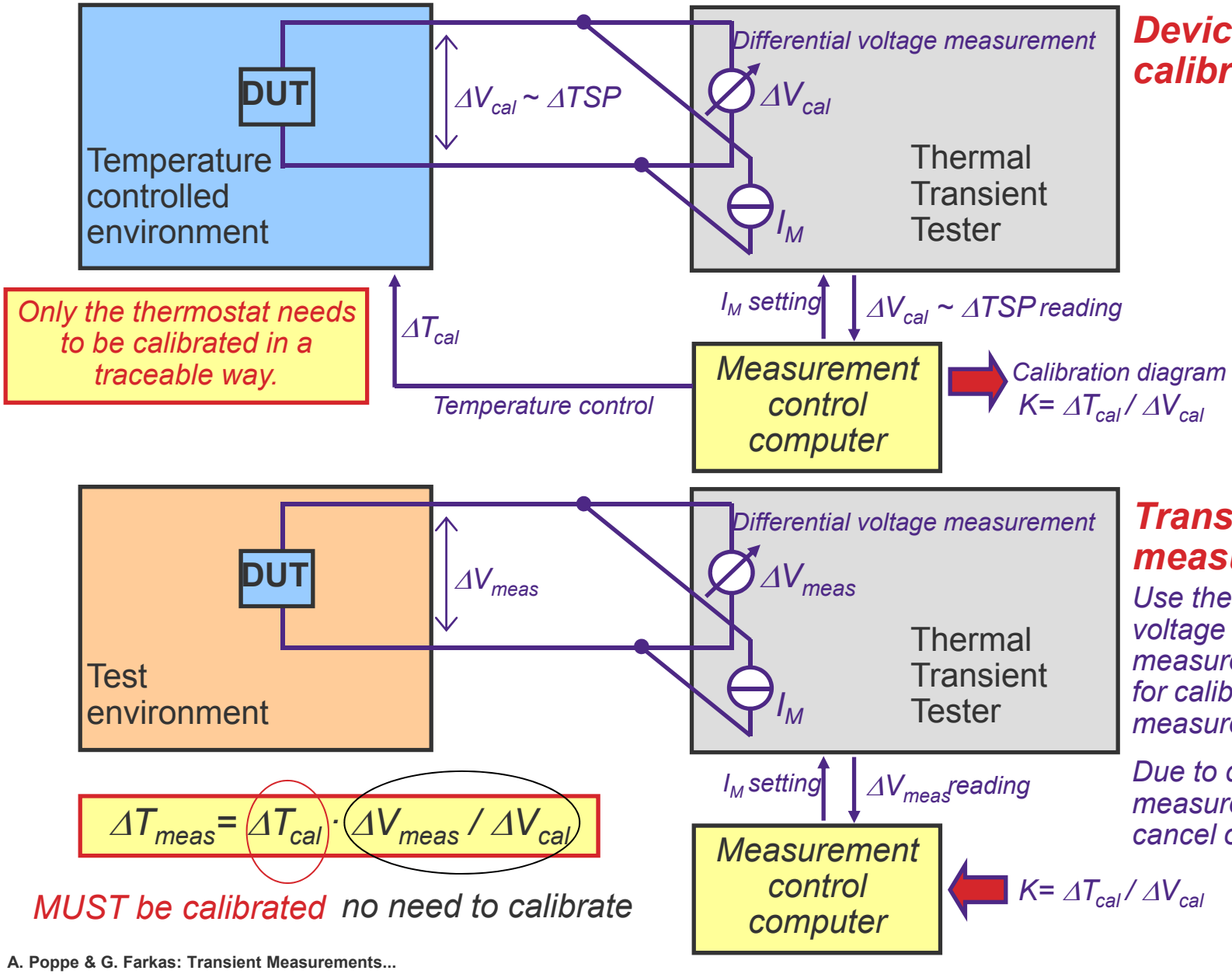
$$S_{VF} = 1/K$$

$$K = \left| \frac{(T_{Hi} - T_{Lo})}{(V_{Hi} - V_{Lo})} \right| \qquad (9)$$

[°C/mV]

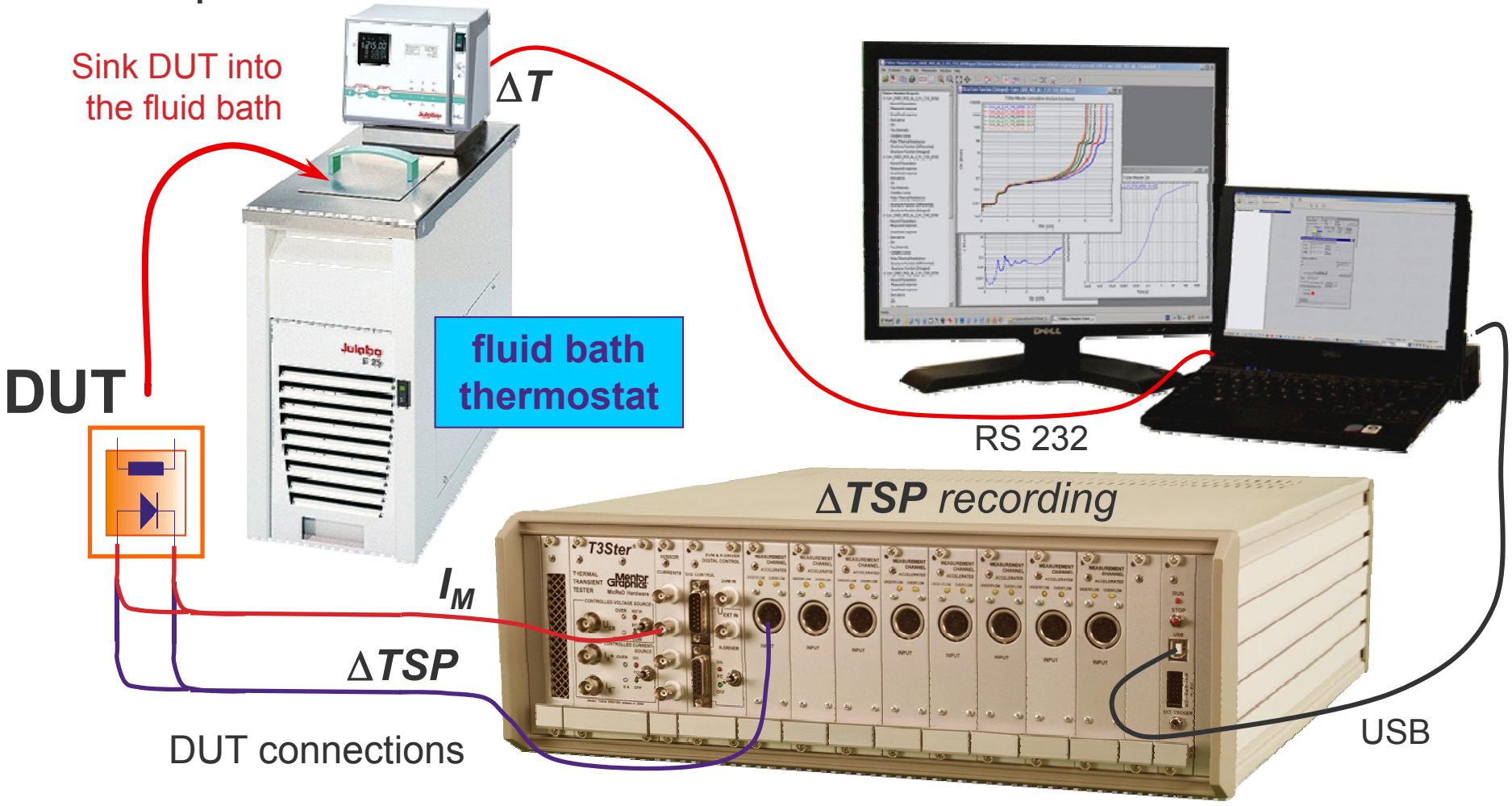
where T_{Hi} & T_{Lo} = High & Low temperatures [°C]
V_{Hi} & V_{Lo} = corresponding High & Low TSP voltages [mV]

Recommended setup for calibration and actual test



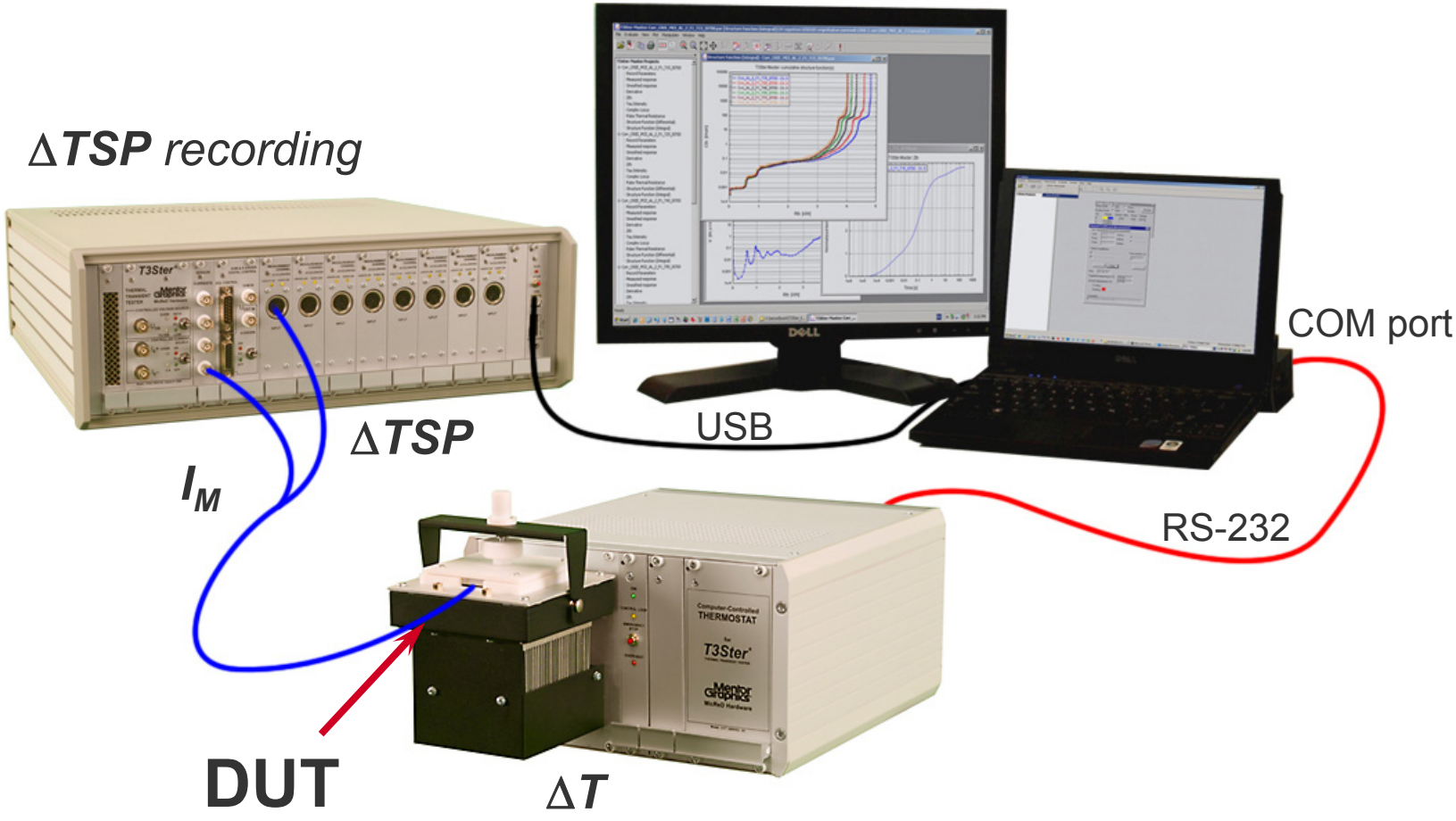
TSP calibration setup with a fluid-bath thermostat

- Device calibration – to identify the sensitivity of TSP.
- The ambient surrounding the DUT should have uniform temperature.



TSP calibration setup with a dry thermostat

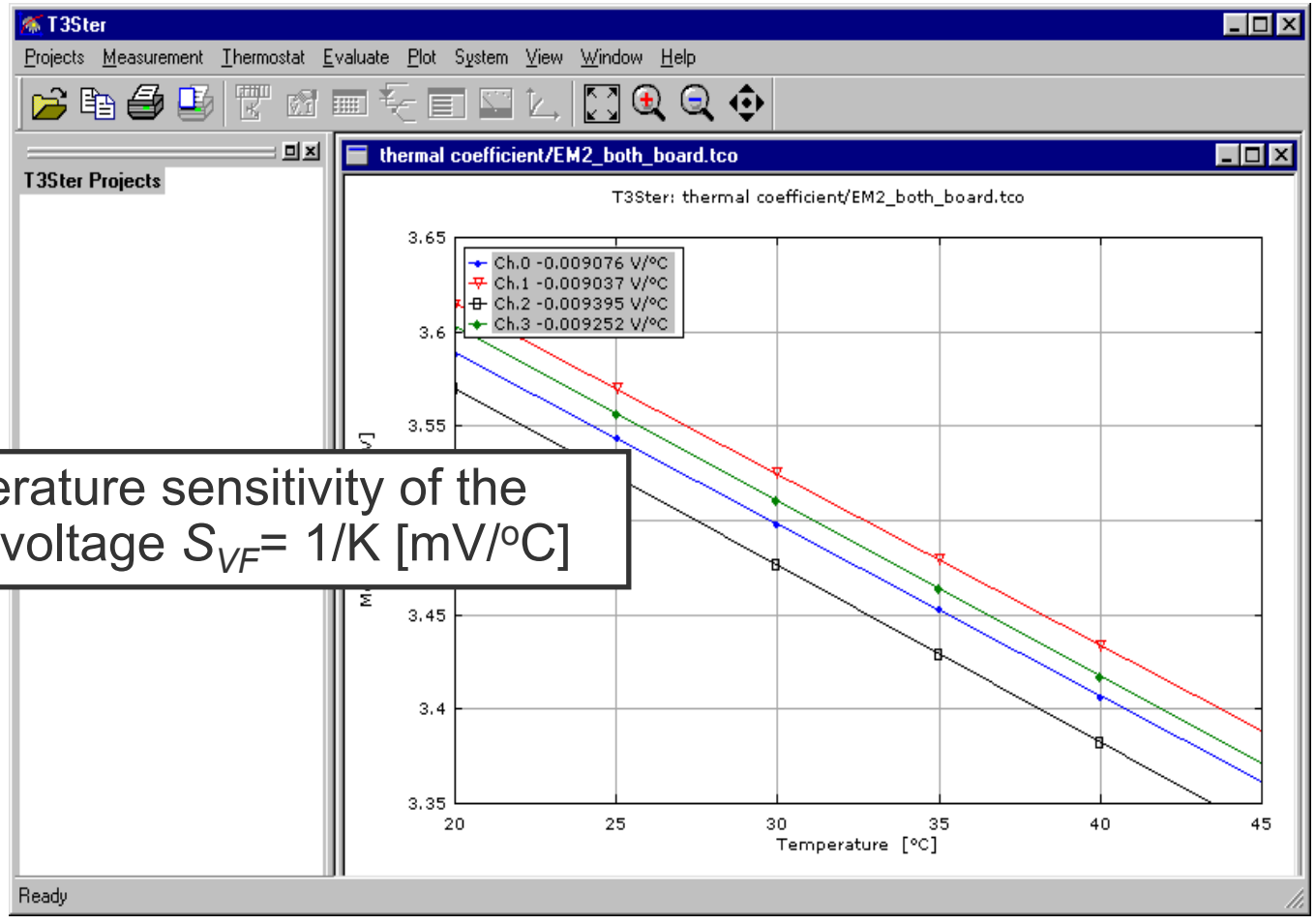
- Alternate solution: dry thermostat
- Can also be used as a test environment (cold plate)



Procedure specified in the JEDEC JESD51-1 standard

K-factor calibration diagram

- Device calibration – to identify the sensitivity of TSP



Temperature sensitivity of the forward voltage S_{VF}= 1/K [mV/°C]

Procedure specified in the JEDEC JESD51-1 standard

TSP calibration issues

- The temperature range covered during *TSP* calibration should cover at least the temperature range the DUT is expected to be tested in.
- Differential measurement of the *TSP* measurement is of great advantage
  - if using the same voltage measurement unit for *TSP* calibration and transient measurement, any (voltage) measurement error cancels out
  - that is why only the temperature measurement in the device calibrator must be NIST traceable
- *K*-factor slightly depends on the current used
  - Use the same sensor current at *TSP* measurement as used for calibration
- When the temperature sensitive parameter is inherently nonlinear (channel resistance, SiC or GaN junctions) the whole temperature-to-voltage mapping has to be stored

Limitations in using a K-factor

Issues in Testing Advanced Power Semiconductor Devices

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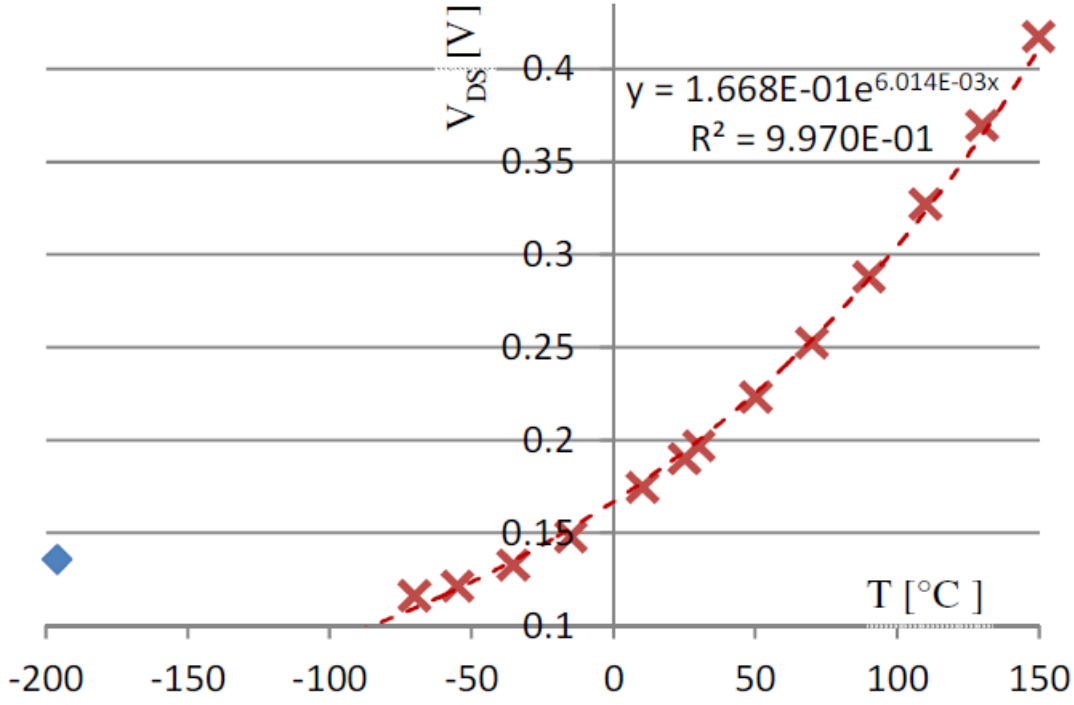


Figure 5: RDS calibration curve of the depletion device with exponential regression, at 0.5A measurement current

Environmental conditions

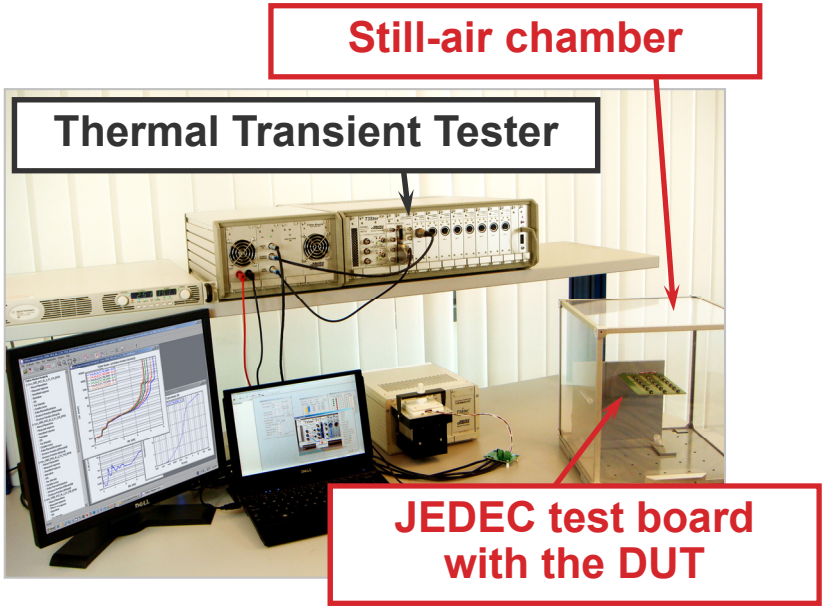
JEDEC standard test conditions

- Besides test equipment, standard test conditions need to be provided
  - test environments
    - natural convection
    - forced convection
    - cold plate
  - device fixtures / test boards

Natural convection: JEDEC JESD51-2A standard

Forced convection: JEDEC JESD51-6 standard

Different test boards: JEDEC JESD51-3, 5, 7, 10, 11

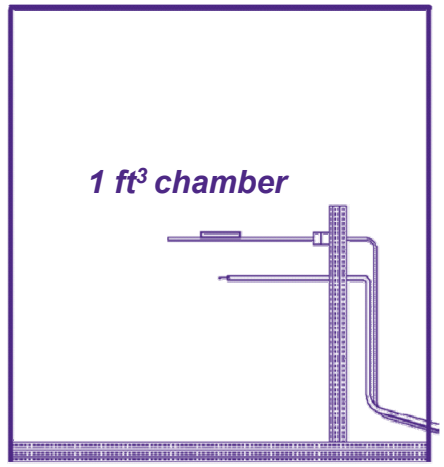


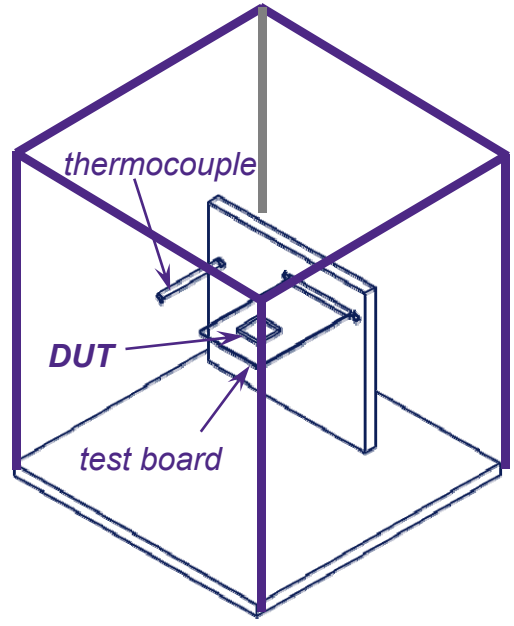
Source of image
http://www.utacgroup.com/technology_contents_analysis2.html

Still-air chamber / test board definitions examples

JEDEC JESD51-2A standard

Low conductivity chamber material (e.g. polycarbonat)





JEDEC JESD51-11 standard

Figure 1a — Cross section of 1s PCB showing trace and dielectric thicknesses in package placement and trace fan-out regions

Figure 1b — Cross section of 2s2p PCB showing trace and dielectric thicknesses

Table 1 — PCB sizes for packages

Package Length	PCB Size (+/- 0.25 mm)
Pkg. Length ≤ 40 mm	101.5 mm x 114.5 mm (4.0 in x 4.5 in)
40 mm < Pkg. Length ≤ 65 mm	127.0 mm x 139.5 mm (5.0 in x 5.5 in)
65 mm < Pkg. Length ≤ 90 mm	152.5 mm x 165.0 mm (6.0 in x 6.5 in)

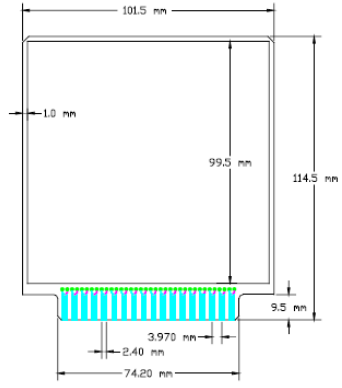


Figure 2 — Example test board outer dimensions and edge connector design

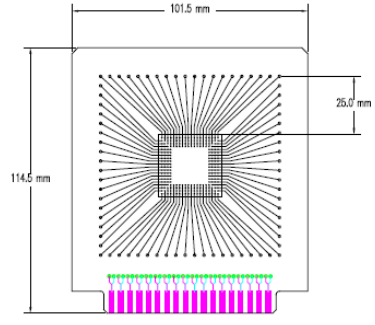
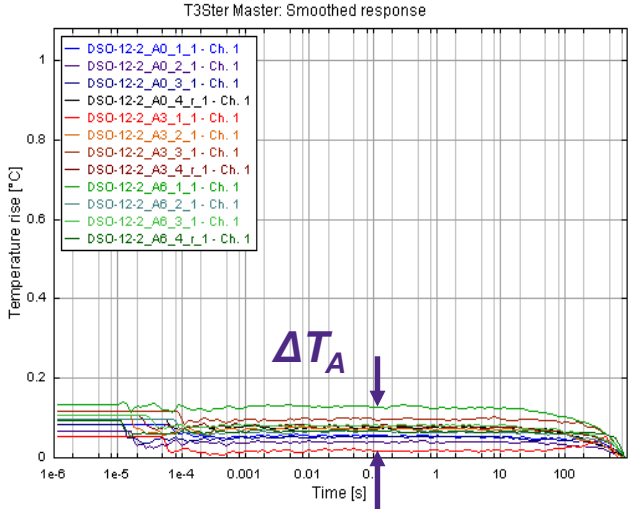
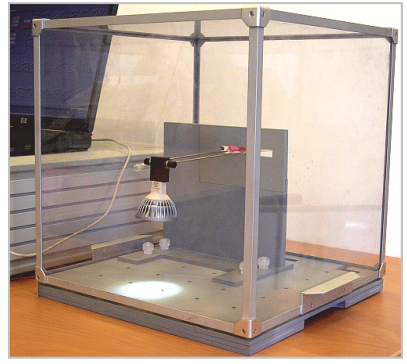


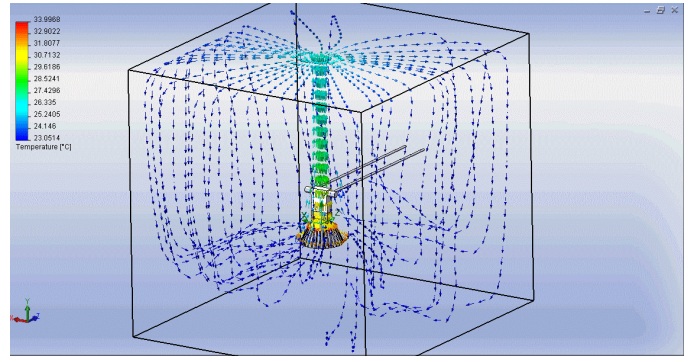
Figure 3 — Traces to outer pin row flared to perimeter 25 mm from package body.

JEDEC standard still-air chamber

- The chamber temperature must be measured according to the JEDEC standard
- It does not change too much when the transient extension of the static test method is used (max. variation is 0.2 °C in all practical cases)
  - no need to use this data except that
    - it is a good indicator if there is any odd air-flow inside the chamber
    - indicates other problems like air-heating due to e.g. direct sunshine



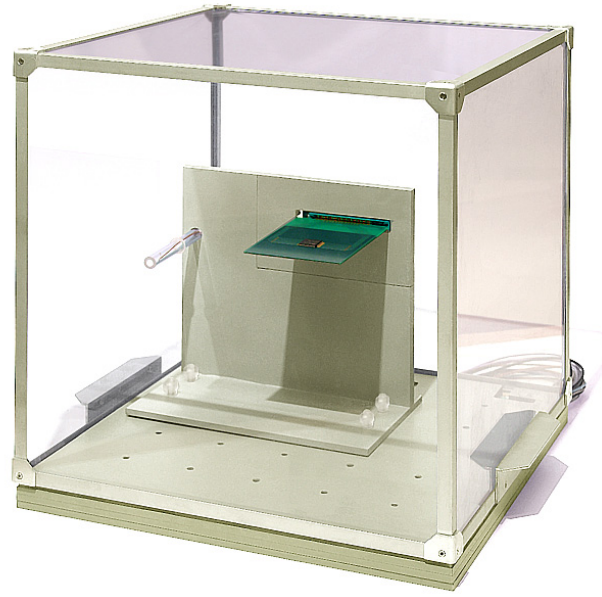


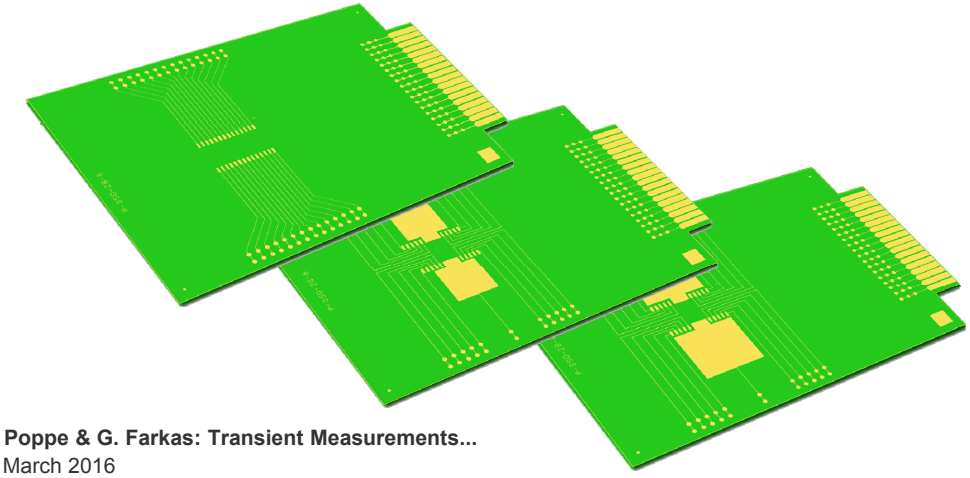


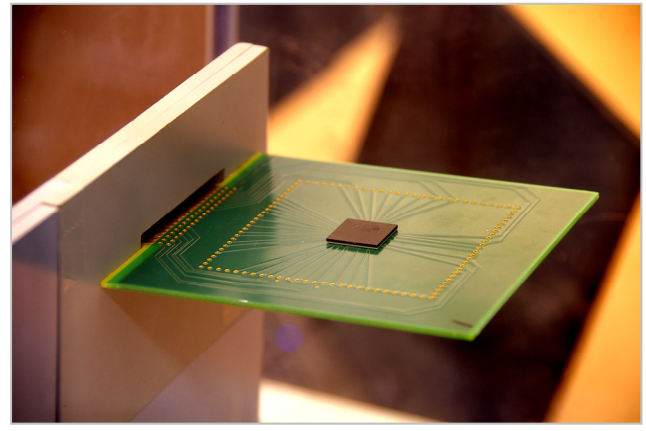
- as shown before, it cancels from our equations

JEDEC standard test conditions

- Test environments
  - natural convection: 1 ft^3 still-air chamber: **JESD51-2A** (2008)
  - forced convection: wind tunnel **JESD51-6** (1999)
- Test boards
  - copper coverage / number of layers
    - high / low conductivity, 1s / 2s
  - different designs mathching different package styles
  - design / orientation counts a lot, as shown by structure functions

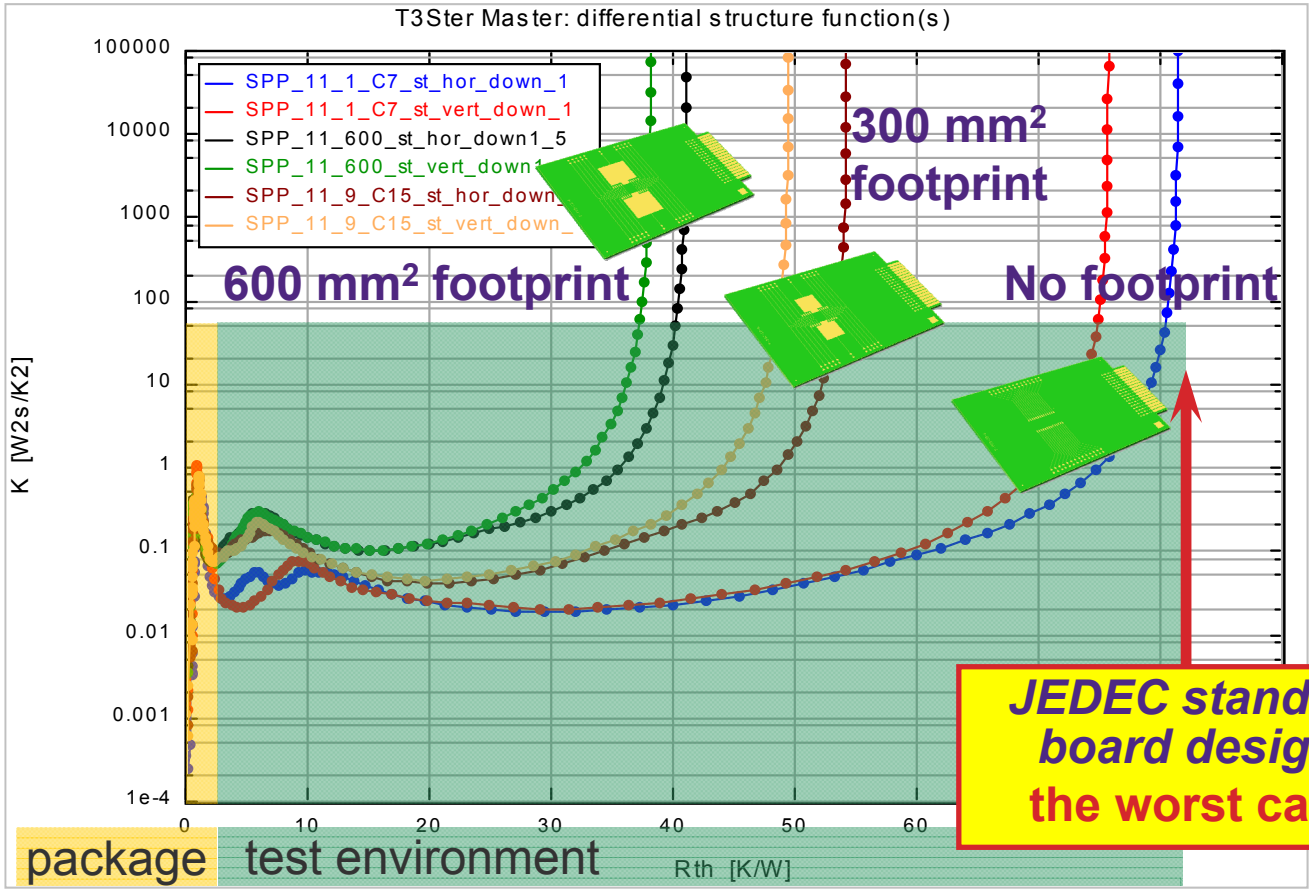






Effect of test board design / orientation

- Tests performed in a JEDEC standard still-air chamber
- Measured transients converted to structure functions



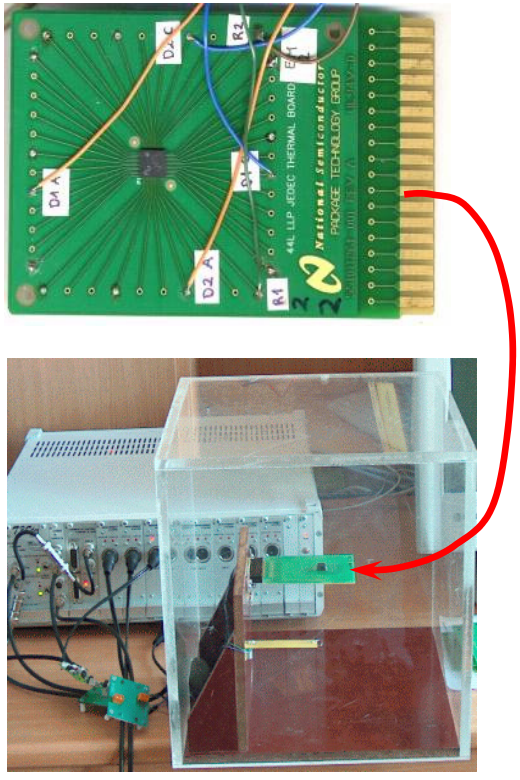
Board design (Cu area of footprint region) and board position (vertical or horizontal) strongly effects the ultimate R_{thja} value

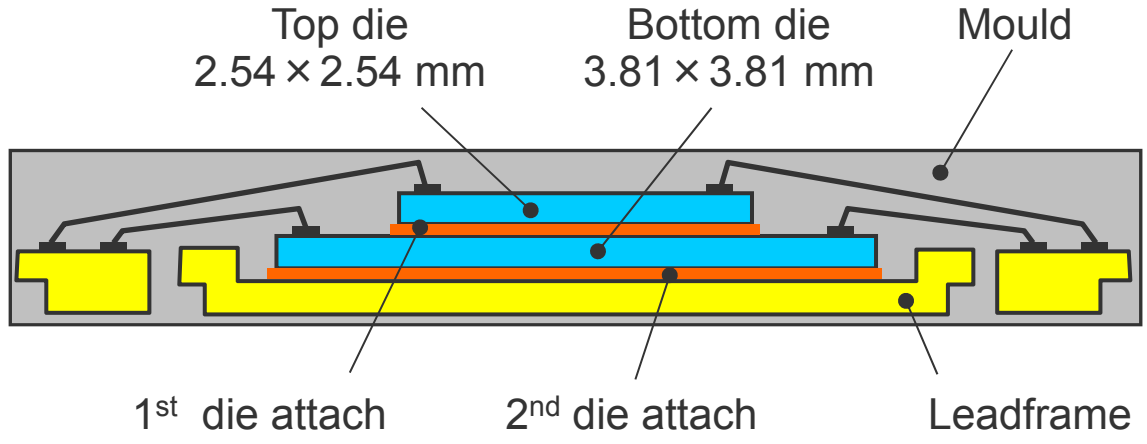
JEDEC standard board design:
the worst case

- Measured R_{th} is mostly due to the test environment
  - measure on cold plate if possible, it is also faster

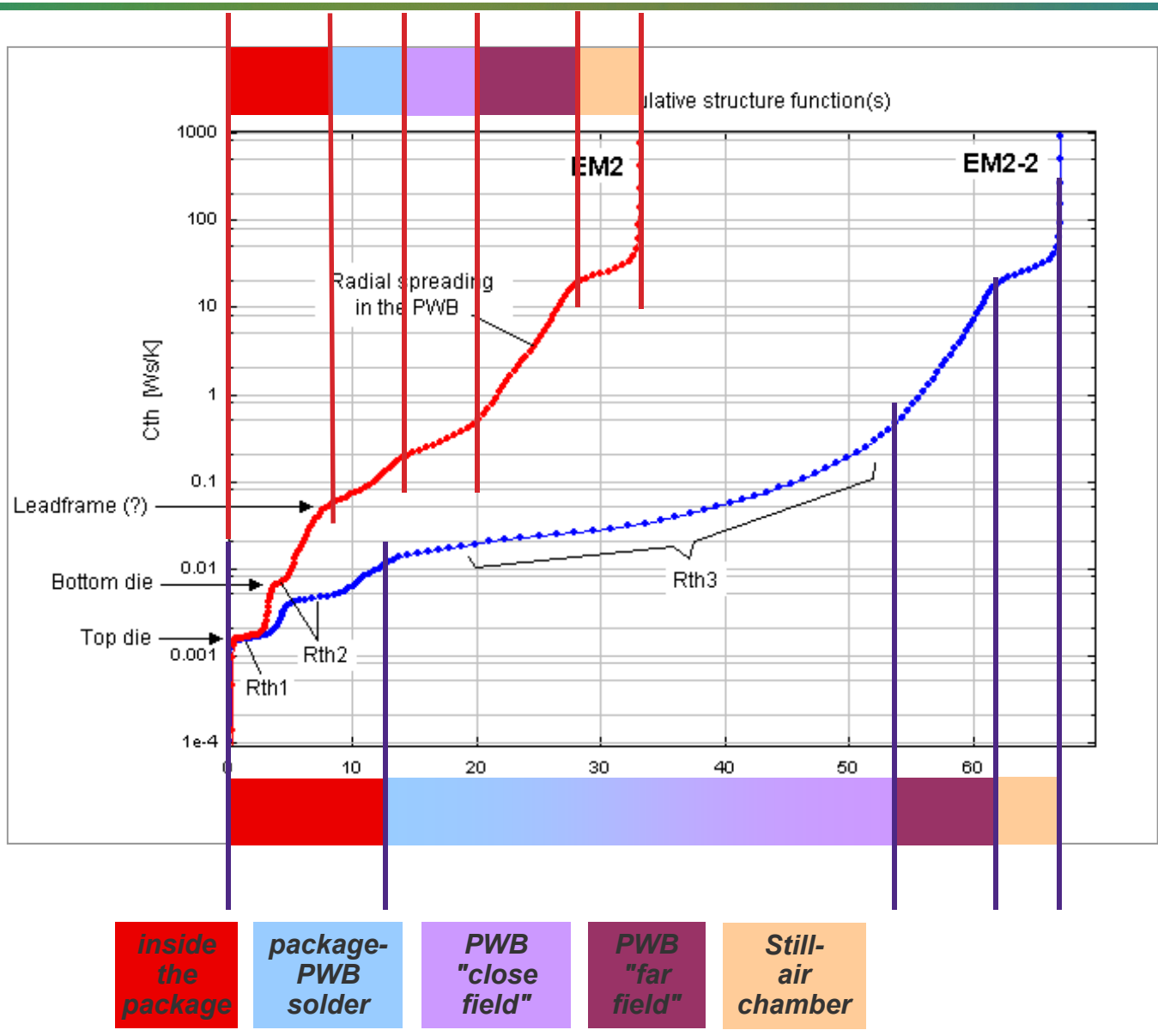
Two live chips stacked in a 44L LLP package

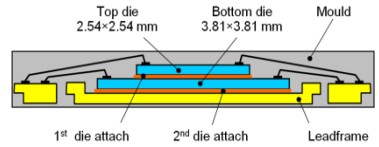
- Stacked die package tested in JEDEC standard test environment
- Transient extension of the JESD51-1 static test method was used (**T3Ster** equipment), followed by structure function analysis

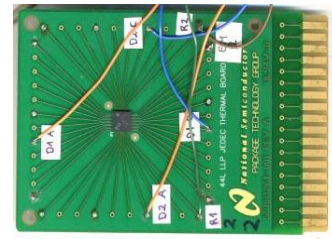


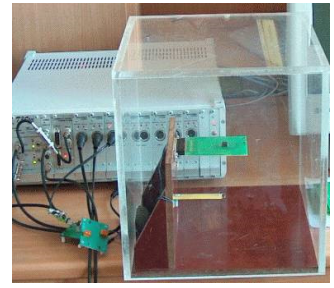


Results in terms of structure functions





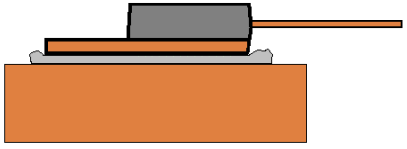


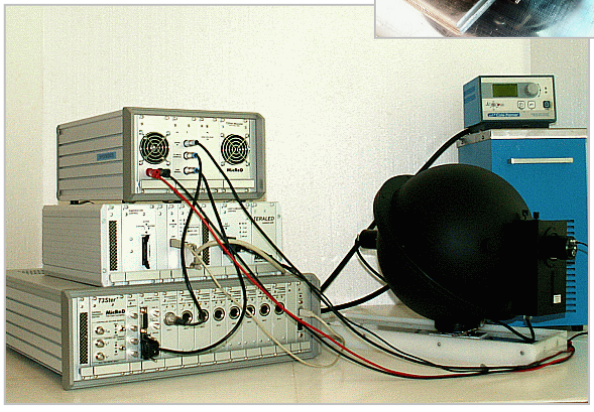


Majority of the R_{thja} is caused by the JEDEC standard test environment.

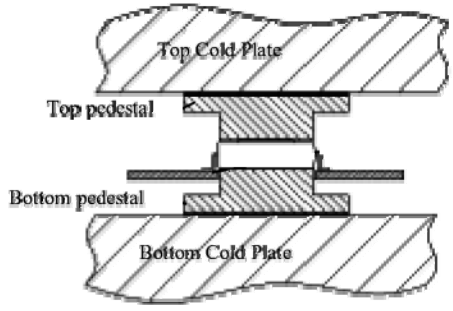
Cold plate as a test environment

- Single cold plate setups for R_{thJC} measurements
  - also, test based models of power packages (transient extended JEDEC 2R models)
  - LED testing
- Quicker test, shorter heat-flow path, results are characteristic to the package



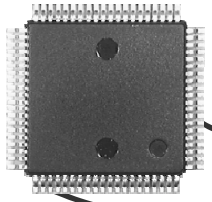


- Dual cold plate setups for DELPHI boundary conditions
  - validation of detailed models of test set of boundary conditions
  - DCP1, DCP2, DCP3, DCP4 setups



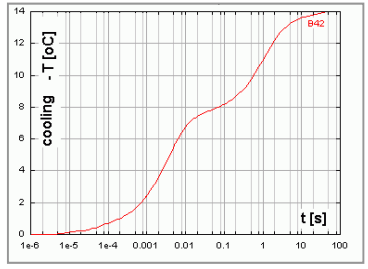
Test based model validation: for DELPHI models

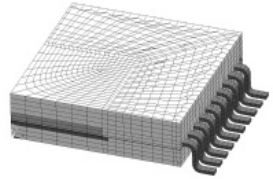
Real package



T3Ster

Thermal transient measured by ***T3Ster***





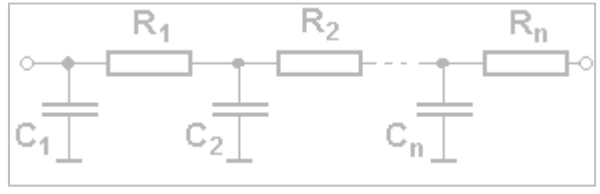
Detailed package model

Automated process now in FloTHERM v11

FloTHERM

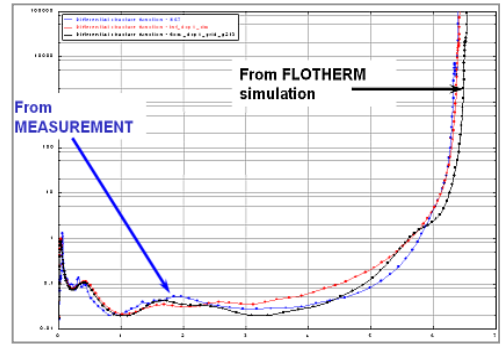
T3Ster software

Structure functions for test based compact model generation



FloTHERM

Structure functions for validation of detailed models



This model structure is characteristic to power semiconductor packages

Special environment for power LEDs: cold-plate and integrating sphere

Test environment for LEDs: cold-plate and sphere

CIE 127-2007 compliant photometric & radiometric measurement system

photometric/radiometric measurements in thermal steady-state

JESD51-52

steady-state electrical powering

I_F

Detector

Integrating sphere

Test LED

I_F

V_F

Temp. controlled heat-sink

Aux. LED

Force (current)

Thermal test equipment

Sense (voltage)

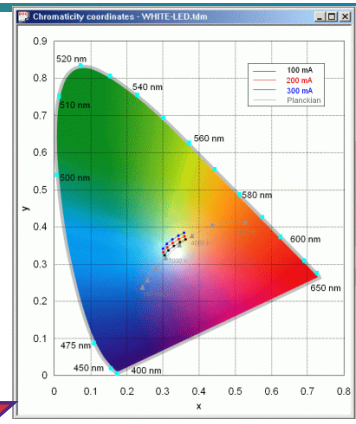
I_H

I_M

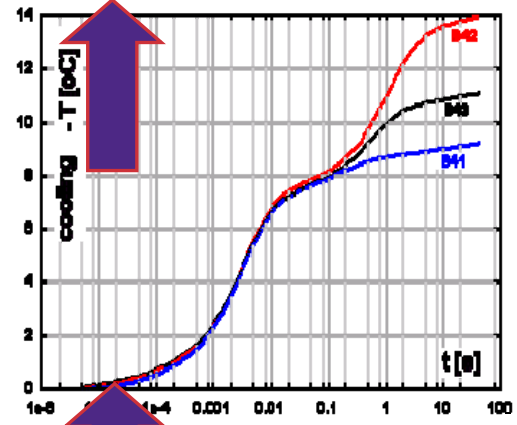
switching-off from I_H to I_M

$\Delta V_F(t)$ ~ $\Delta T_J(t)$

$P_{opt}(T,I_F)$
$\eta_e(T,I_F)$
$\Phi_V(T,I_F)$



calculate $R_{th\text{-}r}$ and T_J

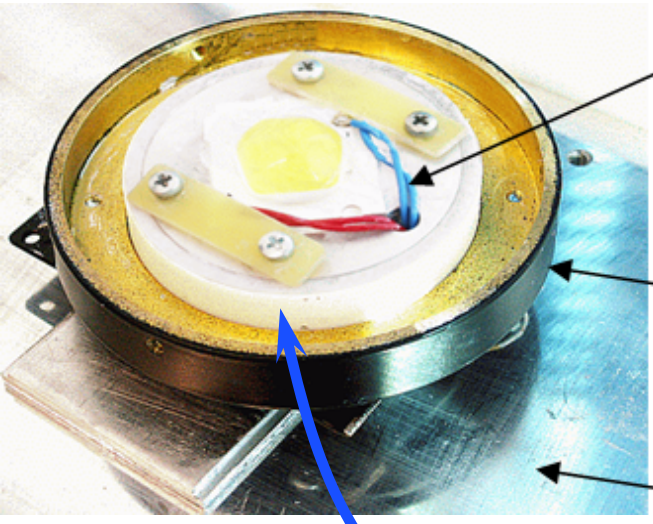


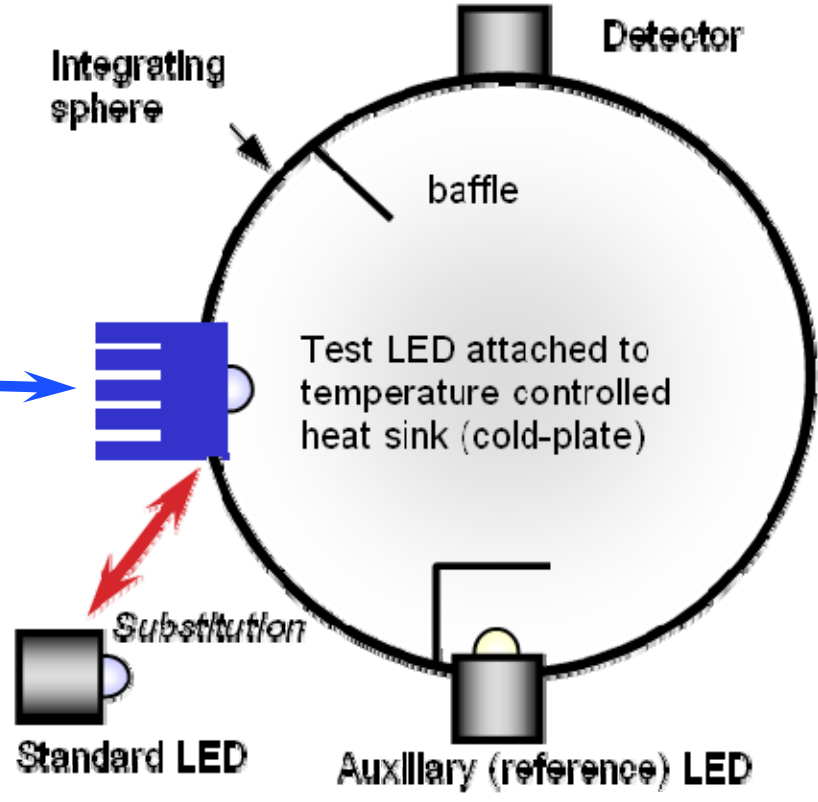
thermal resistance/impedance measurement

JESD51-51

JEDEC JSD51-1 static test method compliant thermal measurement system

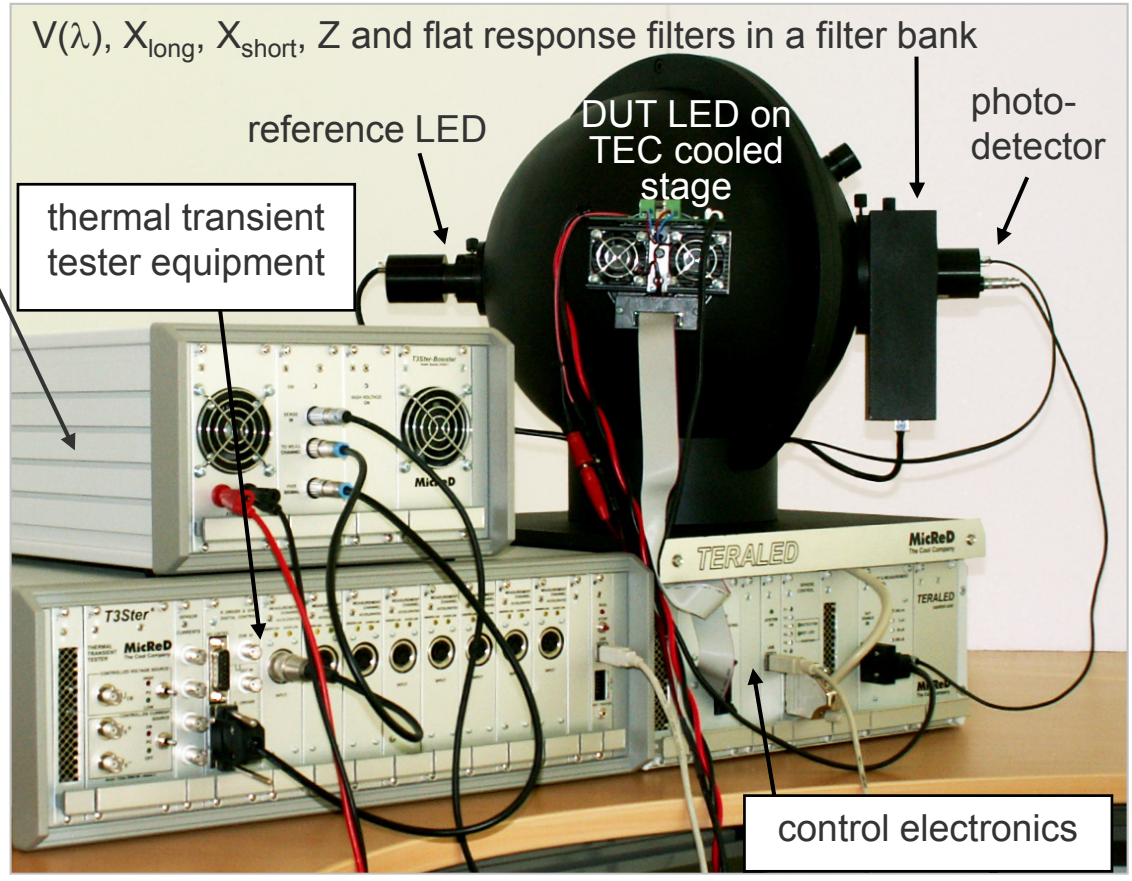
Some details of the test environment





The Mentor Graphics MicReD implementation:

Special LED booster: allows high voltage across a LED line (overall forward voltage can reach 280V).

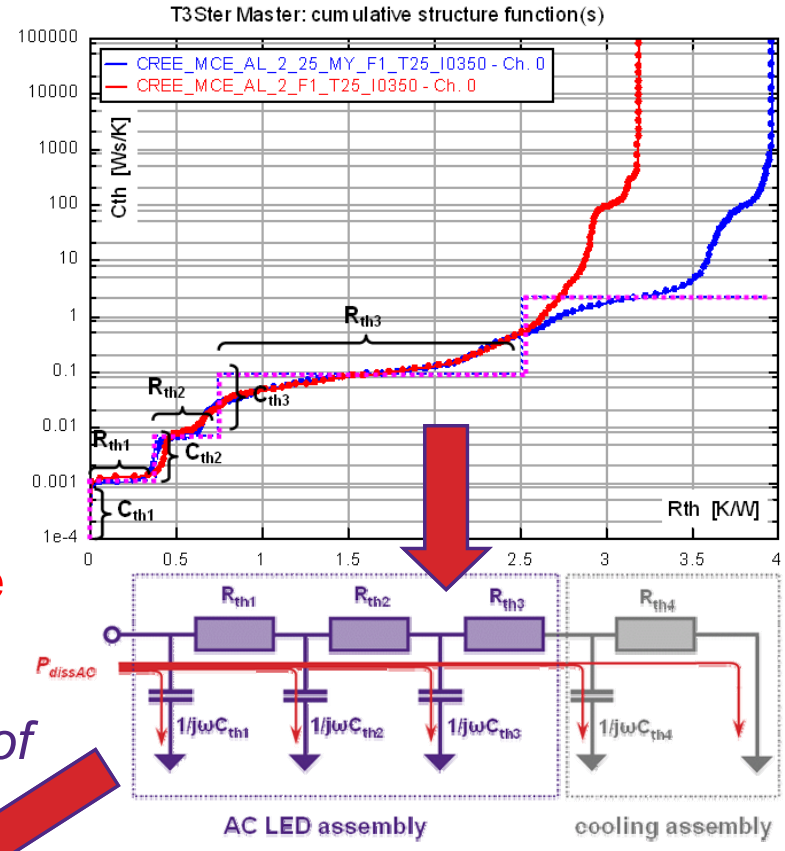


It can be added to the system in a plug&play manner if the voltage of the base tester is not sufficient.

Different representations of the thermal impedance

Different representations of the thermal impedance

- There is a single "Z_{th}" of the heat-flow path only
- Can be represented by structure functions and RC models



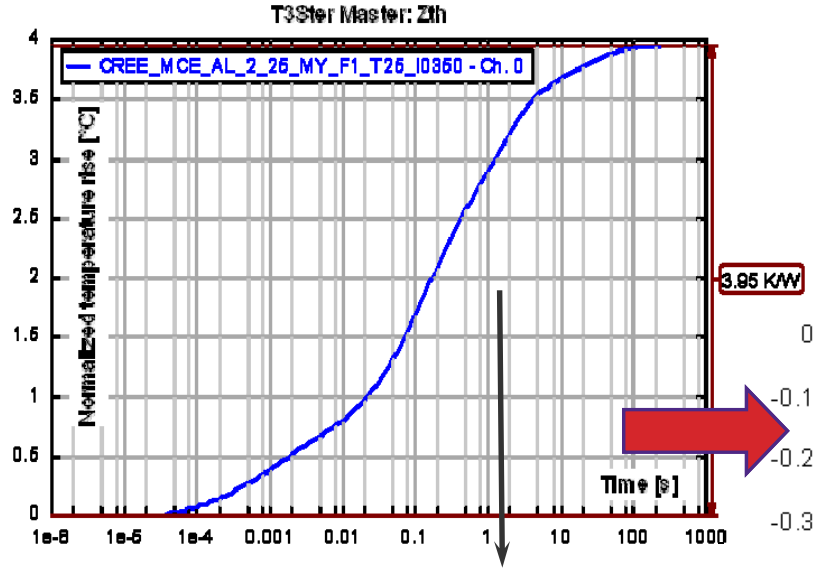
A simple model can be created, suitable even for hand calculations.

At higher frequency the absolute value of Zth(ω) *is smaller*

$$Z_{th}(\omega) = \frac{1}{j\omega C_{th1}} \times \left\{ R_{th1} + \frac{1}{j\omega C_{th2}} \times \left(R_{th2} + \left[\frac{1}{j\omega C_{th3}} \times \left(R_{th3} + Z_{th-cooling\_ass} \right) \right] \right) \right\}$$

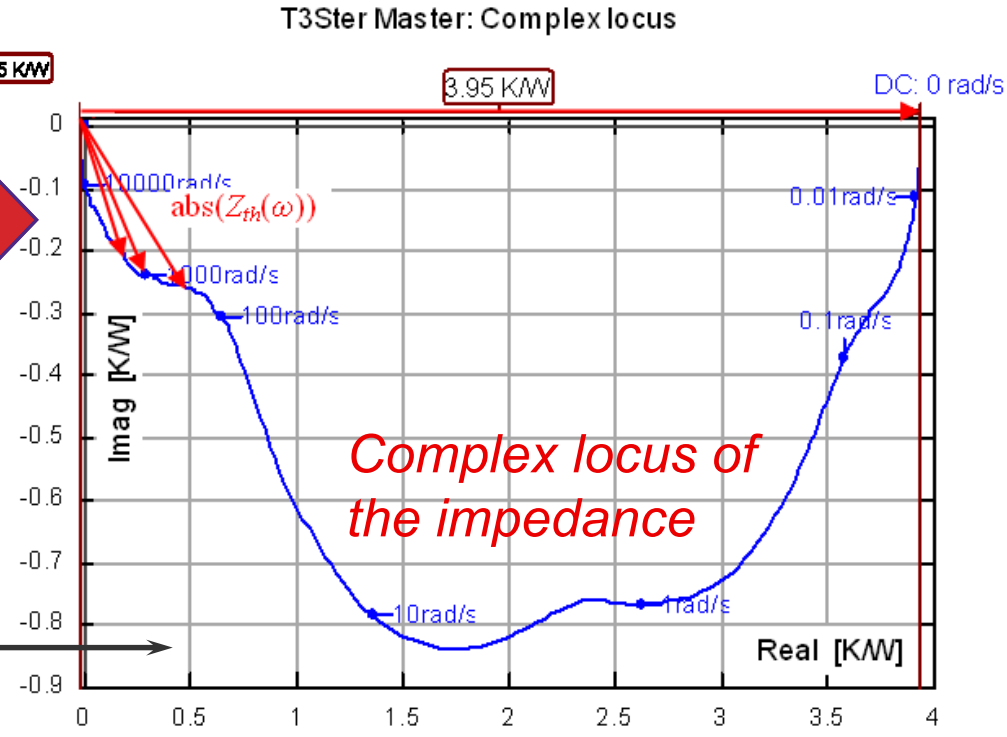
Different representations of the thermal impedance

- There is a single "Z_{th}" of the heat-flow path only
- Frequency domain representation is Ok e.g. for AC LEDs



$$Z_{th}(\omega) = \int_0^{\infty} Z_{th}(t) e^{-j\omega t} dt$$

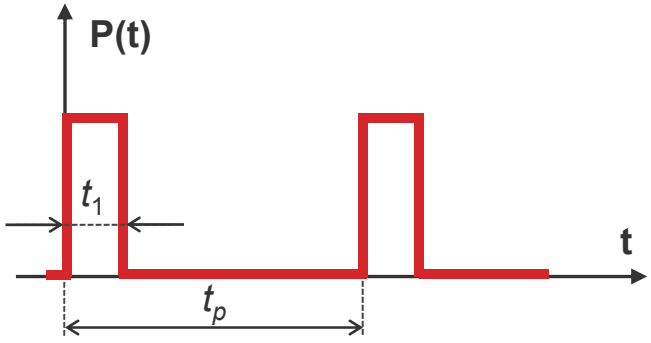
At higher frequency the absolute value of $Z_{th}(\omega)$ is smaller:



Allows calculating "the" thermal impedance at any frequency.

The concept of pulse thermal resistance

- In case of the Zth-matrix concept we have seen the concept of spatial and temporal superposition
- The concept of the pulse thermal resistance is derived from the temporal superposition concept
- The concept of pulse thermal resistance is used to predict the average stationary temperature of a single heat-source subject to a series of square wave dissipation with a given pulse width t_1 and period t_p



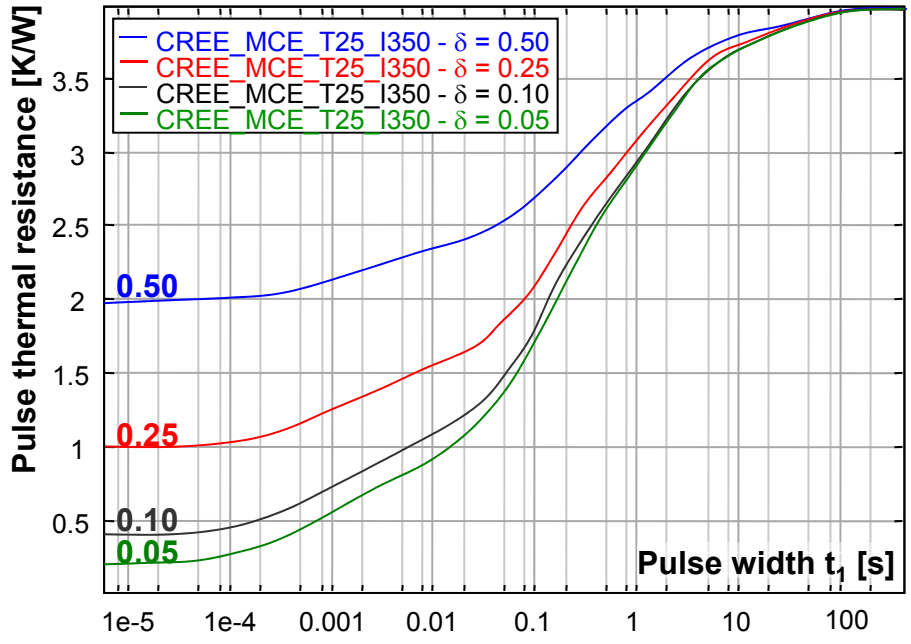
$\delta = t_1 / t_p$ is called *duty factor*

- Provided that the $R_\zeta(z)$ time constant spectrum of the driving point thermal impedance is known the pulse thermal resistance can be calculated as

$$Z_{th}(z = \ln t_1, \delta) = R_\zeta(z) \otimes \frac{1 - \exp[-\exp(z)]}{1 - \exp[-\exp(z)/\delta]}$$

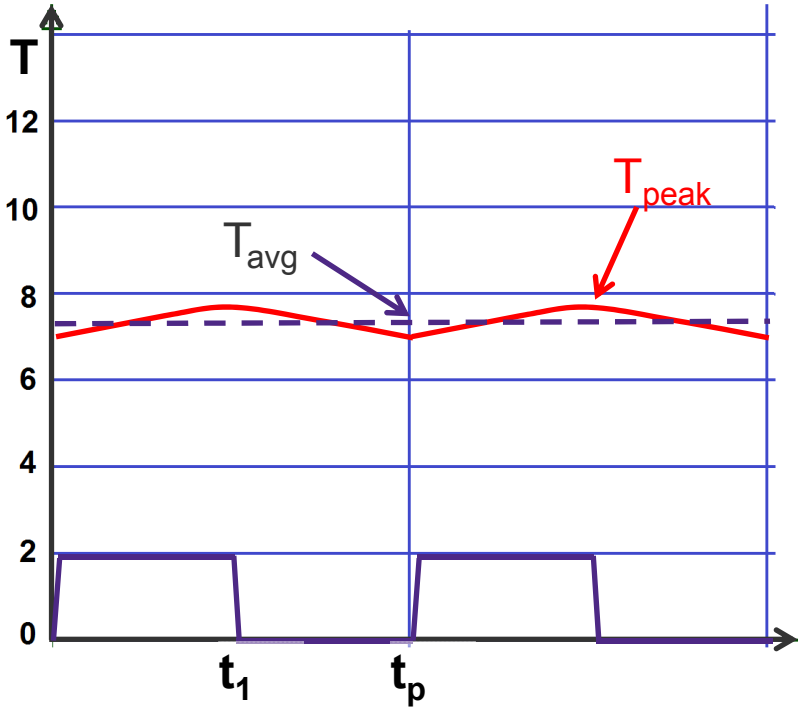
The concept of pulse thermal resistance

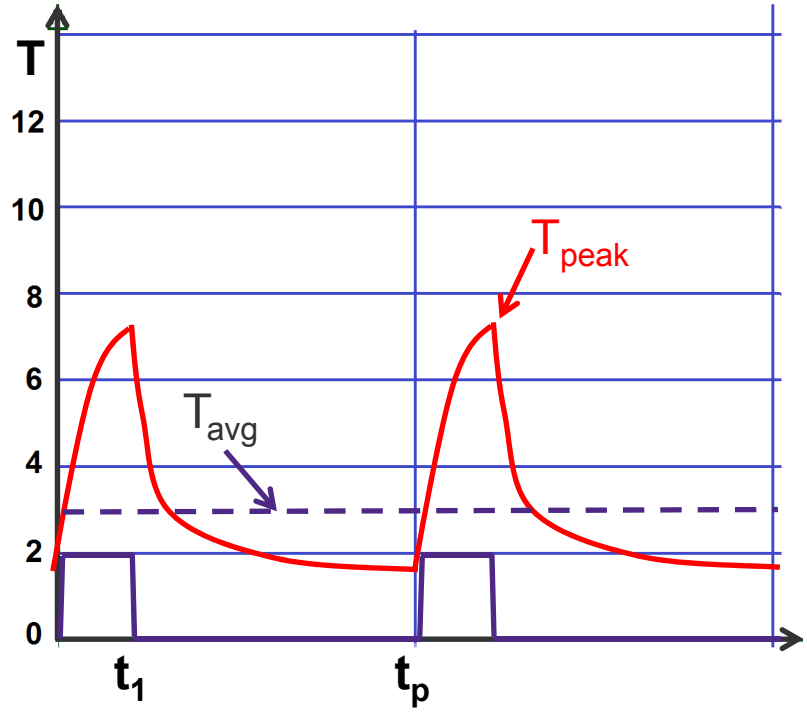
- The usual parameters are: t_1 pulse width and δ duty factor



- The average and peak junction temperature response to the thermal load of **devices operated in pulsed mode** can be predicted this way

Examples

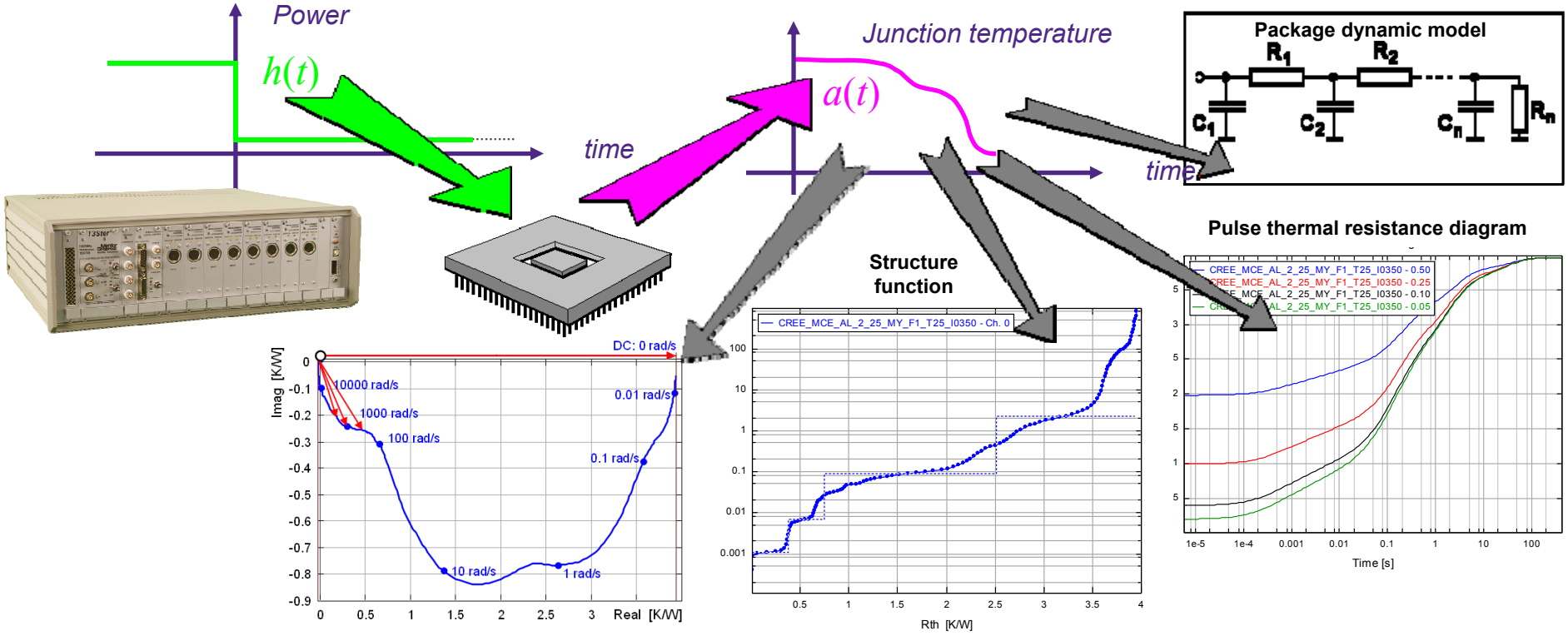




t_1=0.1ms, t_p=0.2ms, δ=0.5, f=1/t_p=5kHz, dT_{peak}=7.8K, dT_{avg}=7.3K

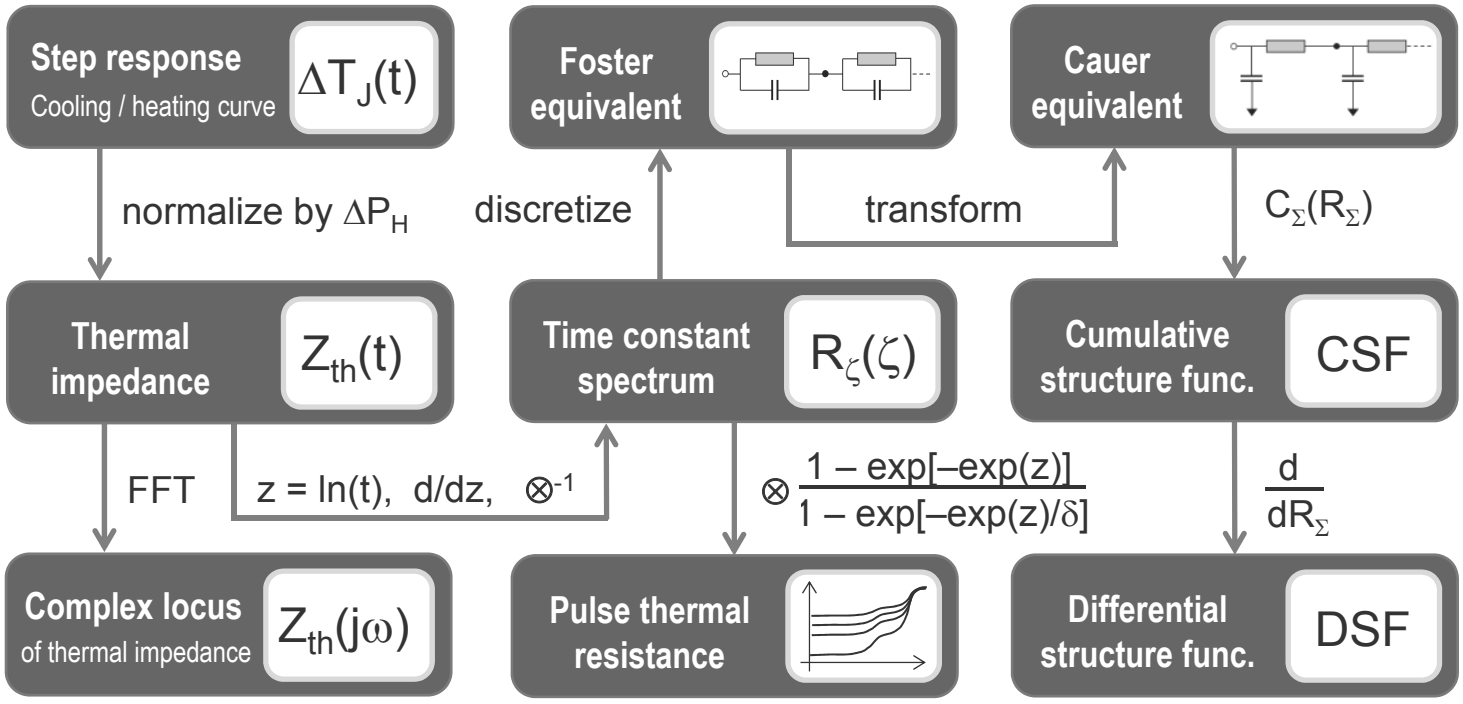
t_1=1ms, t_p=5ms, δ=0.2, f=1/t_p=200Hz, dT_{peak}=6.9K dT_{avg}=2.9K

Summary of thermal transient testing



- Thermal transient testing:
  - The $h(t)$ step-wise change in heating is applied at the junction (abrupt switching)
  - The $a(t)$ temperature response at the junction is being measured (unit-step response function) while linearity is assumed. Typical resolution is 1μs / 0.01 °C
- All available information is extracted from $a(t)$ using sophisticated mathematical procedures:
  - structure functions ➔ **structural analysis, failure detection**
  - pulsed thermal resistance ➔ **thermal design of pulsed operation**
  - complex locus (frequency domain rep.) ➔ **thermal design of AC driven devices**

Different representations of the thermal impedance



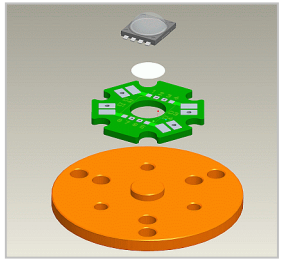
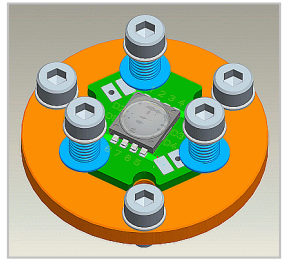
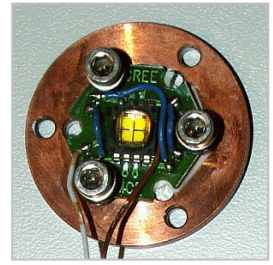
Taken from Chapter 4 ("Thermal testing of LEDs" by G. Farkas and A. Poppe) of the book **"Thermal Management of LED Applications"** (eds: C. J. M. Lasance and A. Poppe) by **Springer** in **2014** in the *Solid State Lighting Technologies and Applications series.*

Chart created after B. Vermeersch

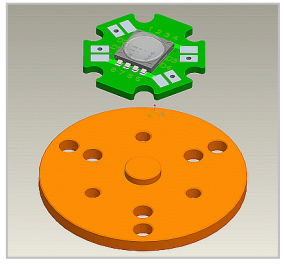
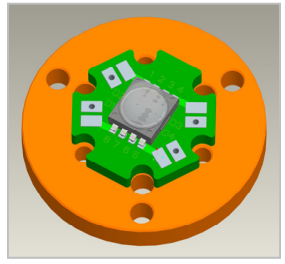
Case study:
Thermal management solutions for a 10 W white LED

Case study: 3 setups with Cree MCE 10W LEDs

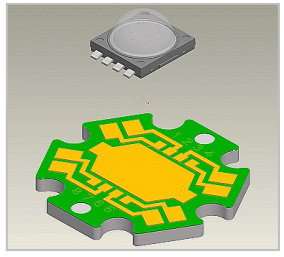
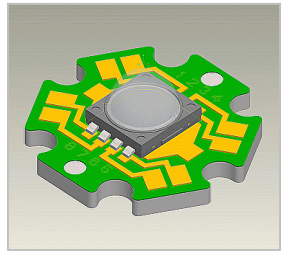
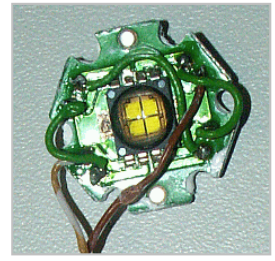
- 3 different kinds of assemblies:
  - FR4 PCB, TIM between the heat-slug and the Cu block

  - FR4 PCB, heat-slug soldered to the Cu block

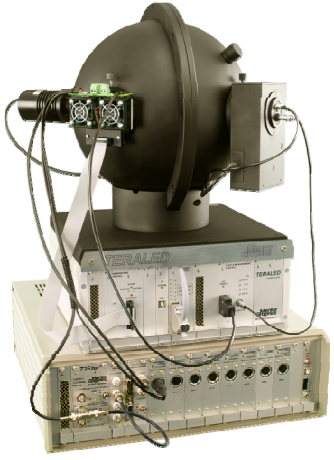

  - MCPCB-s made of Al and Cu, heat-slug soldered

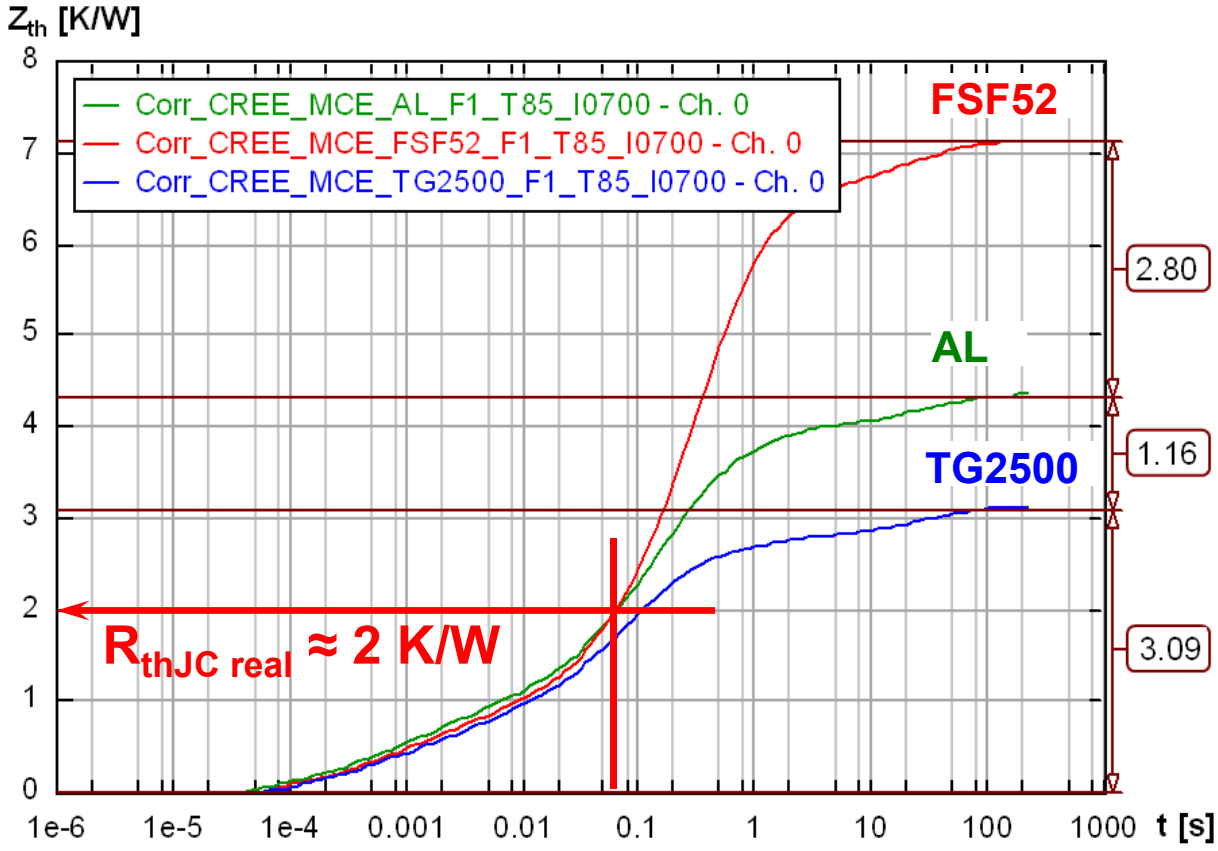




CAD images by courtesy of OptimalOptik Ltd. (Budapest, Hungary), measurements by Budapest University of Technology and Economics (BME).

Results for 10W Cree MCE white LEDs

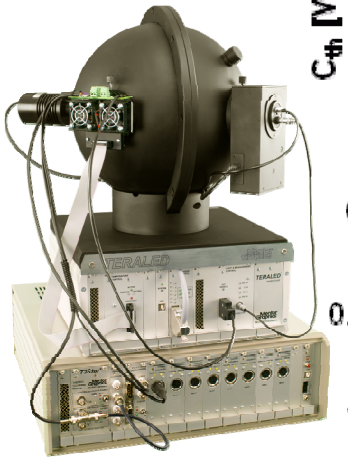
- Measured at 700 mA and 85°C
  - Thermal impedance of 3 samples, power corrected with P_{opt}

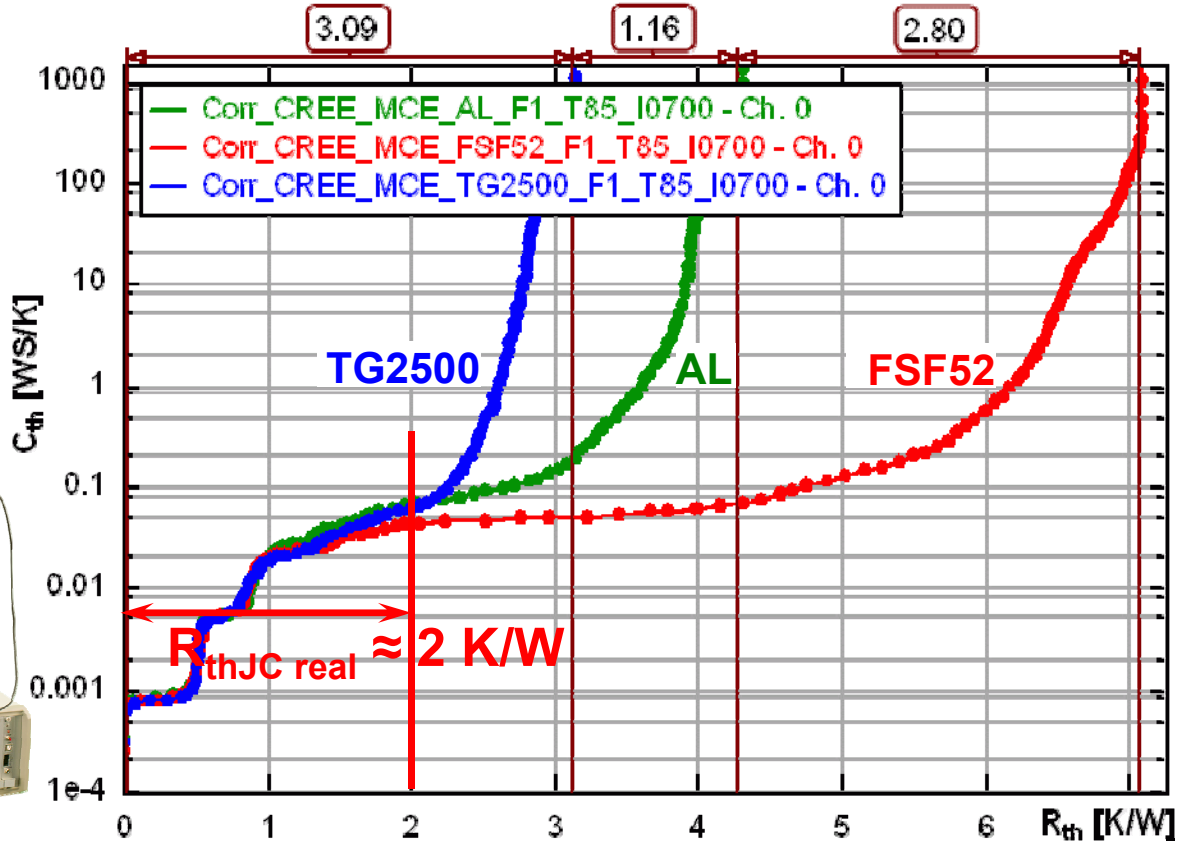




Results for 10W Cree MCE white LEDs

- Measured at 700 mA and 85°C
  - Structure functions of 3 samples, power corrected with P_{opt}

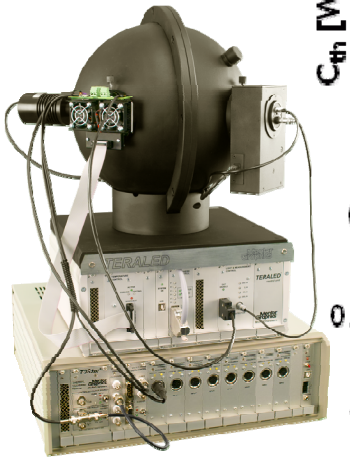


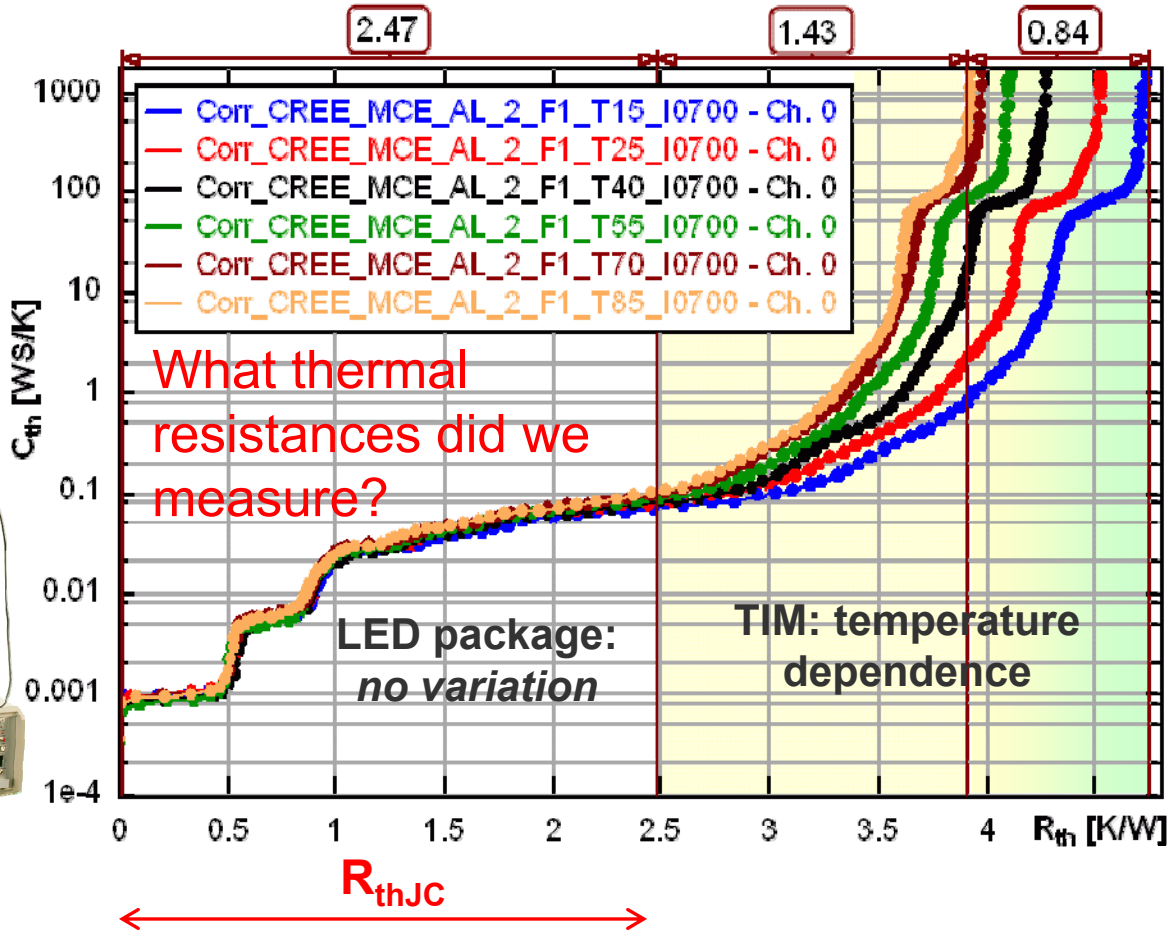


  - R_{thJC} is identified in a way similar to the *transient double interface method*, also being standardized by the JEDEC JC15 committee

Results for 10W Cree MCE white LEDs

- Measured at 350/700 mA & between 15°C and 85°C
  - Structure functions of sample AL-2, power corrected with P_{opt}



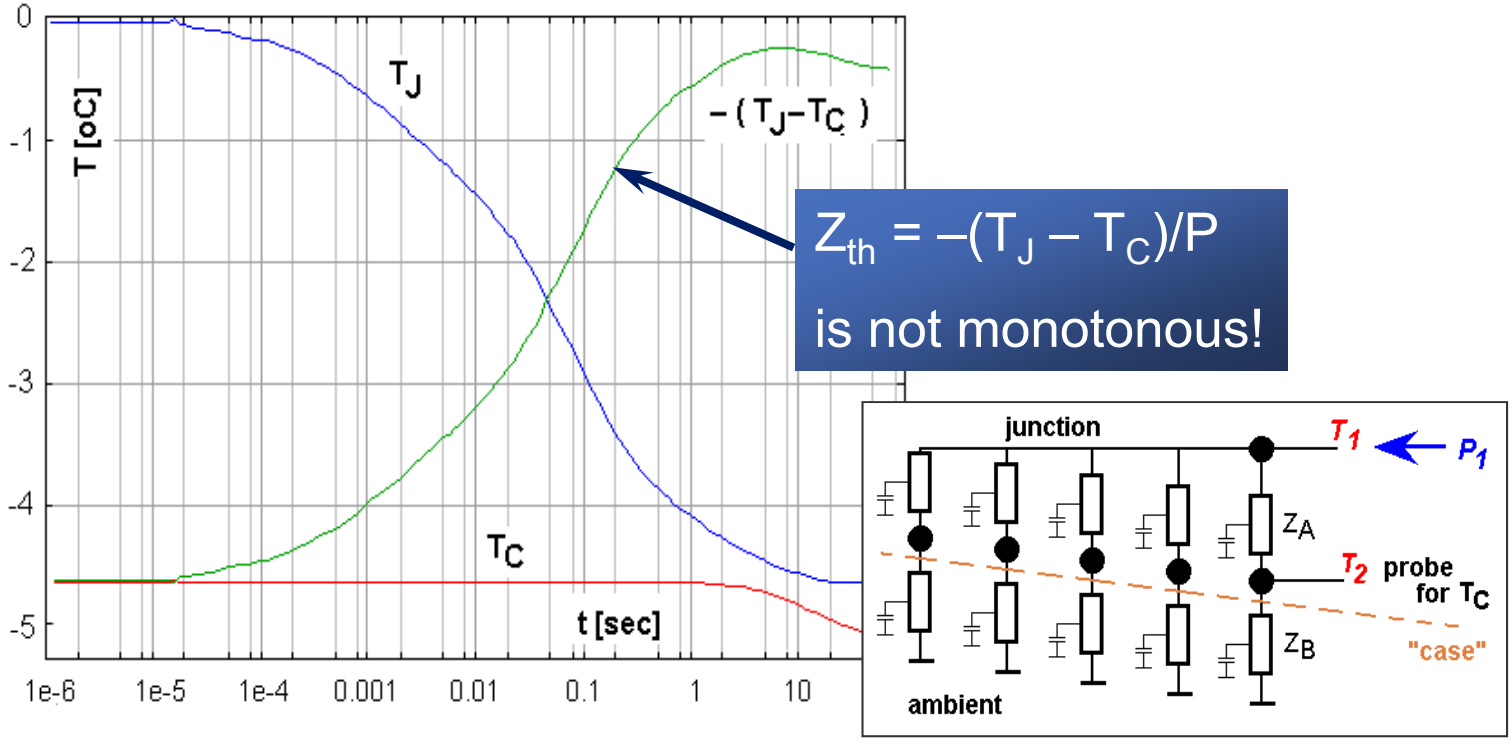


We measured the R_{thJC} of the package and the TIM resistance

The process of finding the R_{thJC} value in T3Ster Master 2.x according to the new JEDEC standard JESD51-14

Power package: transient measurements

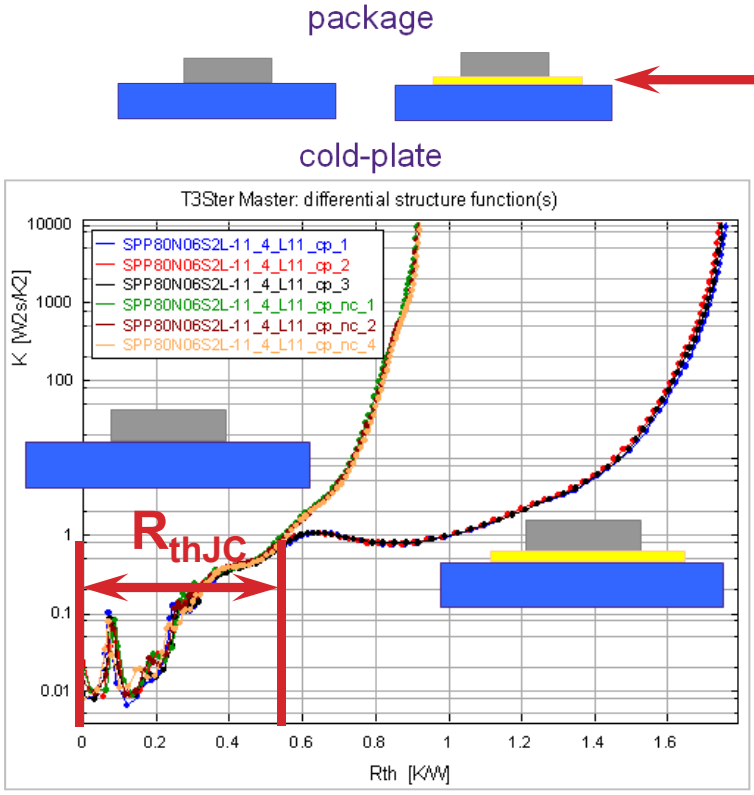
- Cooling curve for a diode with transient case-temperature probing:
- $Z_{th} = -(T_J - T_C)/P$ as dynamic extension of R_{thJC}?



- Z_{th} derived as $-(T_J - T_C)/P$ is just is a difference of a self-impedance and a transfer impedance: **It has no physical meaning! → new definition of R_{thJC} by JEDEC JESD 51-14**

The transient dual interface method for R_{thJC}

- Original idea from 2005, **standard JESD51-14 published in November 2010**
- Change of thermal interface quality at the ‘case‘ surface
- Divergence point in measured structure functions: ‘case’ surface

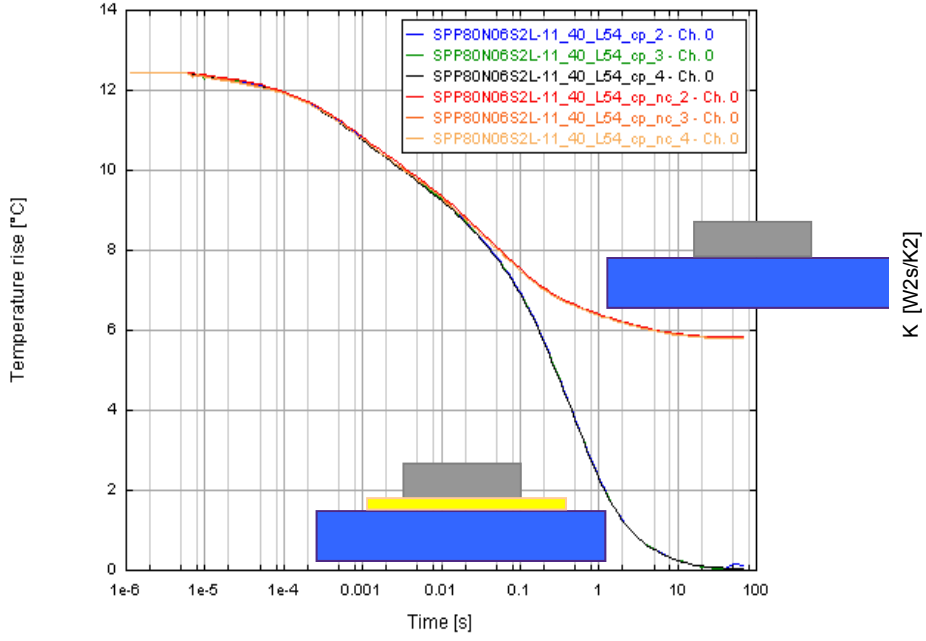


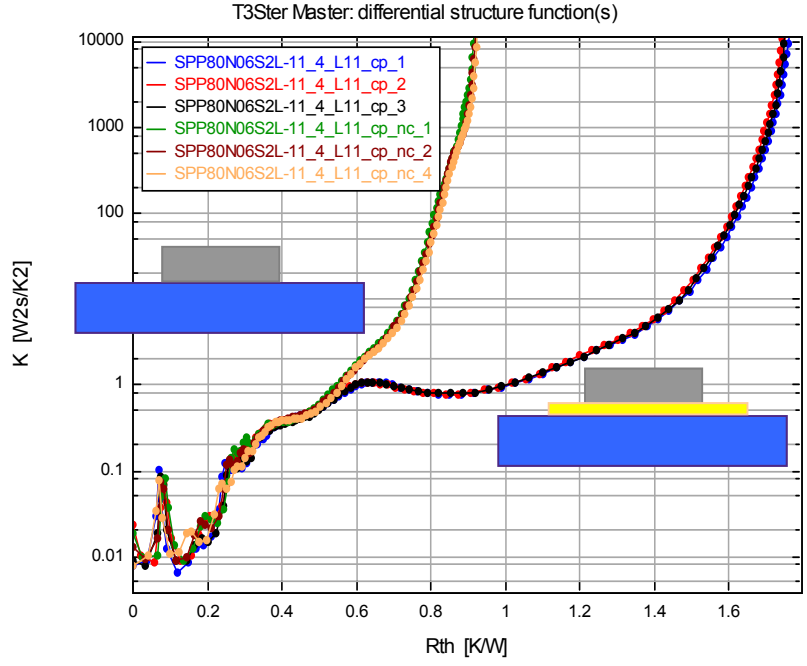
Change the quality of the thermal interface

Measurement of 2 setups (2x3 min), ***structure functions***

High accuracy and repeatability

- This type of R_{thJC} measurement provides high repeatability
  - the continuous measurement of thermal transients is very reliable and highly repeatable if the setup is not changed
  - repeatability is also high among different samples
  - structure functions are derived from the transients by a mathematically well defined numerical procedure, thus, resulting structure functions are also highly repeatable



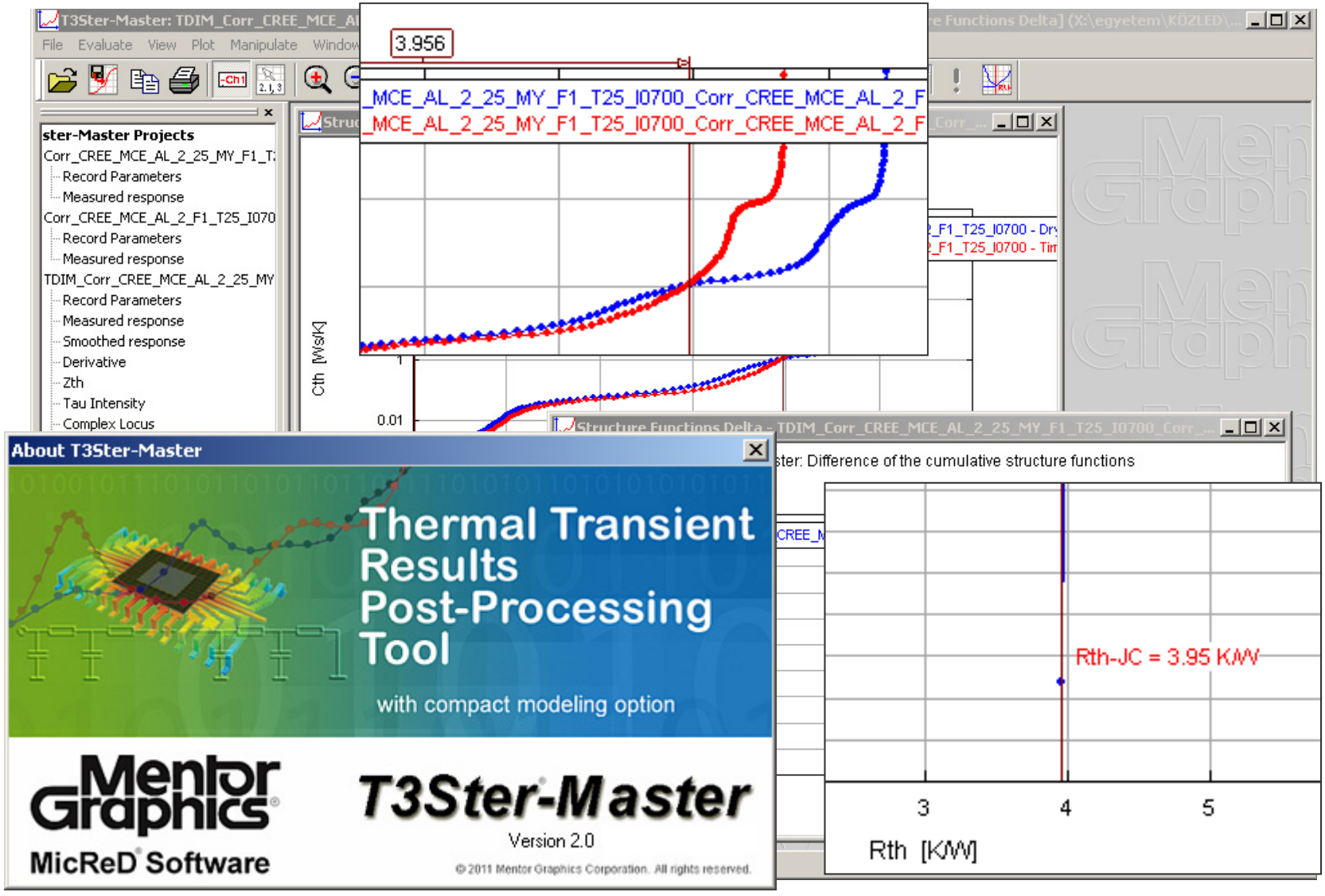


Mentor Graphics implementation of JESD51-14

- **The high accuracy thermal transient measurements** at two different qualities of the thermal interface of the power semiconductor packages is performed by the **T3Ster** equipment
  - Two measurements of the same device with two TIM qualities (wet and dry according to JESD51-14)
  - In case of LEDs emitted optical power is measured by TeraLED and it is considered in the heating power
- Divergence point of structure functions automatically found by T3Ster Master 2.0
- CTM exported from T3Ster Master 2.x to FloTHERM 9.2 and above
  - Extended JEDEC 2R models: the junction to bottom branch is considered by a transient model

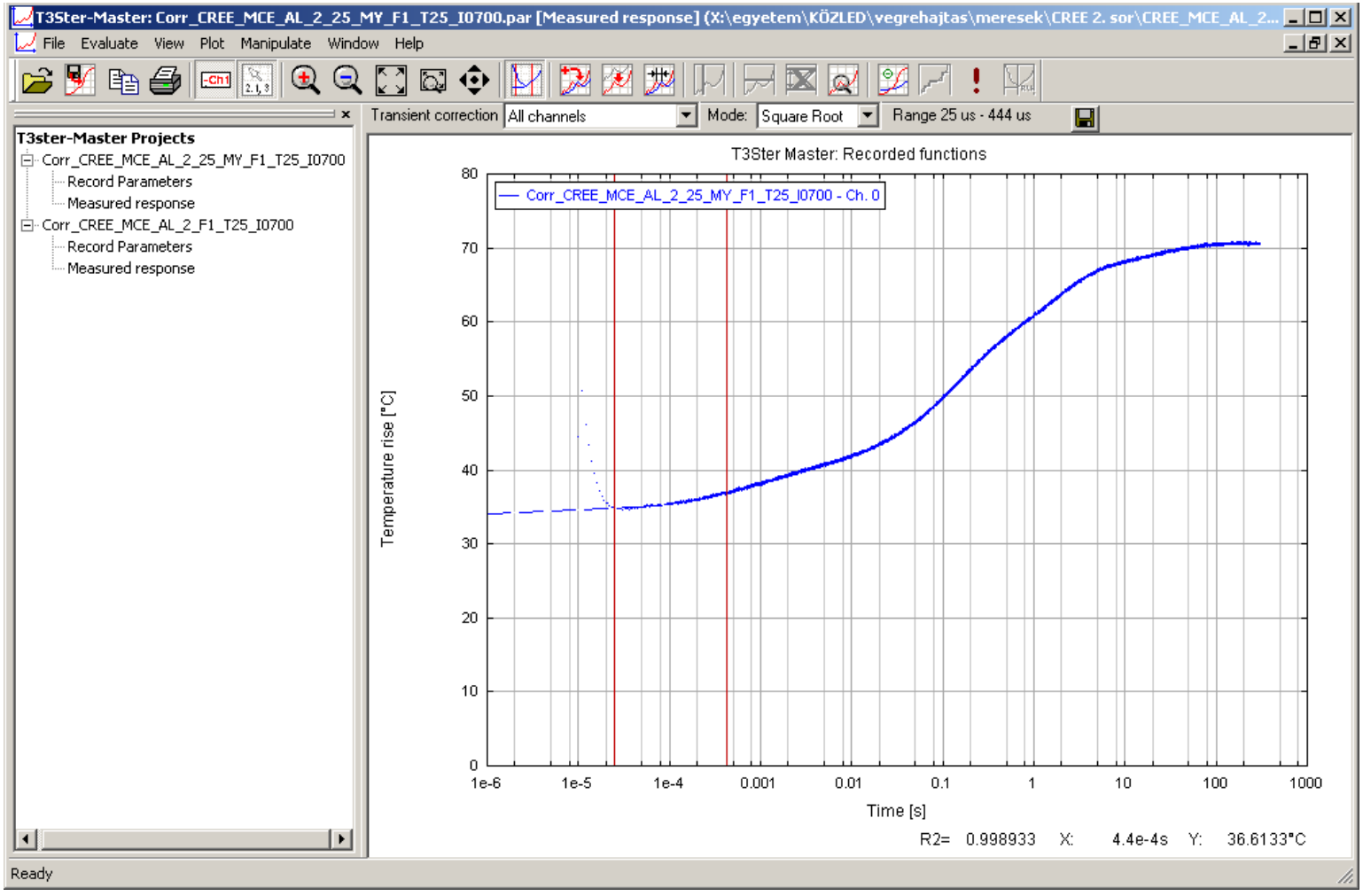
Mentor Graphics implementation of JESD51-14

- What was done manually before, is now fully automated:



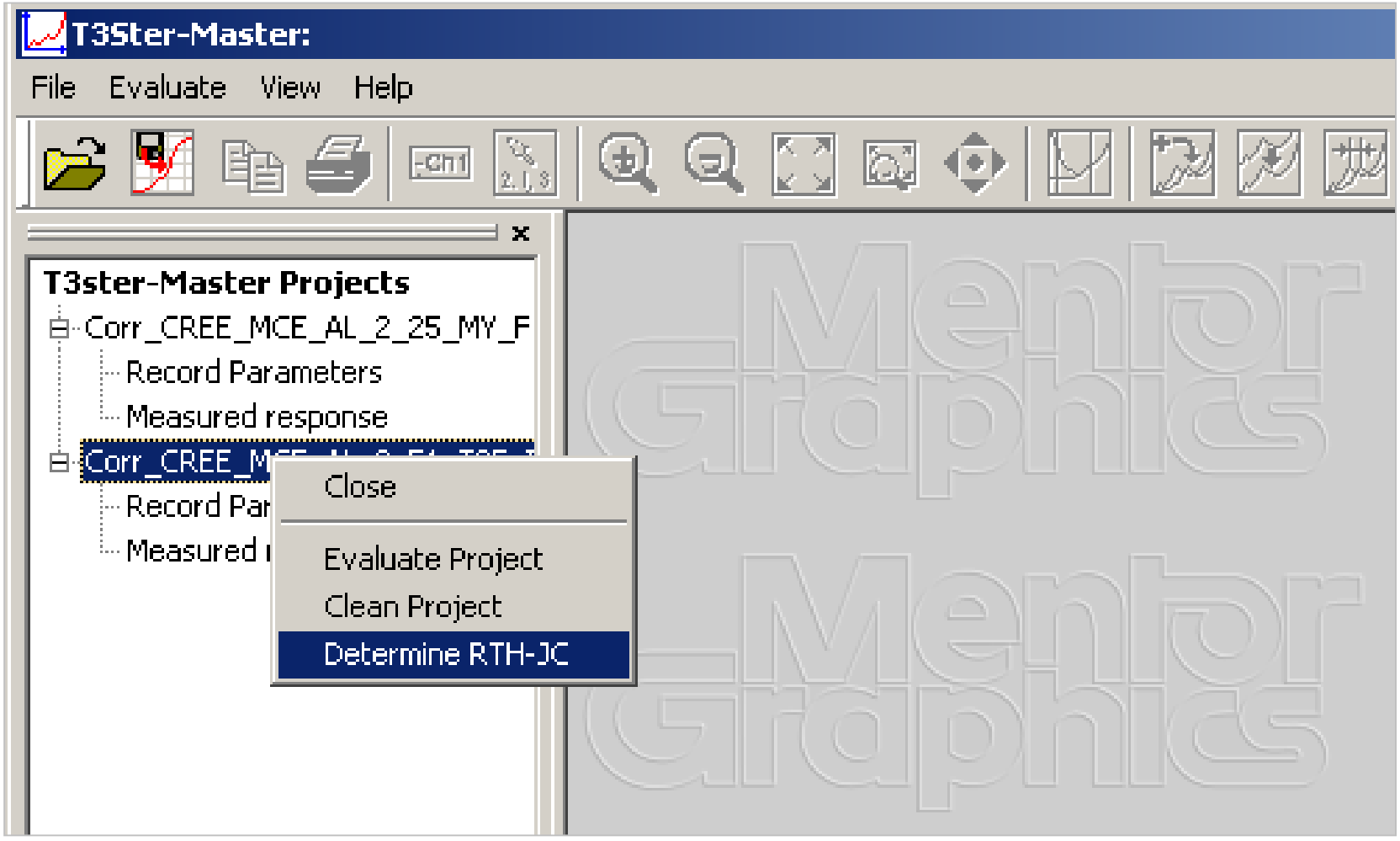
Find R_{thJC} in T3Ster Master 2.x as per JESD51-14

- The first step is getting rid of the initial electrical transients and completing the transient curve according to the standard



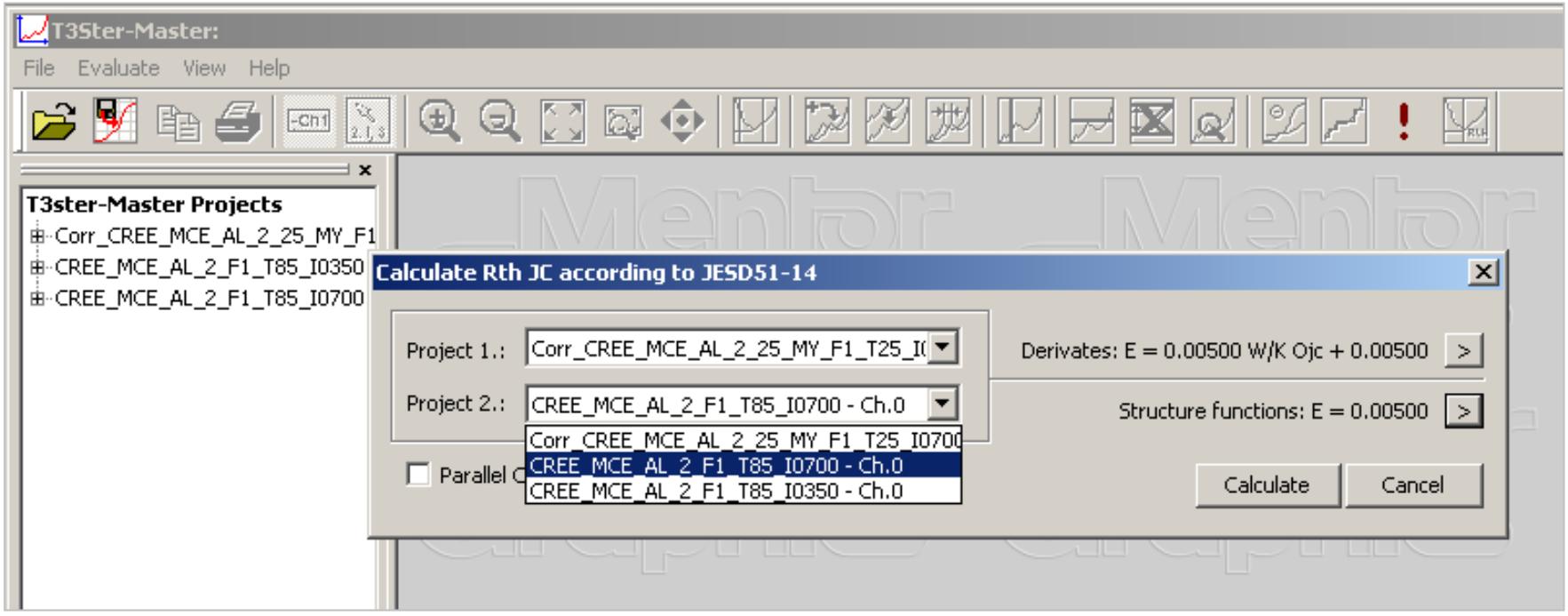
Find R_{thJC} in T3Ster Master 2.x as per JESD51-14

- After the correction of both measured transients (each for a given TIM quality), the process starts with a mouse click:



Find R_{thJC} in T3Ster Master 2.x as per JESD51-14

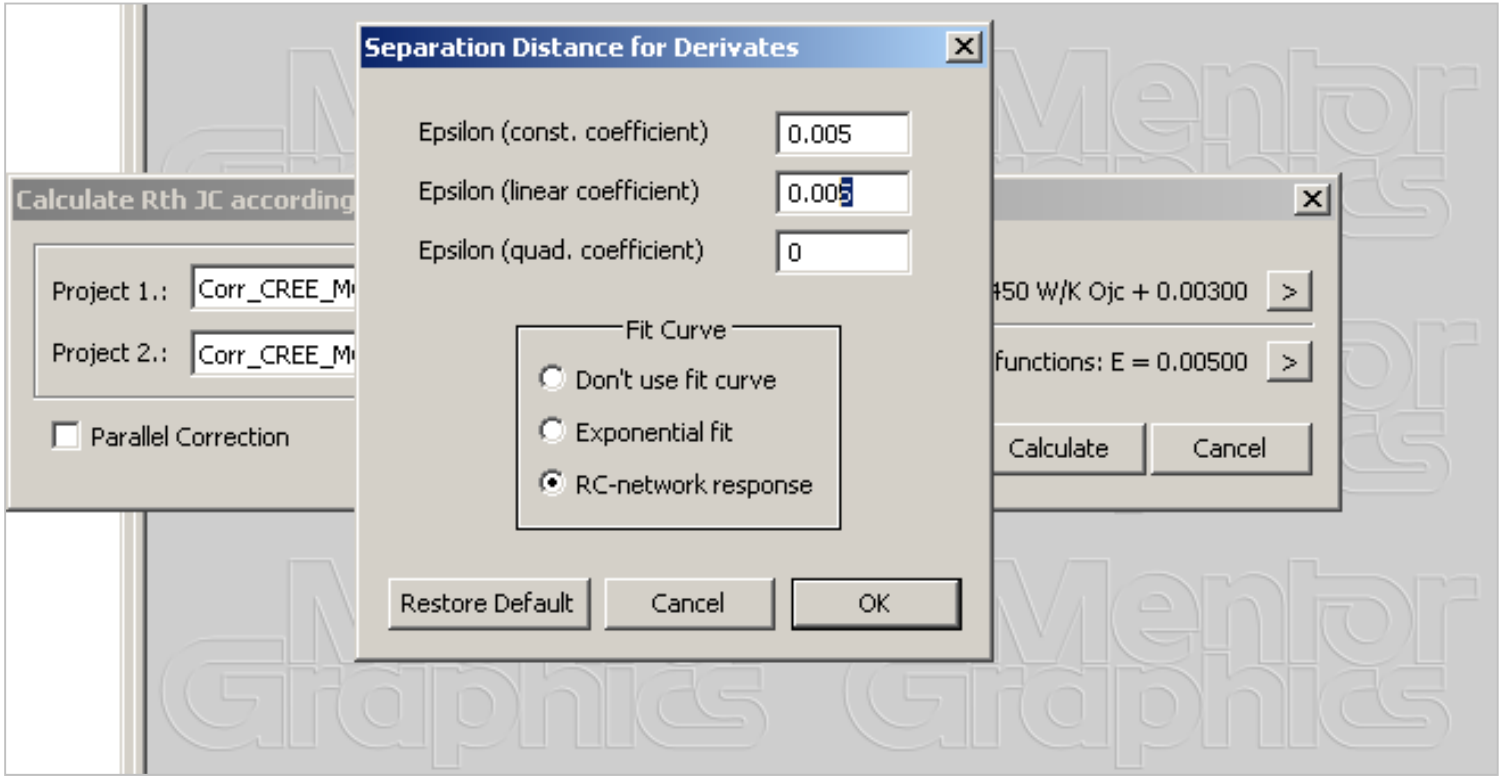
- The firs step is to define the two T3Ster measurements corresponding to the two TIM qualities:



The required projects can be selected easily

Find R_{thJC} in T3Ster Master 2.x as per JESD51-14

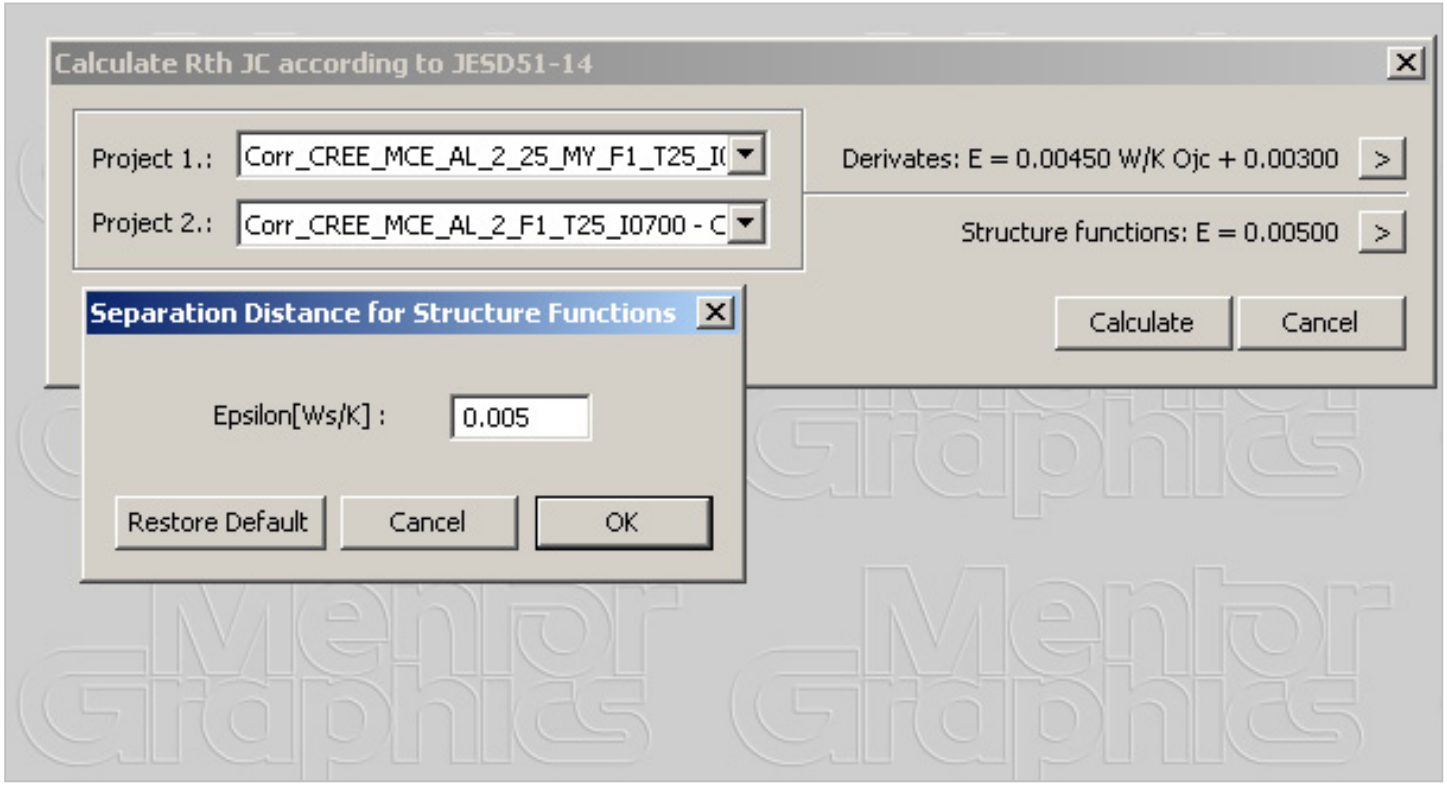
- The next step is to set the parameters for finding the divergence point of the two measurement results



Settings when R_{thJC} is to be calculated from the *derivatives of the measured transients*. Defaults would usually do.

Find R_{thJC} in T3Ster Master 2.x as per JESD51-14

- The next step is to set the parameters for finding the divergence point of the two measurement results

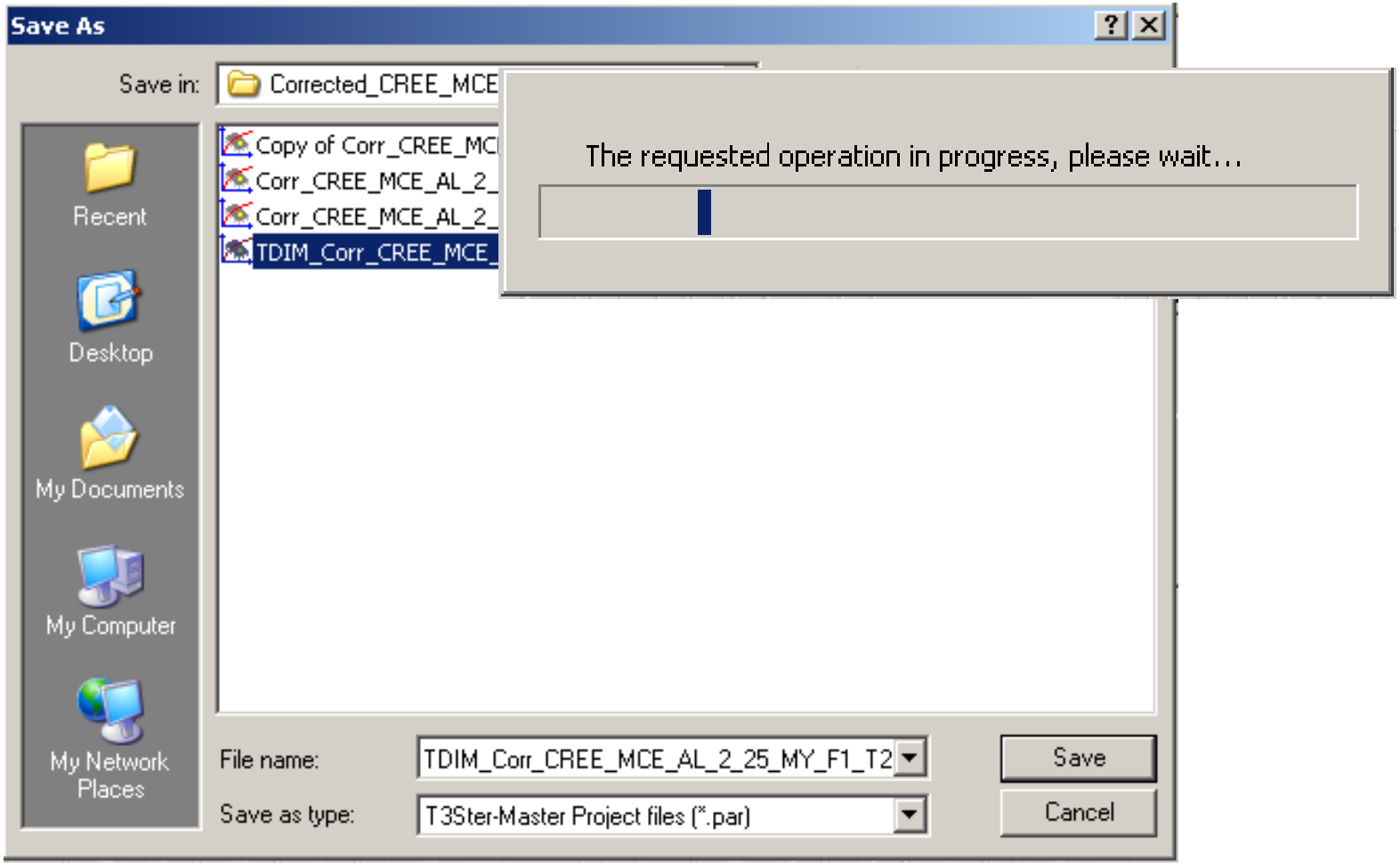


Settings when R_{thJC} is to be calculated from the *structure functions*. Default would usually do.

In this particular case we shall calculate R_{thJC} from structure functions.

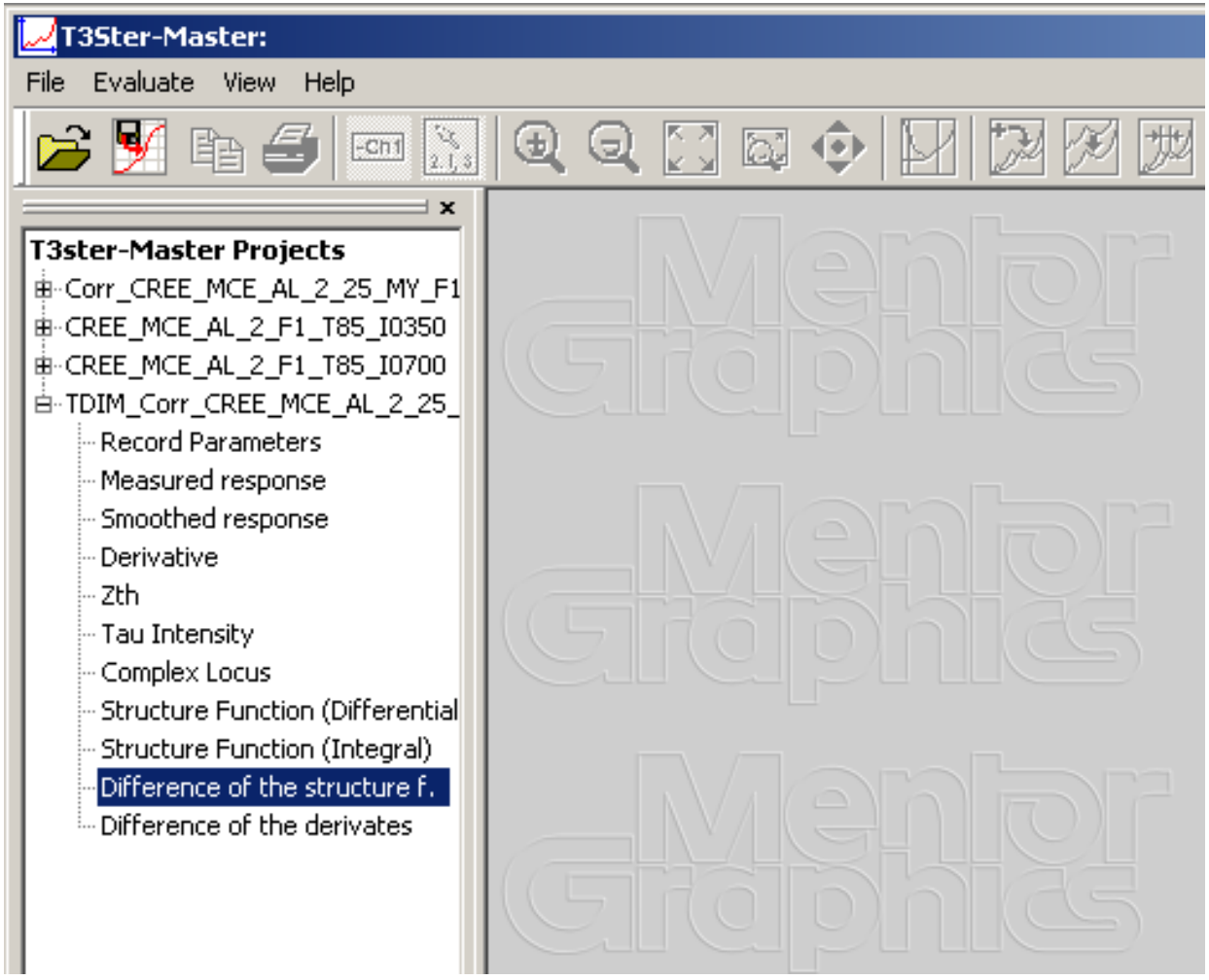
Find R_{thJC} in T3Ster Master 2.x as per JESD51-14

- After pressing the **Calculate** button, a new project for the results will be created, the two selected projects will be processed:



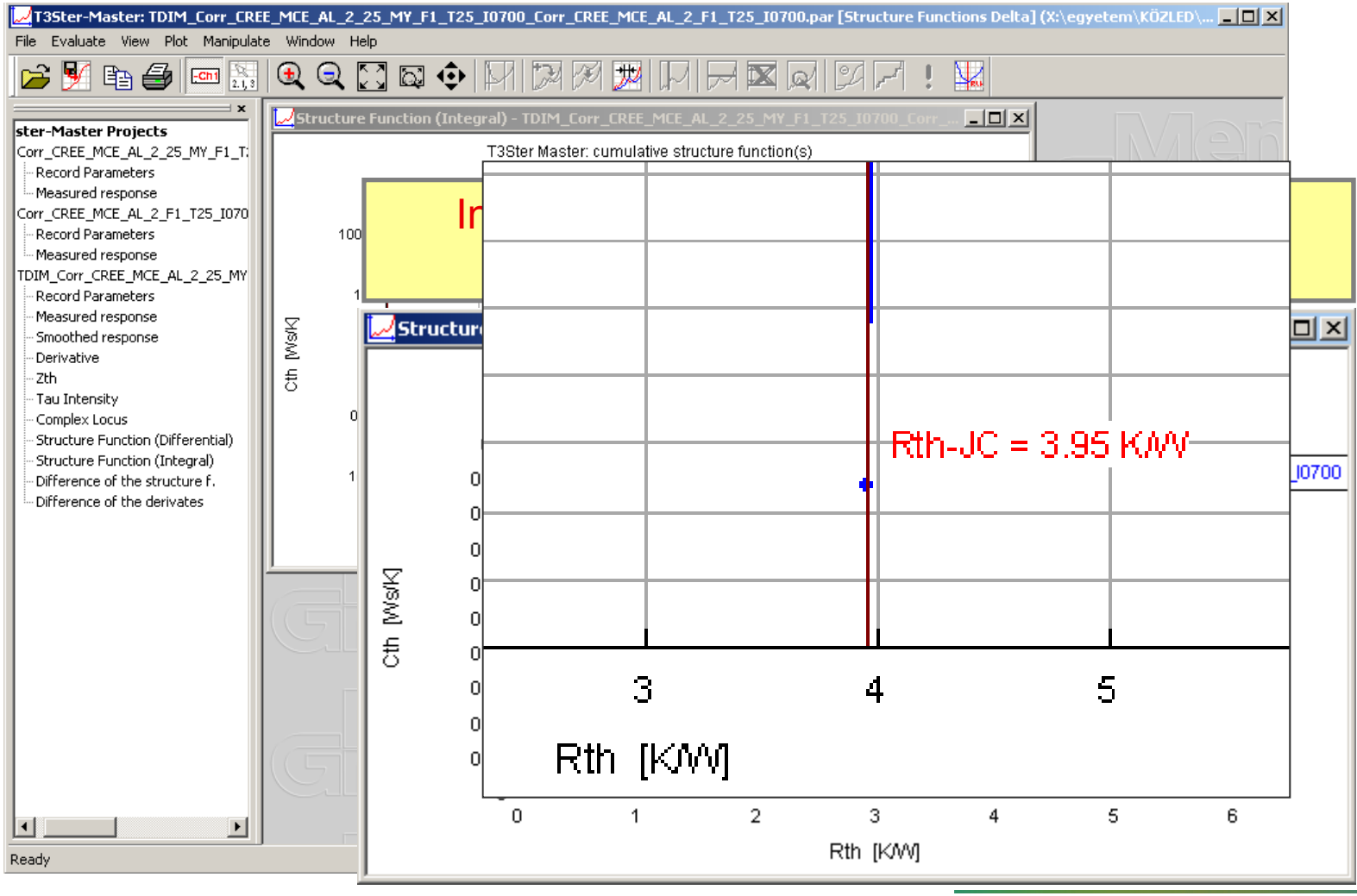
Find R_{thJC} in T3Ster Master 2.x as per JESD51-14

- The created new project will have two special views: *difference of derivatives* and *difference of structure functions*



Find R_{thJC} in T3Ster Master 2.x as per JESD51-14

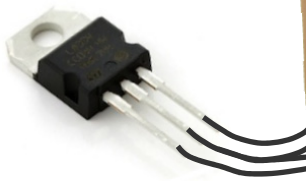
- An R_{thJC} value is shown both in the *difference of derivatives* and *difference of structure functions* view



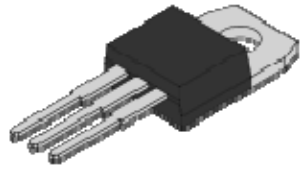
Supporting thermal modeling

Test based modeling and model validation

Real package

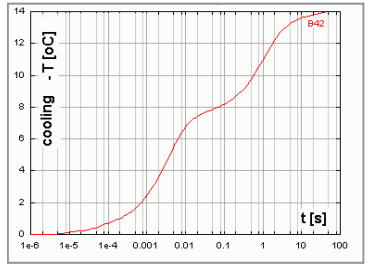


T3Ster



Detailed package model

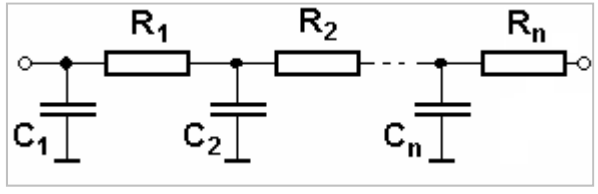
Thermal transient measured by ***T3Ster***



FloTHERM

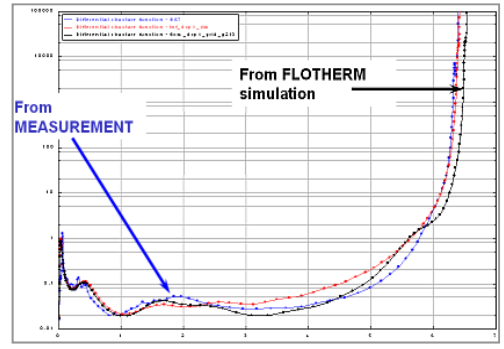
T3Ster software

Structure functions for test based compact model generation



FloTHERM

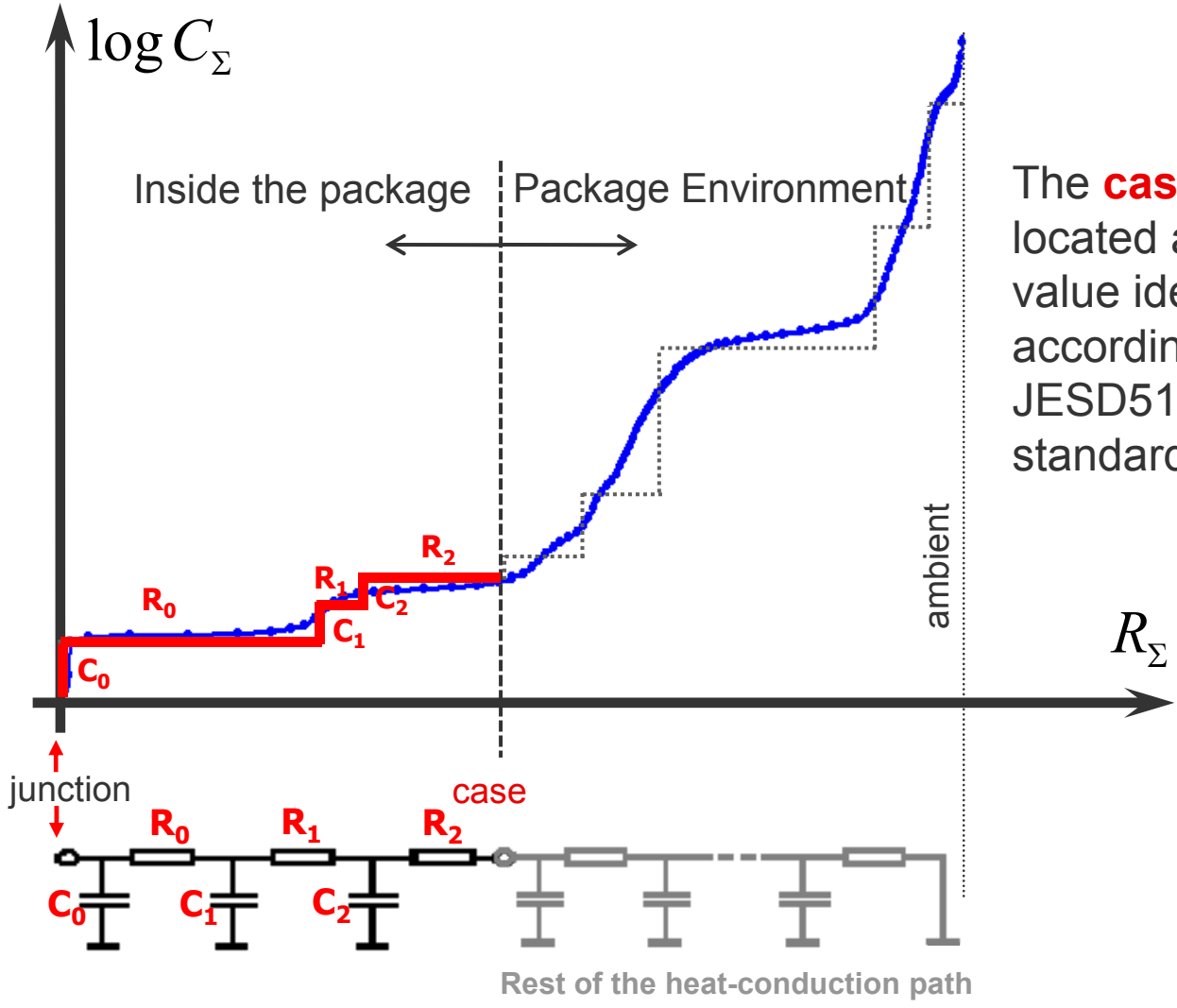
Structure functions for validation of detailed models



This model structure is characteristic to power semiconductor packages

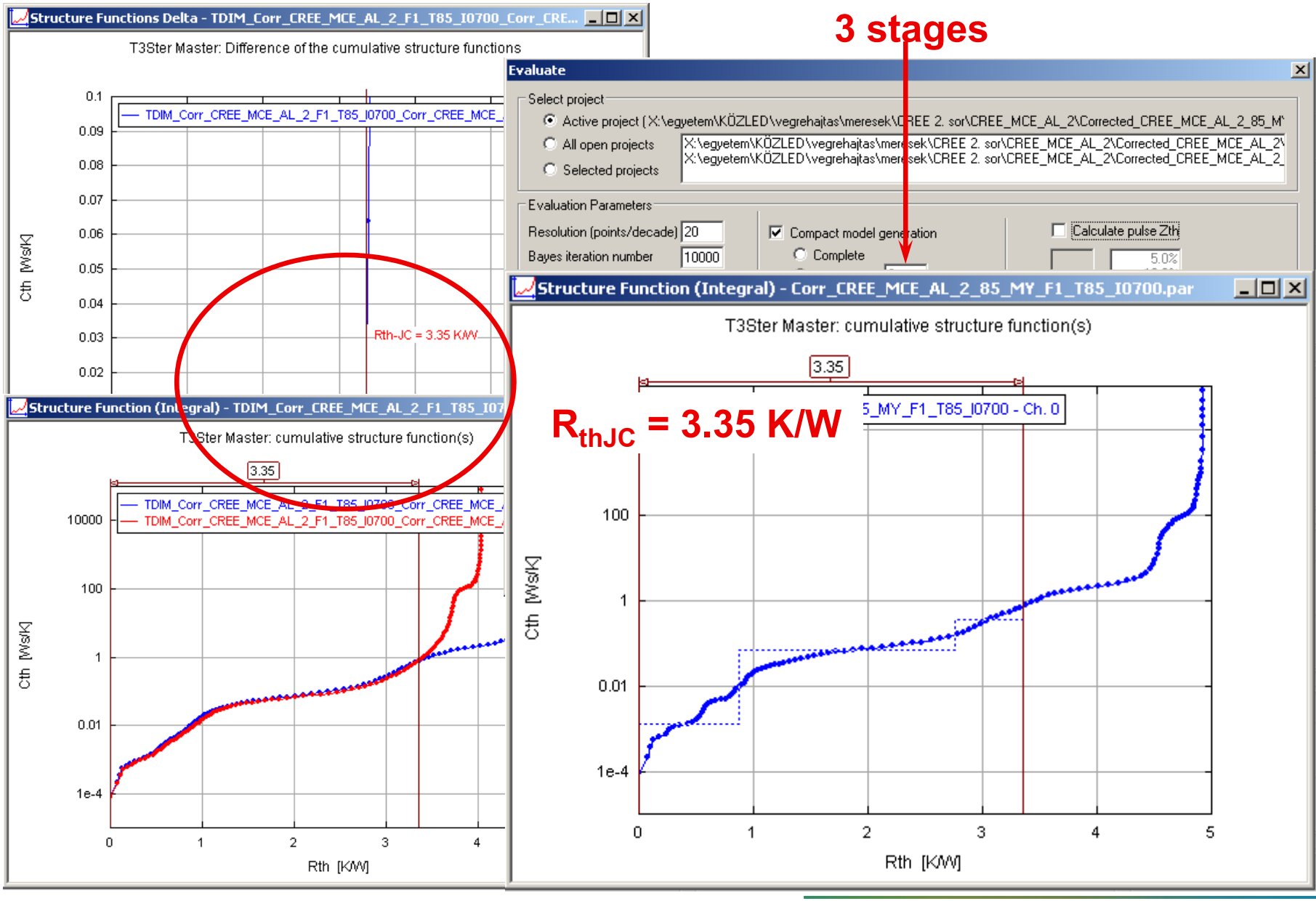
T3Ster Master → FloTHERM Interface

- Compact thermal model of the heat-flow path is created by a step-wise approximation of the structure function



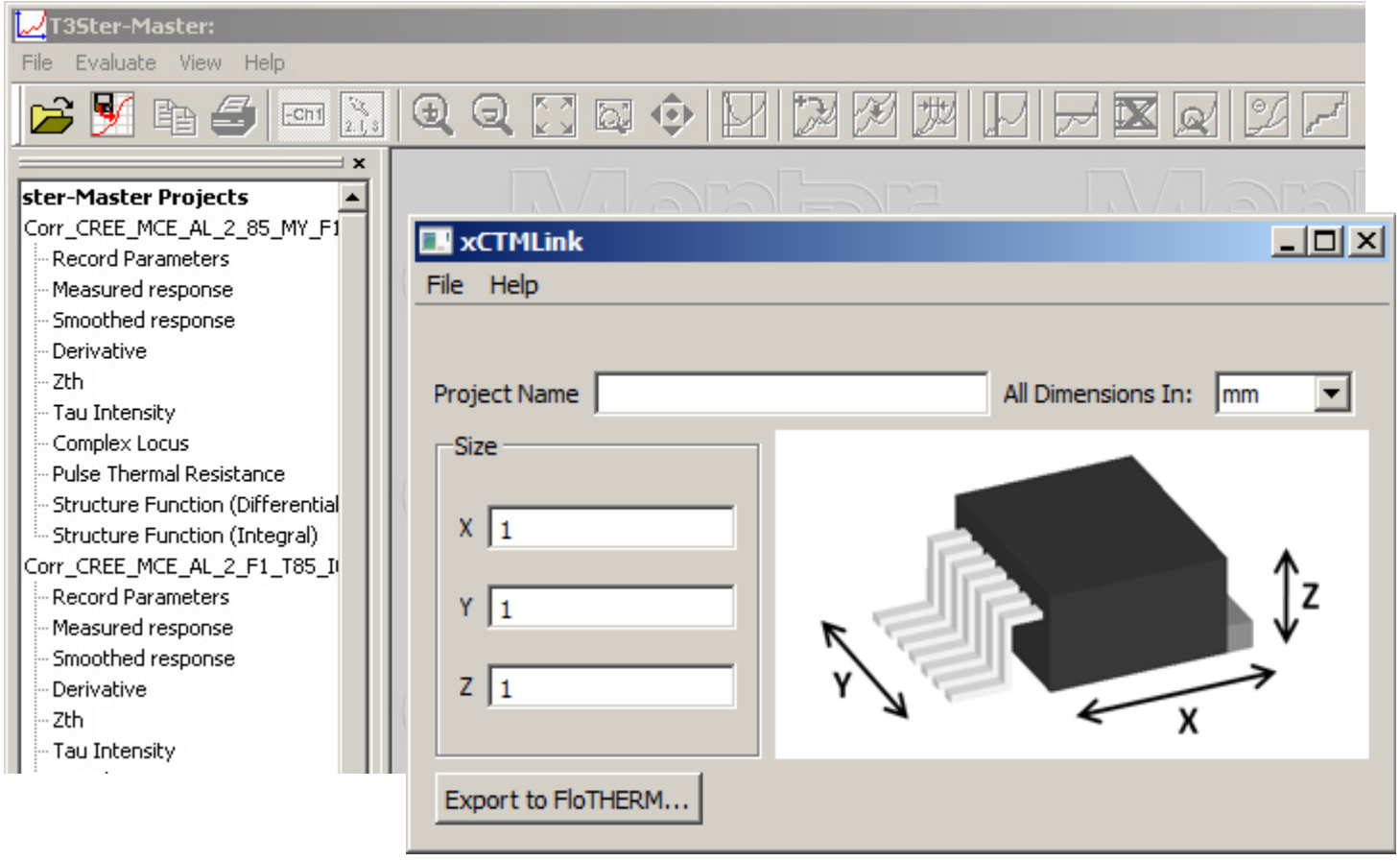
The **case** node is located at the R_{thJC} value identified according to the JESD51-14 standard

Creating compact models in general



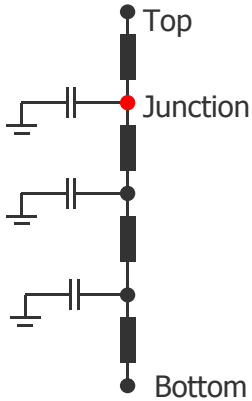
Creating compact models for FloTHERM

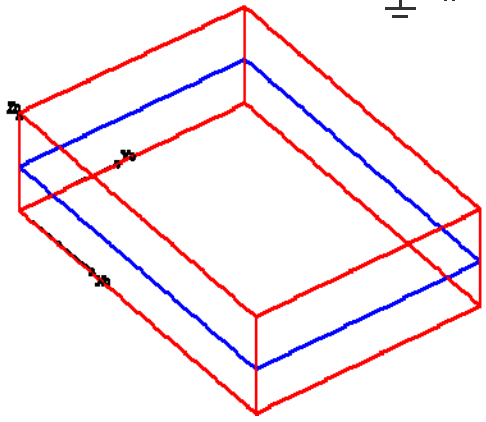
- Package geometry specified on file export from **T3Ster Master**

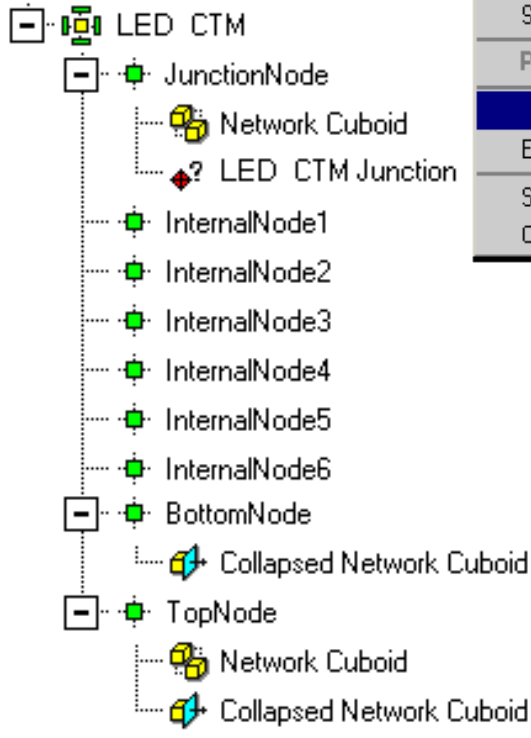


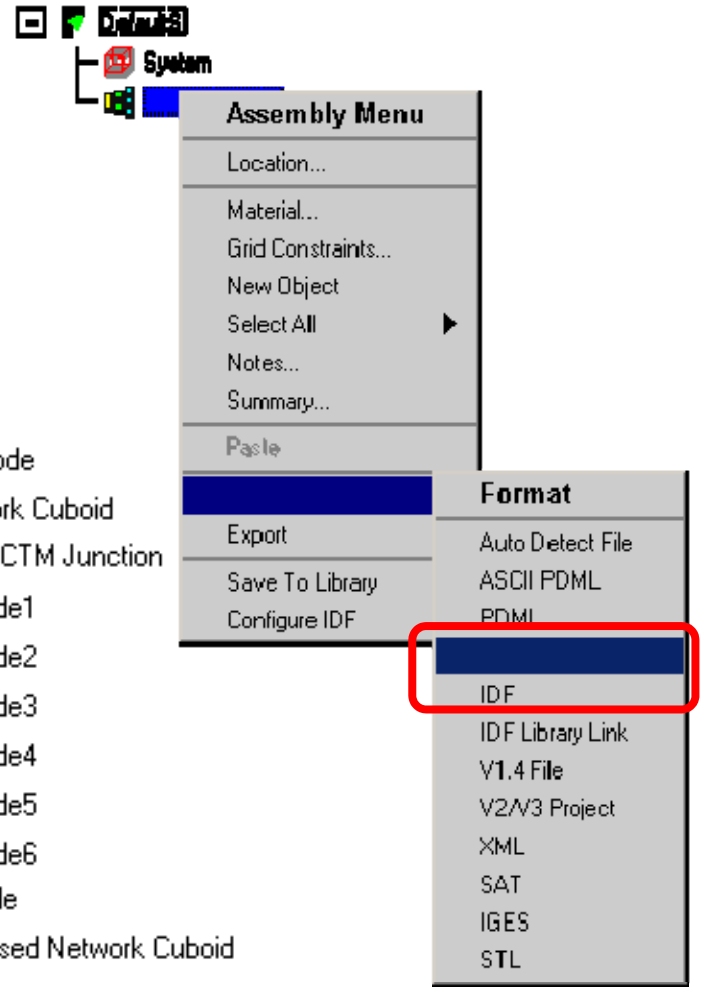
T3Ster Master ⟶ FloTHERM Interface

- Final step in FloTHERM:
  - File imported directly into FloTHERM
  - Resulting in an 'enhanced 2R' CTM defined as a 'Network Assembly' object





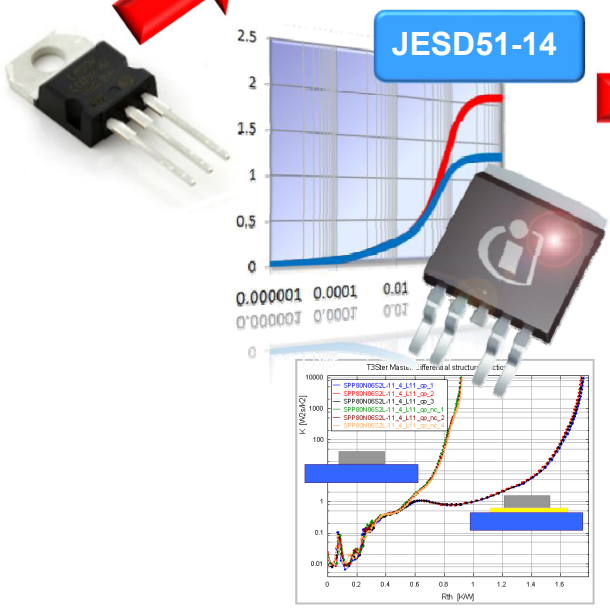




Benefits of the interface

- Simple and quick generation of thermal models based on real measurements (power packages only)
- The generated model shows exactly the same behavior as the real package
- No need to deal with modeling of TIM
- Quicker solution
- No need to exchange proprietary information between vendors and end-users as no detailed structural data is required for the model generation

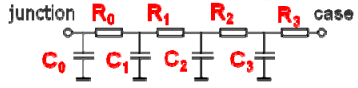
First and Unique Fully Automatic Measurement-Based Modeling of Power Semiconductor Packages



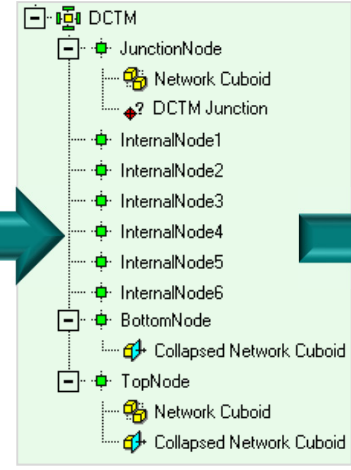
Heat flows from the junction directly to the cooling surface of the package.

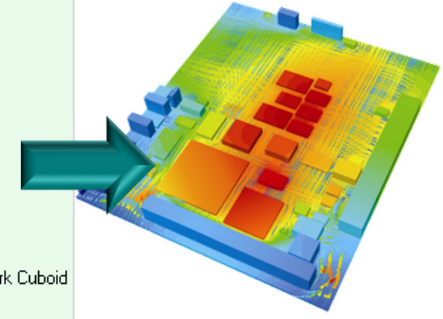
T3Ster Master Software

Model Creation



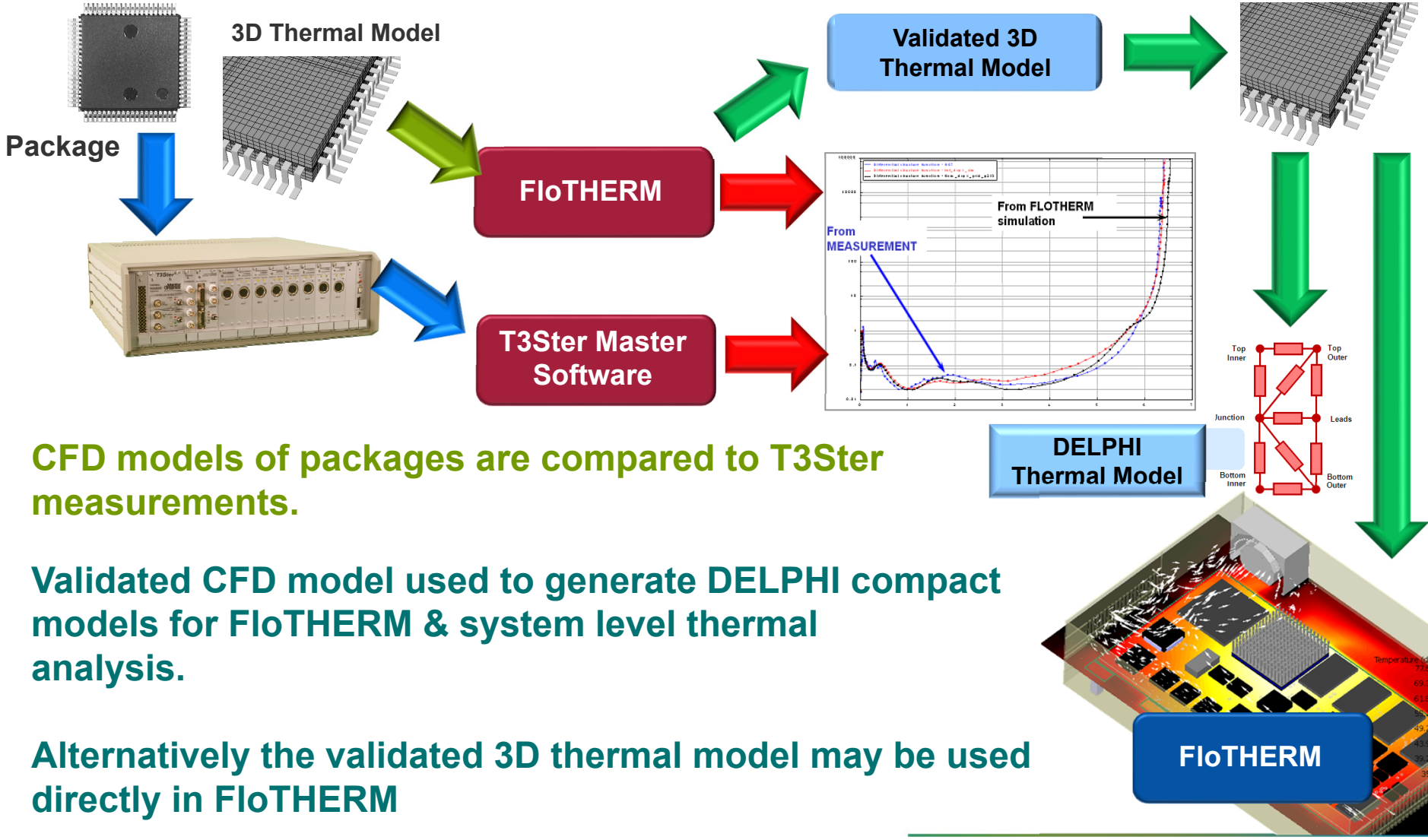
FloTHERM





JESD51-14 compliant RthJC measurements are automatically converted into compact thermal models used in FloTHERM.

First and Unique Measurement and Model Validation of IC Device Packages



CFD models of packages are compared to T3Ster measurements.

Validated CFD model used to generate DELPHI compact models for FloTHERM & system level thermal analysis.

Alternatively the validated 3D thermal model may be used directly in FloTHERM

DEMO

Identification of R_{thJC} of the package measured before, using the JEDEC JESD51-14 method implemented in T3Ster Master

Mentor Graphics®

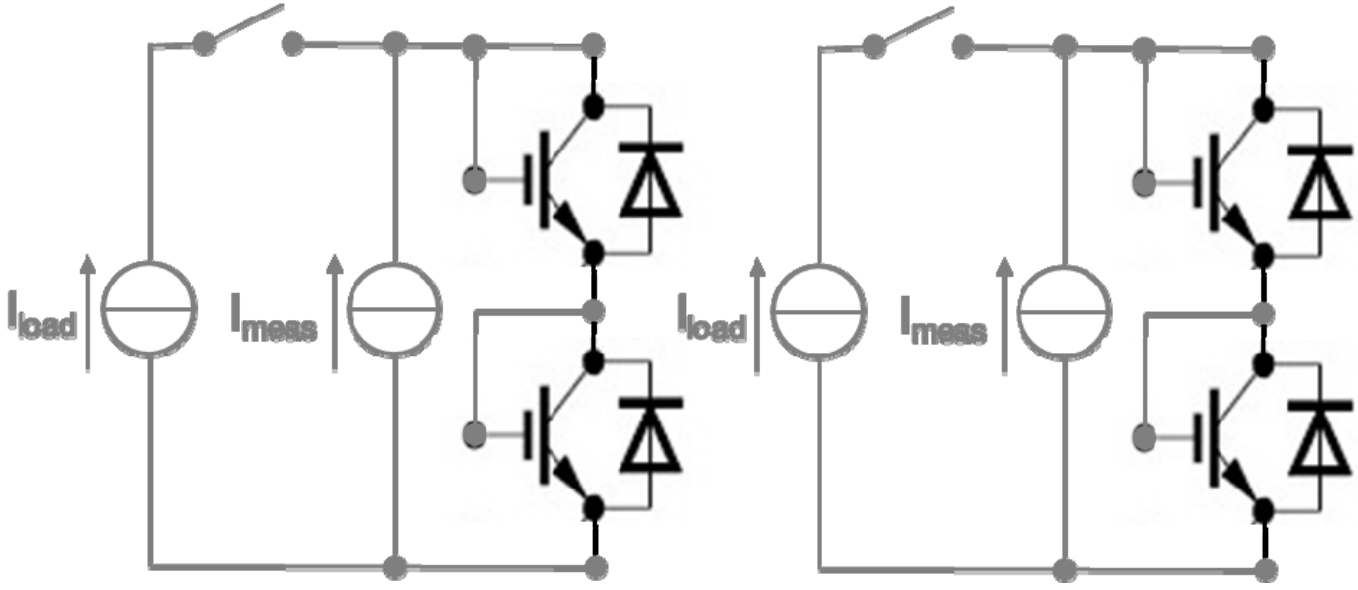
Modeling and industrial QA analysis of IGBTs and other power component in the 1500 A … 3000 A range

Testing an IGBT module with kW level of power

- In power electronics industry both proper thermal design and reliability analysis of components such as IGBT modules is needed
- These tests need to be performed under realistic conditions
  - 500 A … 1500 A … 3000 A of current needs to be supplied
  - This results in multiple kW-s of heat to handle (needs proper cooling)
- MicReD industrial testing series of solutions
  - Test conditions meet industrial requirements
    - Powering
    - Cooling
    - Safety
  - Automated tests
    - Setup
    - In-situ degradation monitoring
    - Stop criteria

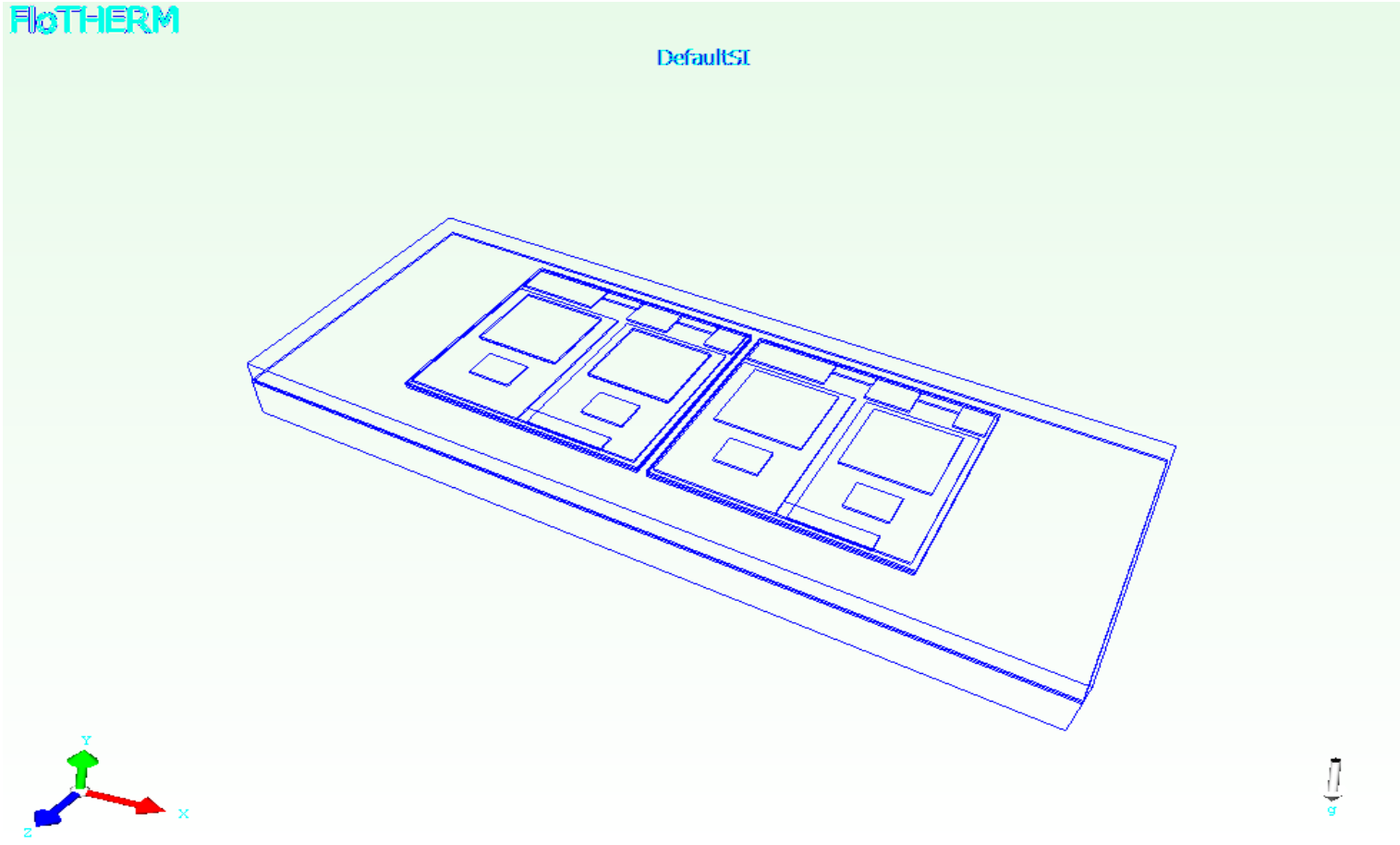
Test conditions for the half bridge modules

- Devices mounted on a cold-plate with highly stable thermal pad
- Gate and drain electrodes interconnected
- Common powering, but each device connected to a T3Ster channel

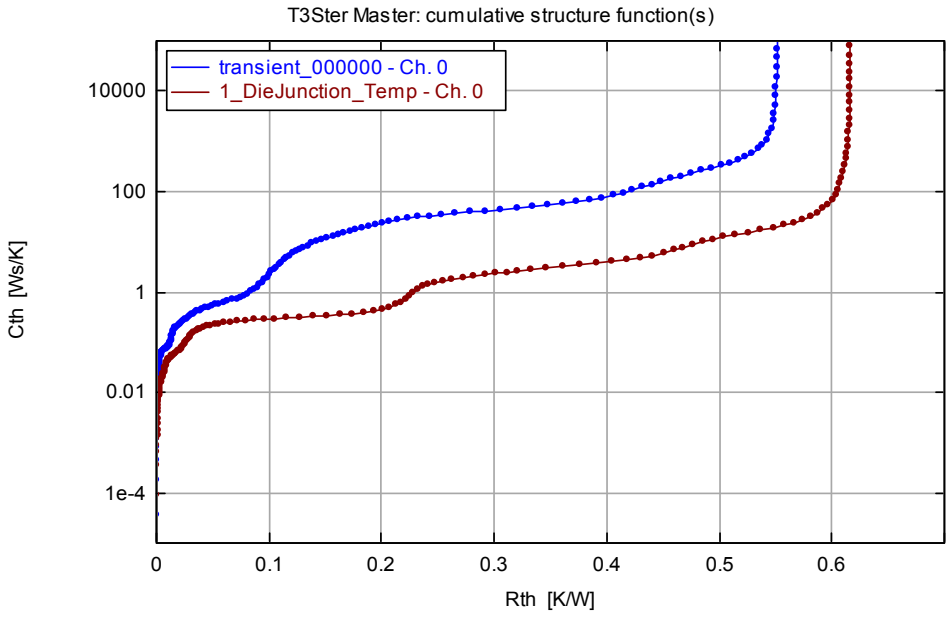


Simulation of temperature distribution

- Model built up, calibrated and simulated in FloTHERM and in FloEFD



Model calibration

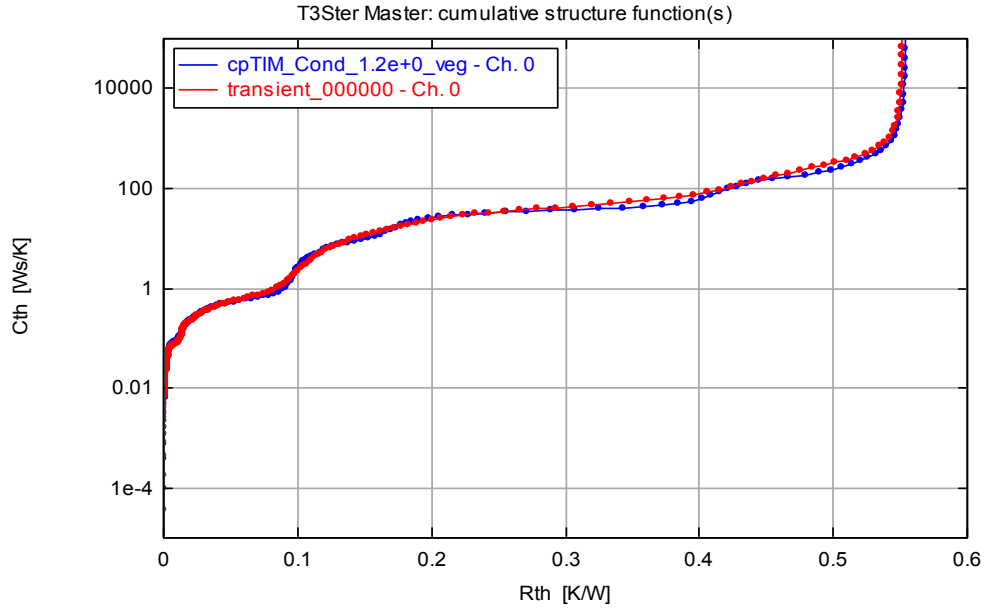


Initial model

Calibration steps:

1. Die material parameters
2. Die-source geometry
3. Die attach resistance
4. Conductivity of the ceramics
5. TIM between copper and cold-plate

Calibrated model



Automated process in FloTHERM v11.

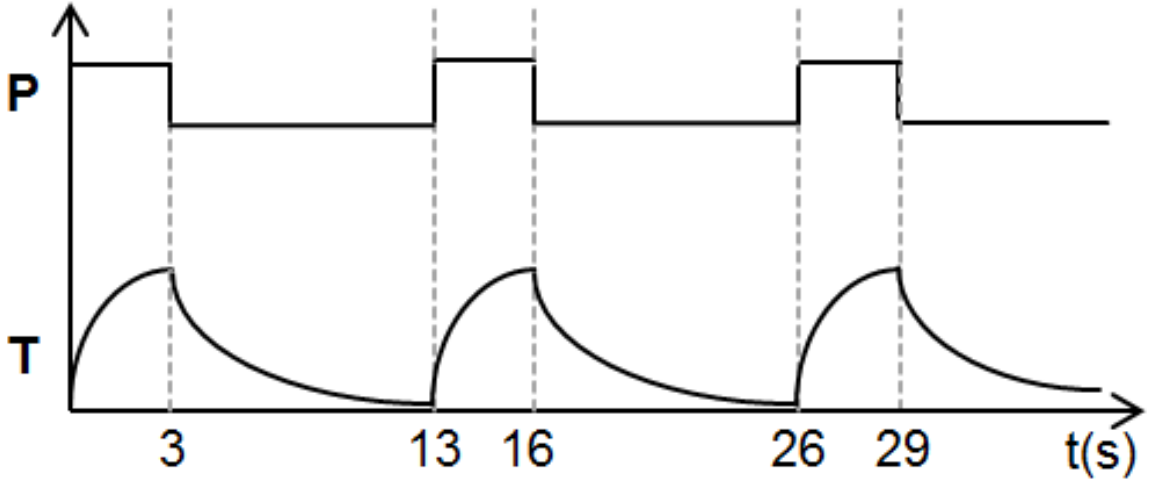
Learn about this in detail in Mentor Graphics' workshop

How to Automatically Calibrate FloTHERM Package Models and Improve Thermal Design Reliability

15 March 2:00 p.m. - 3:00 p.m. (Fir)

Powering conditions

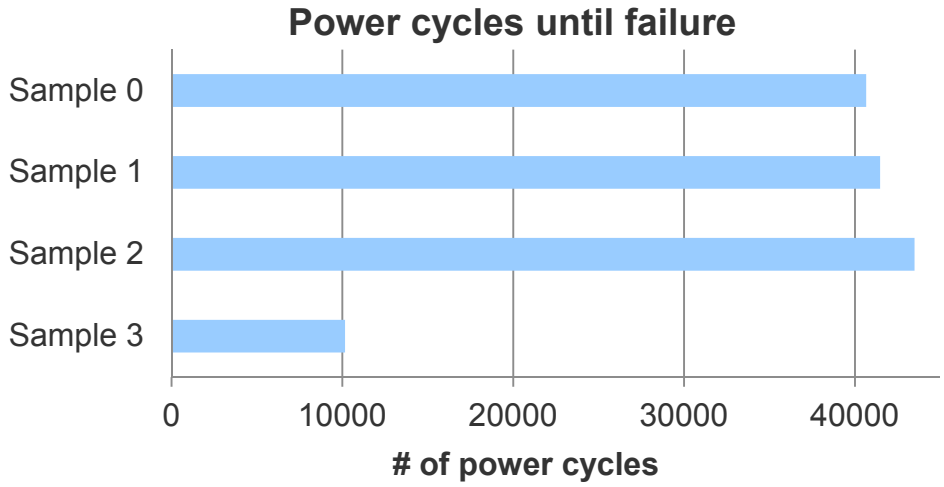
- Base plate temperature: 25° C
- Targeted junction temperature: 125° C
- Input power: 200W @ 25A

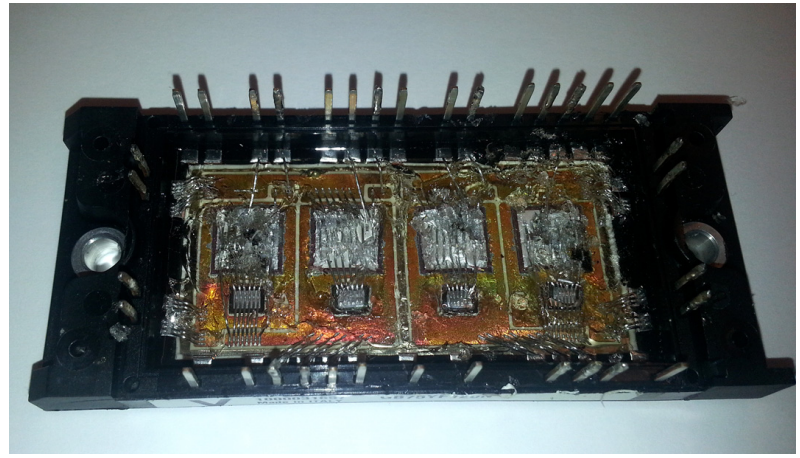


- **Cor** **change**
- Tra

Results of the reliability tests

- The power cycling was conducted until the total failure of the IGBT-s





Failures identified by visual inspection

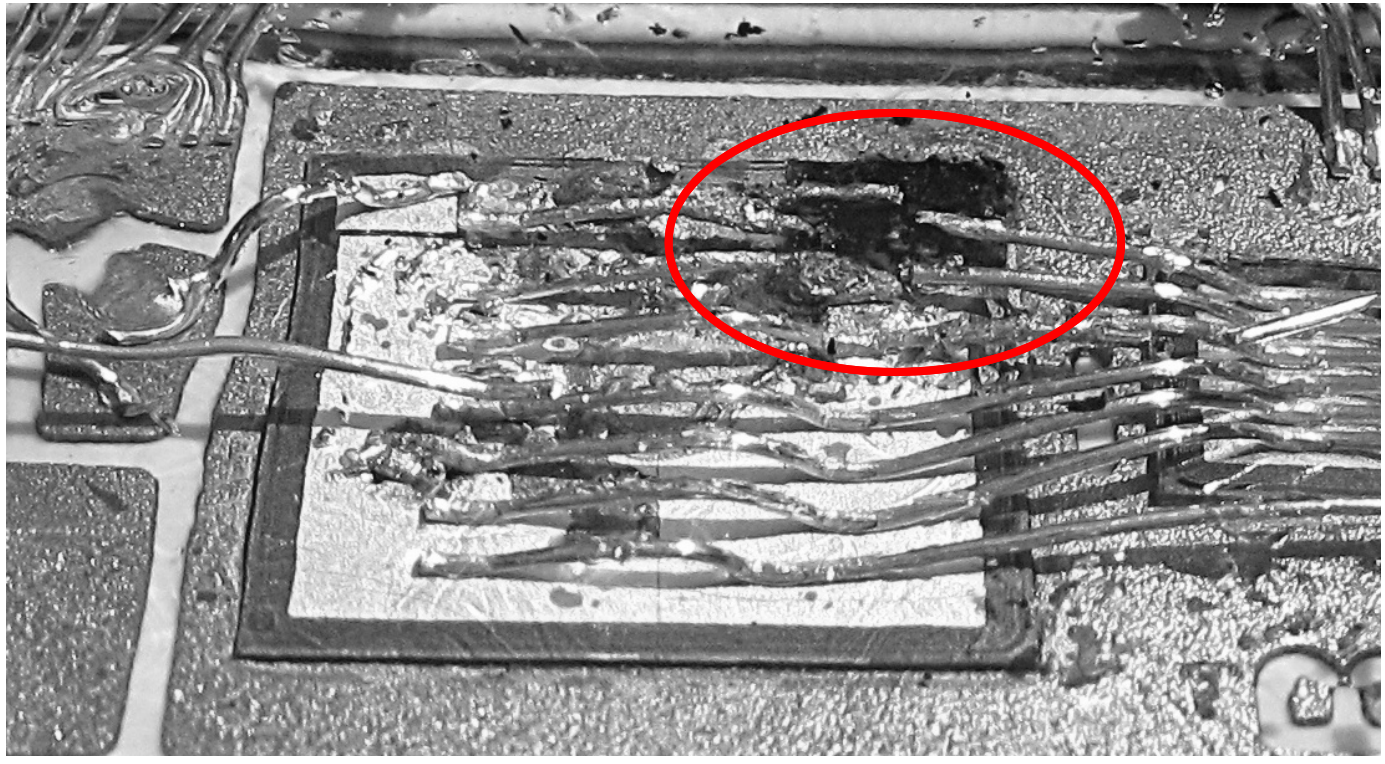
- Broken bond-wires and burnt areas on the chip surface
- In face all IGBT-s failed due to the overheating and damage of the gate-oxide

Further failure analysis

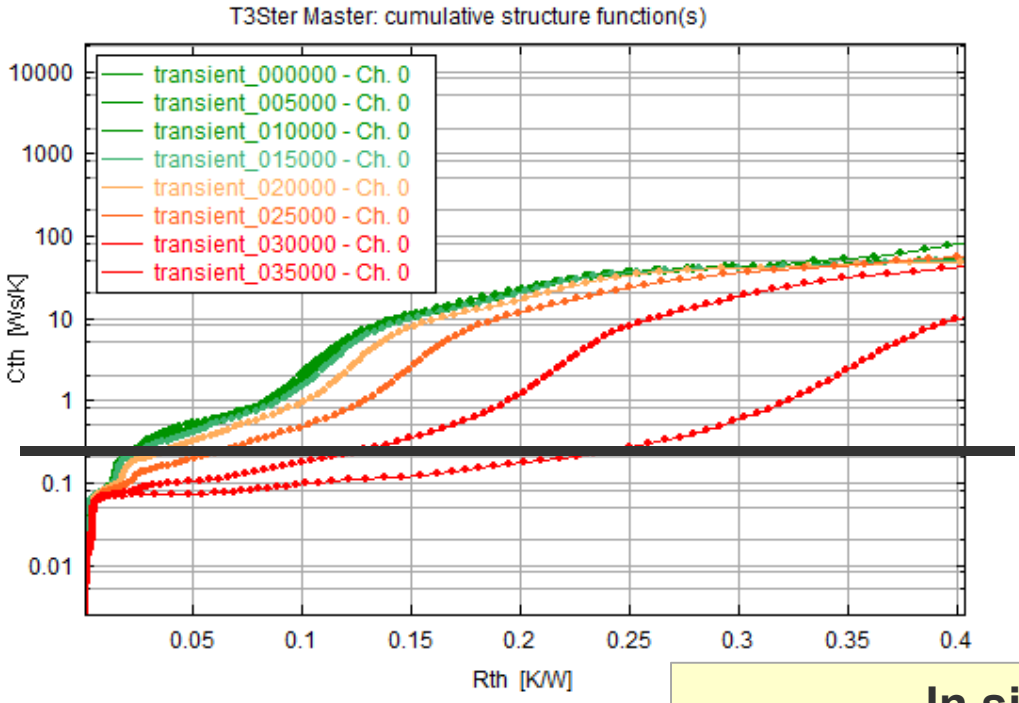
- Structure functions obtained in situ during power cycling

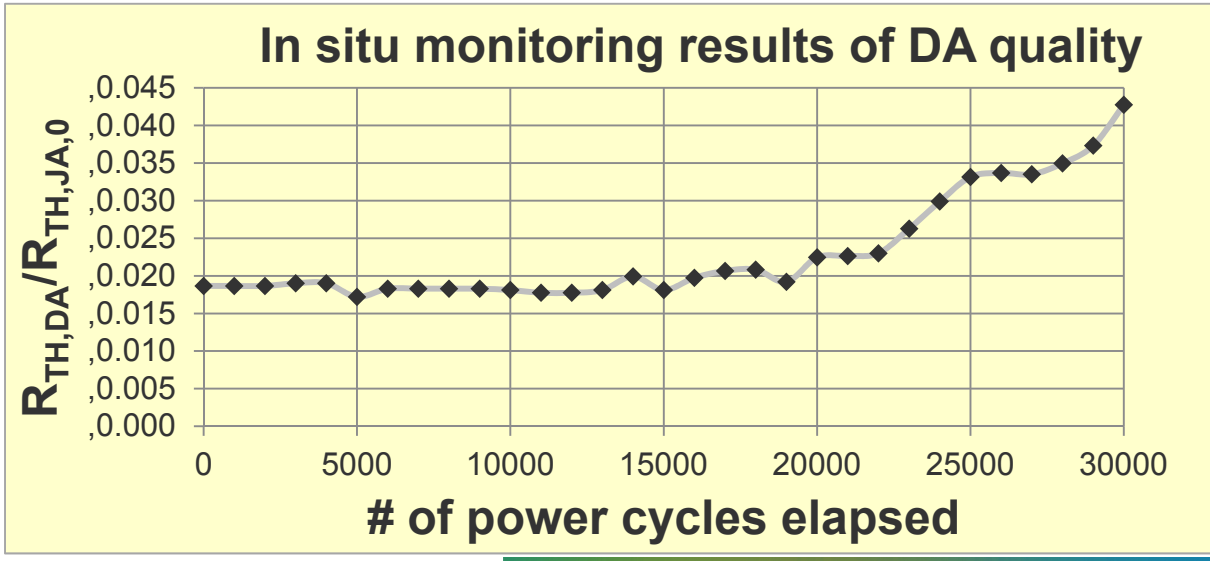
Results of visual inspection

- Broken bond-wires and burnt areas on the chip surface
- In face all IGBT-s failed due to the overheating and damage of the gate-oxide



Structure functions showing die-attach degradation





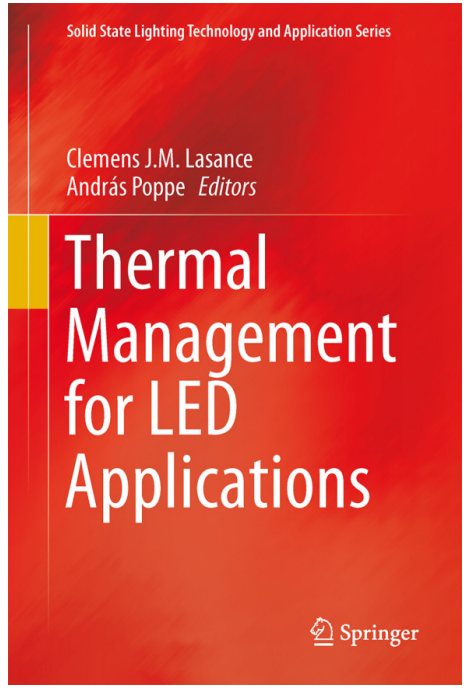

STOP

Further information

Recommended reading:

- For more details and references of the topics covered in this course please refer to

  Chapter 4 **Thermal Testing of LEDs** (G. Farkas, A. Poppe) of a recent book C.J.M. Lasance – A. Poppe (eds): **Thermal Management for LED Applications**, September 2014, **Springer**



http://www.springer.com/engineering/electronics/book/978-1-4614-5090-0