Si and Non-Si Nanotechnologies and their Benchmarking

Robert Chau

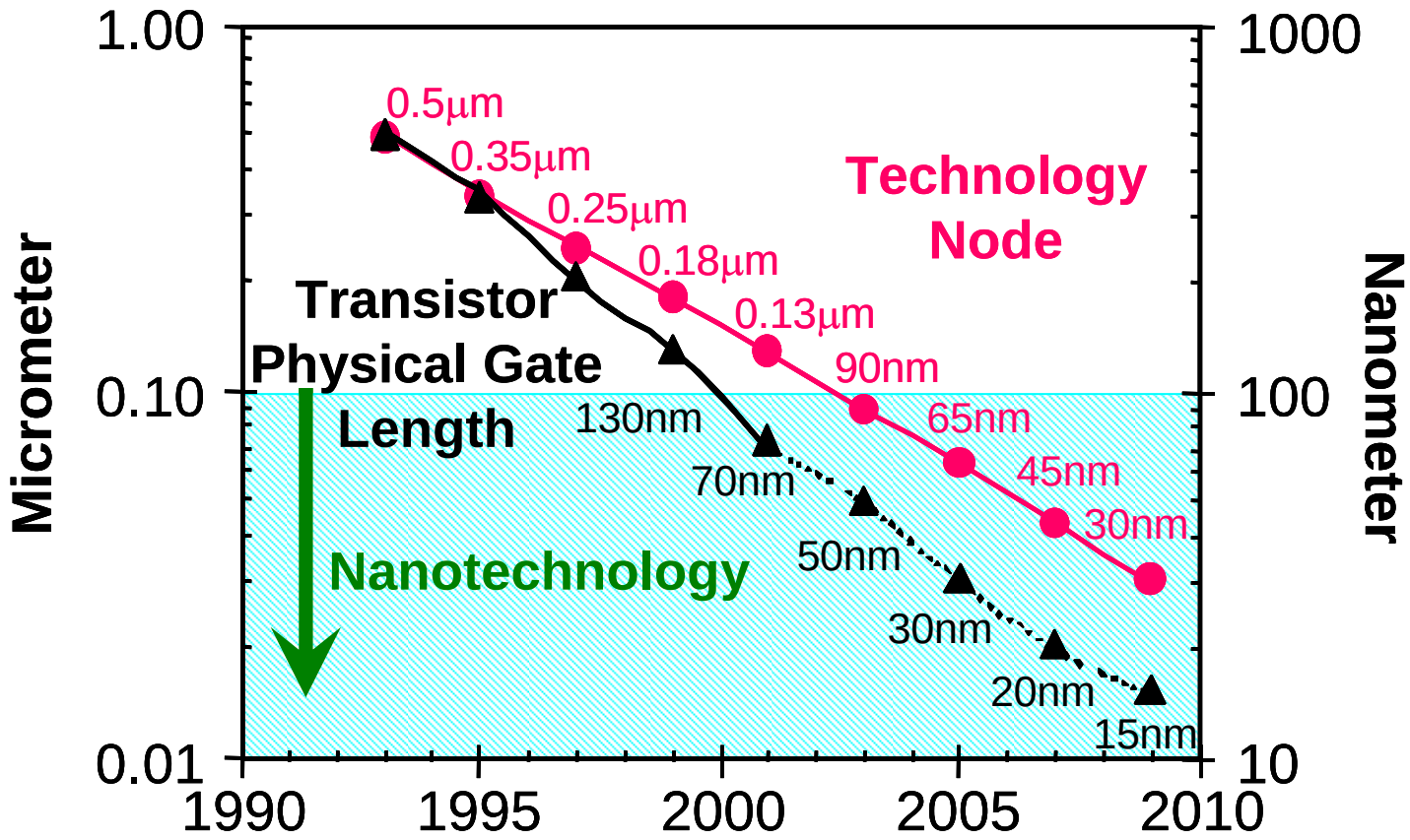
Intel Fellow
Director of Transistor Research and Nanotechnology
Technology & Manufacturing Group
Intel Corporation

April 25, 2005

Content

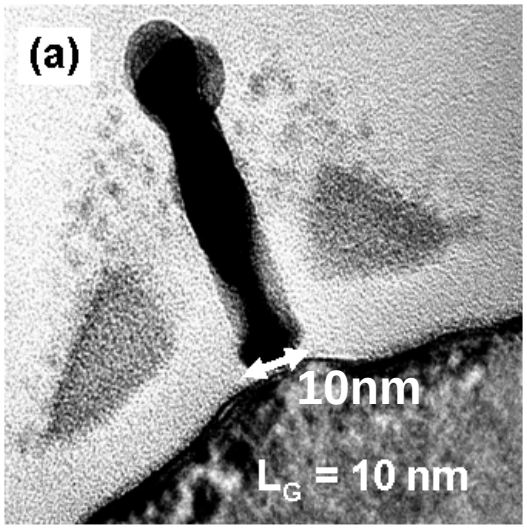
- Introduction
- Benchmarking metrics
- Benchmarking methodology
- Benchmarking results
- Summary

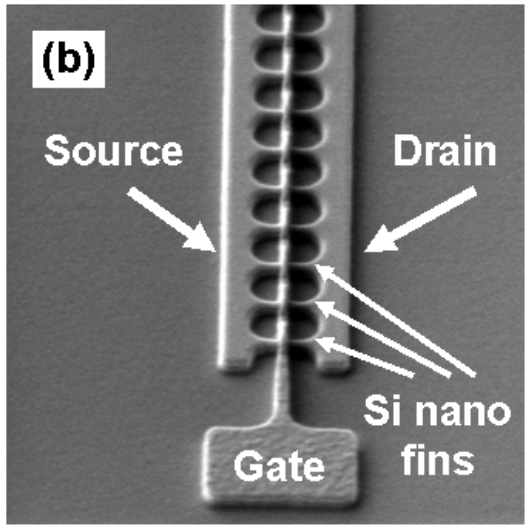
Transistor Scaling



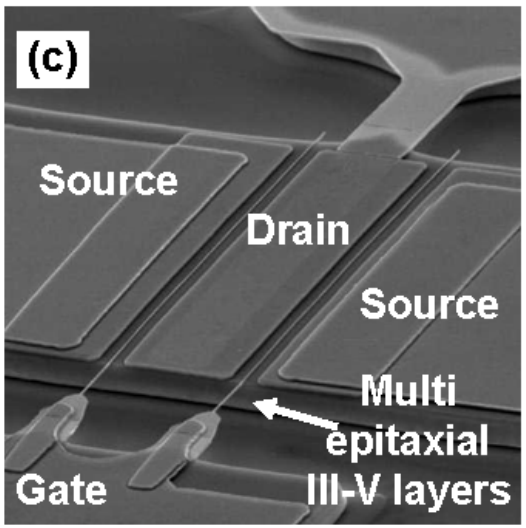
Transistor physical gate length will reach ~15 nm before end of this decade, and ~10 nm early next decade

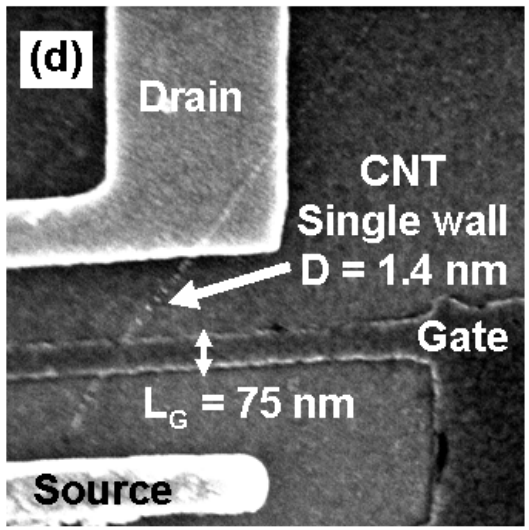
Emerging Nanoelectronic Devices

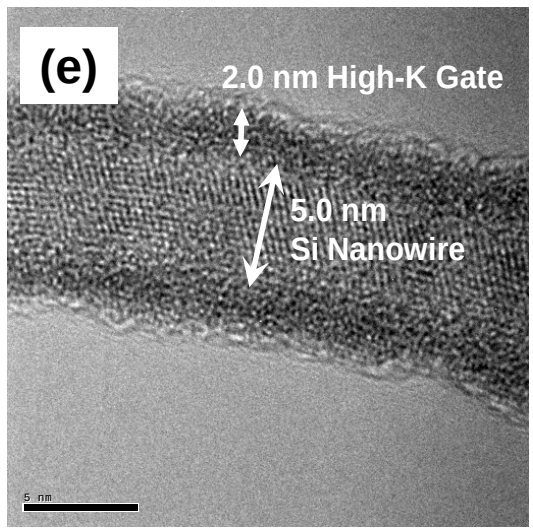




- (a) 10nm L_G Si MOSFET
- (b) Non-planar Si Tri-gate
- (c) III-V QWFET
- (d) CNT FET
- (e) Si nanowire FET







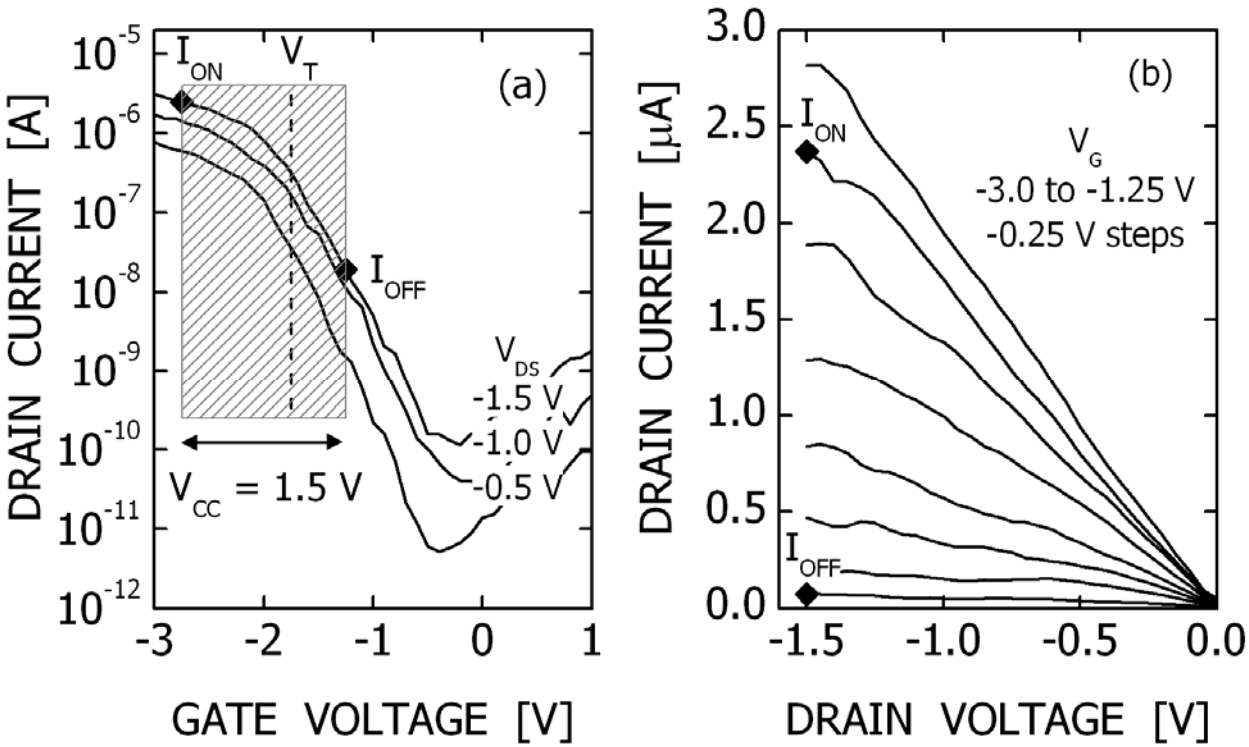
Benchmarking Metrics

- Benchmark emerging nanoelectronic devices against state-of-the-art Si devices
  - Separate reality from hype
  - Identify device strengths and shortcomings
  - Gauge research progress

- 4 key device metrics
  - CV/I vs L_G -- Intrinsic speed
  - Energy-Delay product vs L_G -- Switching energy
  - Subthreshold slope vs L_G -- Scalability
  - CV/I vs I_{ON}/I_{OFF} -- I_{OFF} vs speed tradeoff

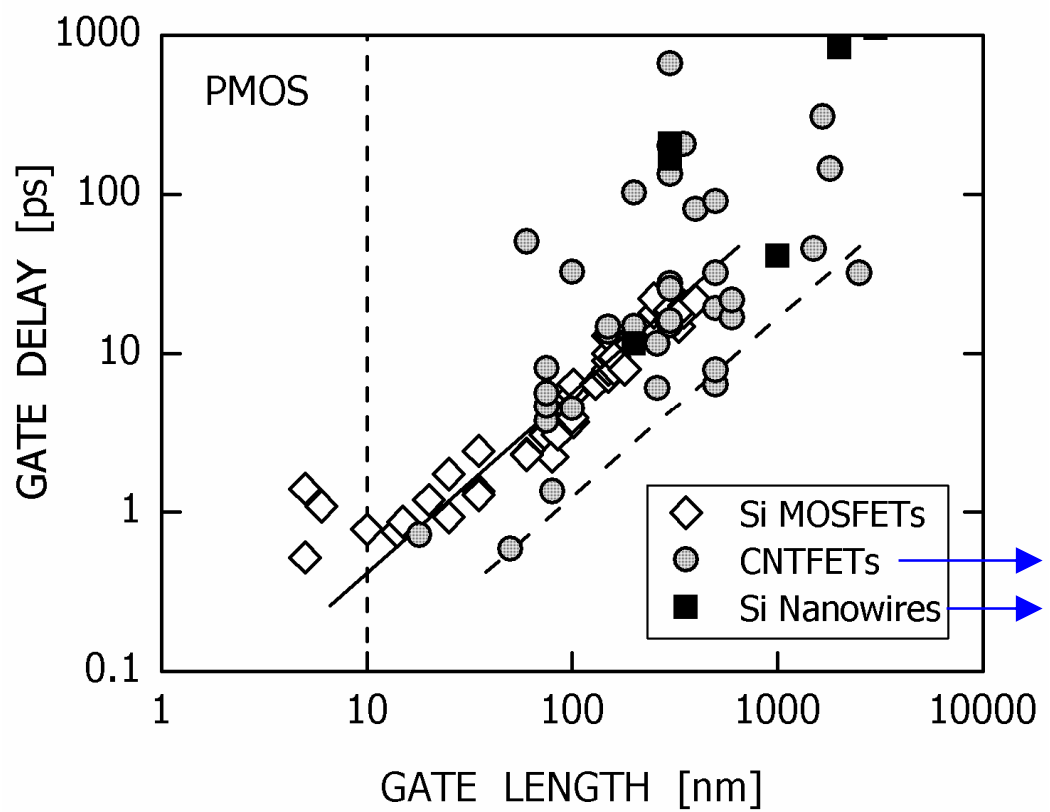
Low CV/I and high I_{ON}/I_{OFF} required for logic applications

Benchmarking Methodology



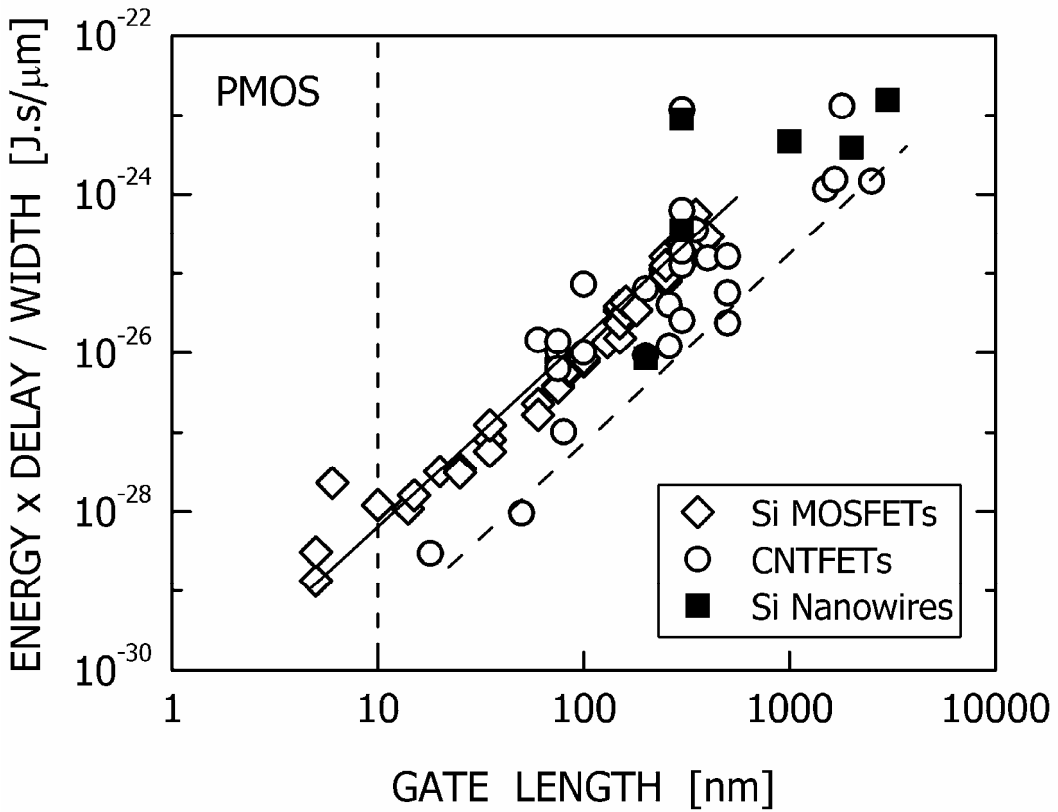
- $I_{ON} = I_{DS}$ at $|V_{DS}| = V_{CC}$ and $|V_G – V_T| = 2\ V_{CC} / 3$
- $I_{OFF} = I_{DS}$ at $|V_{DS}| = V_{CC}$ and $|V_G – V_T| = V_{CC} / 3$
- Measure or estimate capacitance C

Intrinsic Gate Delay CV/I for PMOS



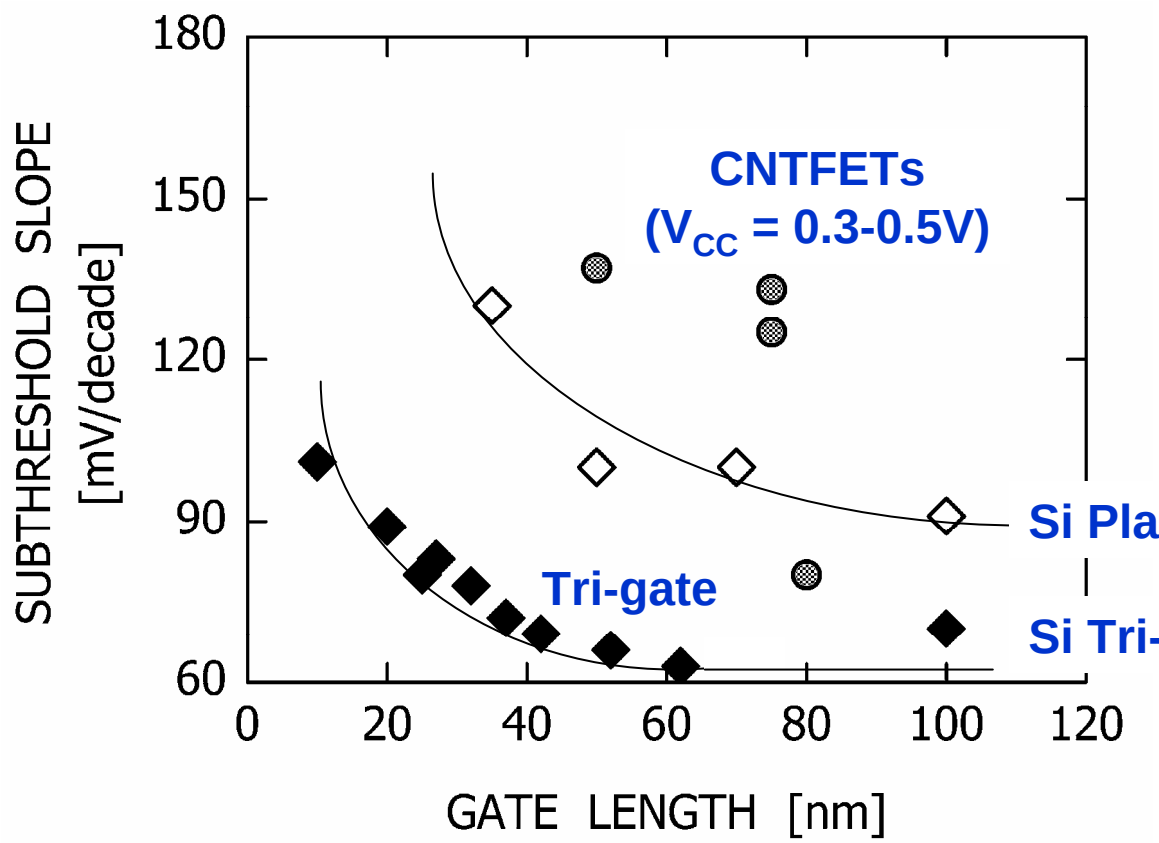
- CNT shows significant p-channel CV/I improvement over Si
  - CNT has >20x higher effective p-channel mobility than Si
- Si nanowires do not show any improvement over Si

Energy-Delay Product for PMOS

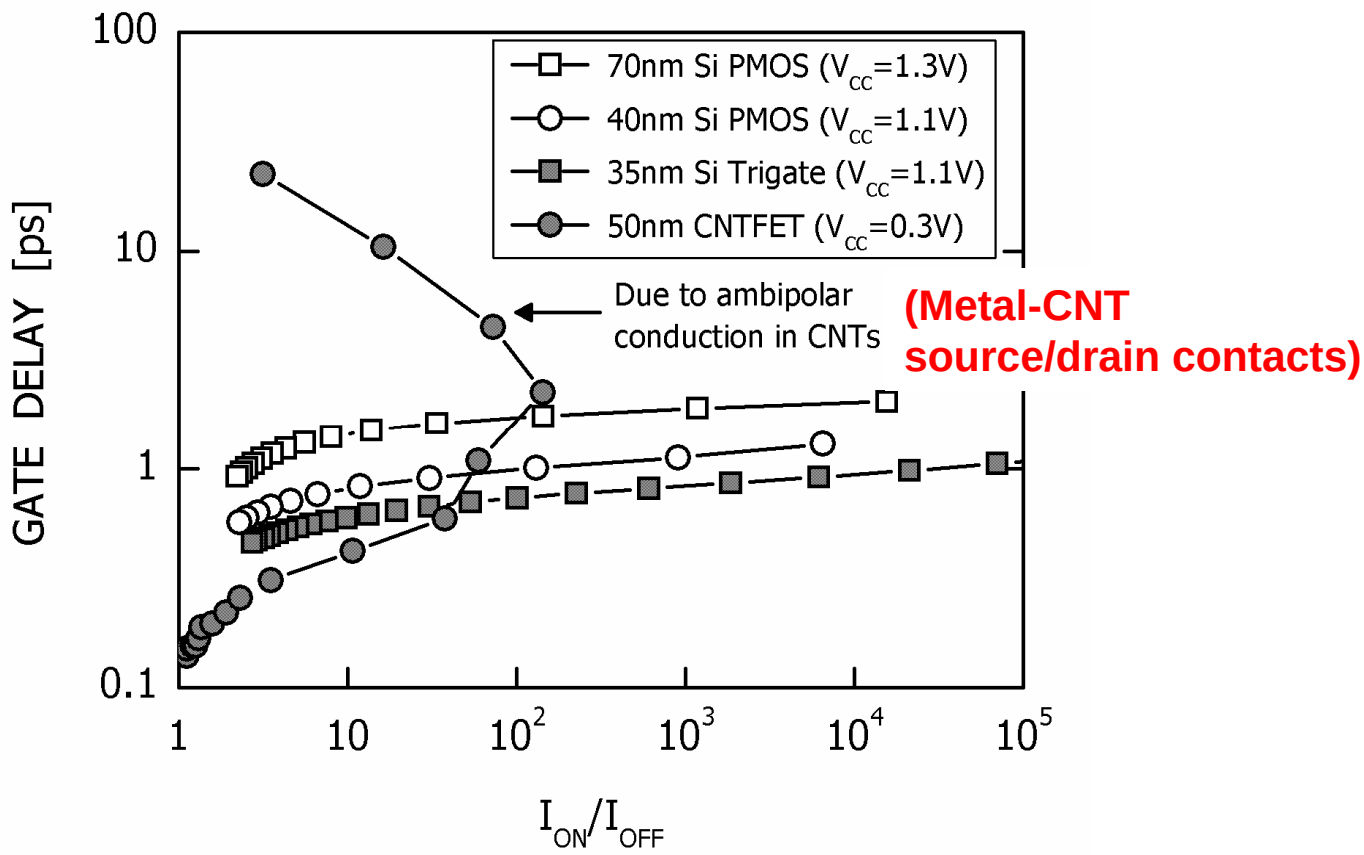


- CNT shows significant p-channel energy-delay product improvement over Si due to higher effective p-channel mobility than Si

Subthreshold Slope vs L_G for PMOS

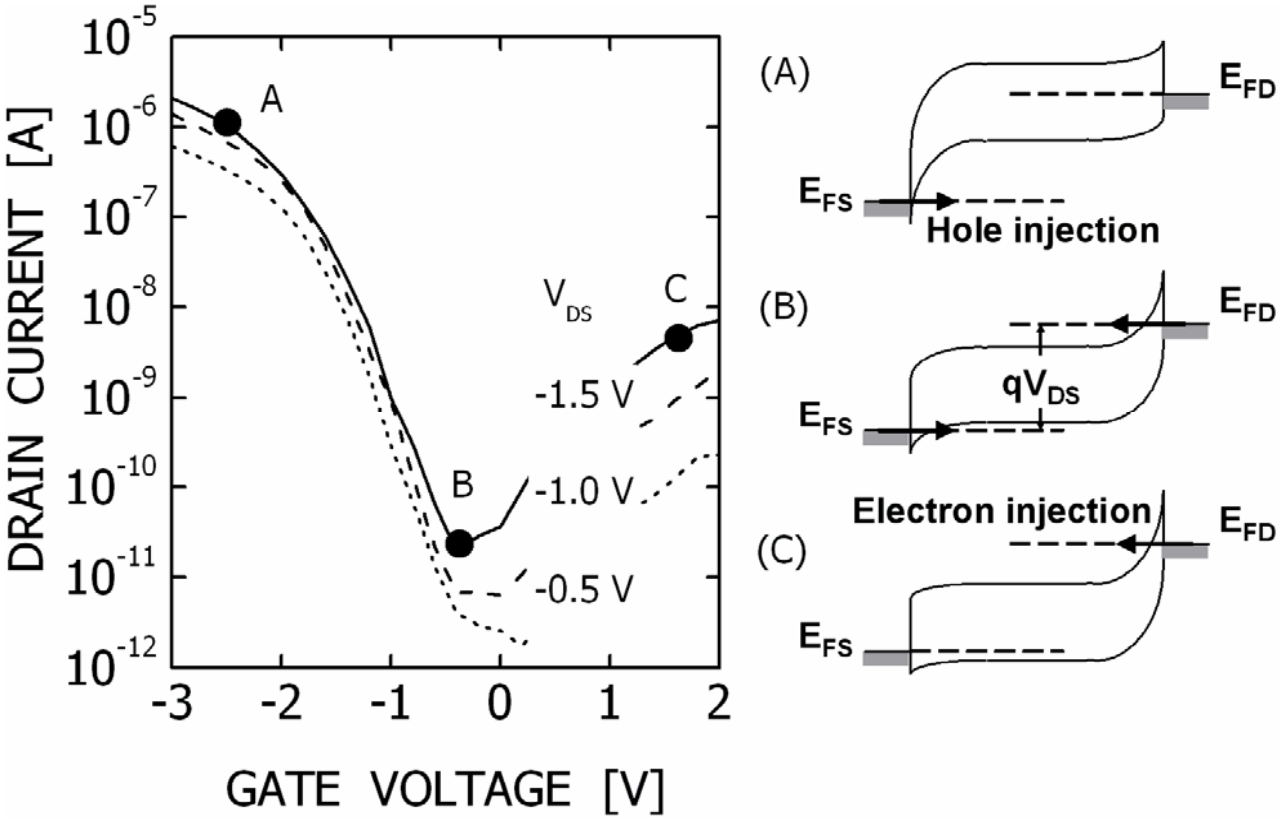


PMOS CV/I versus I_{ON}/I_{OFF} Ratio



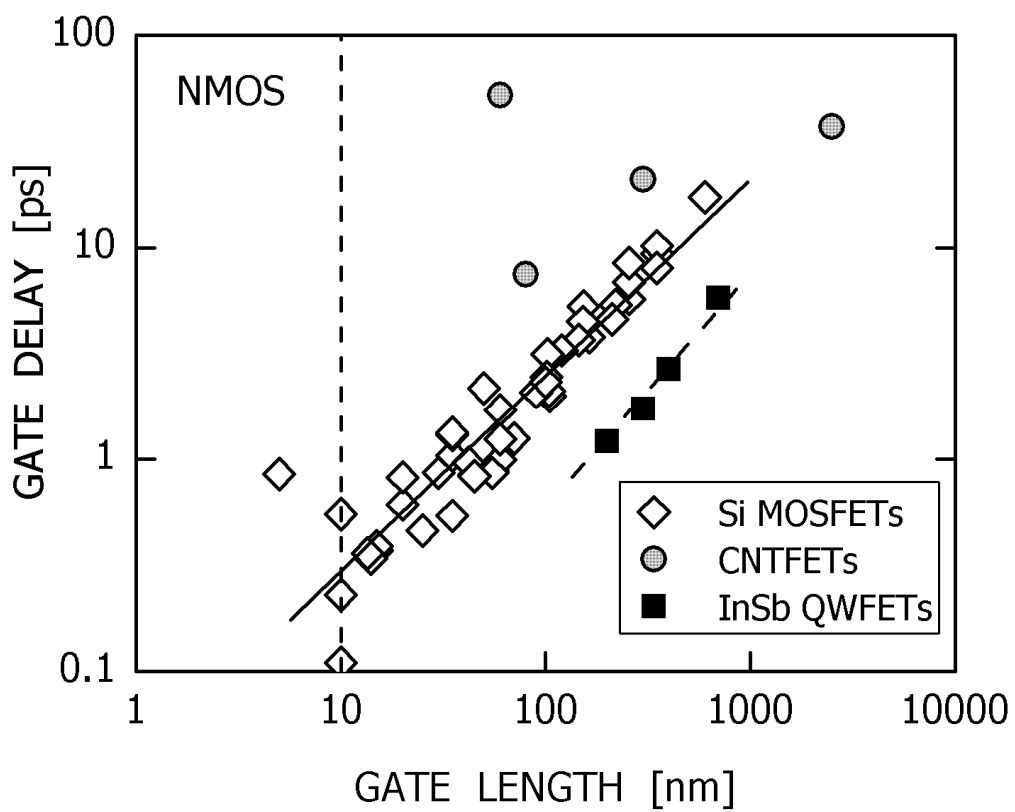
- For I_{ON}/I_{OFF} < 100, CNT shows improvement over Si due to higher channel mobility and lower V_{CC}
- I_{ON}/I_{OFF} (<100) in CNT is limited by ambipolar conduction

Ambipolar Conduction: Parasitic Leakage in CNTs



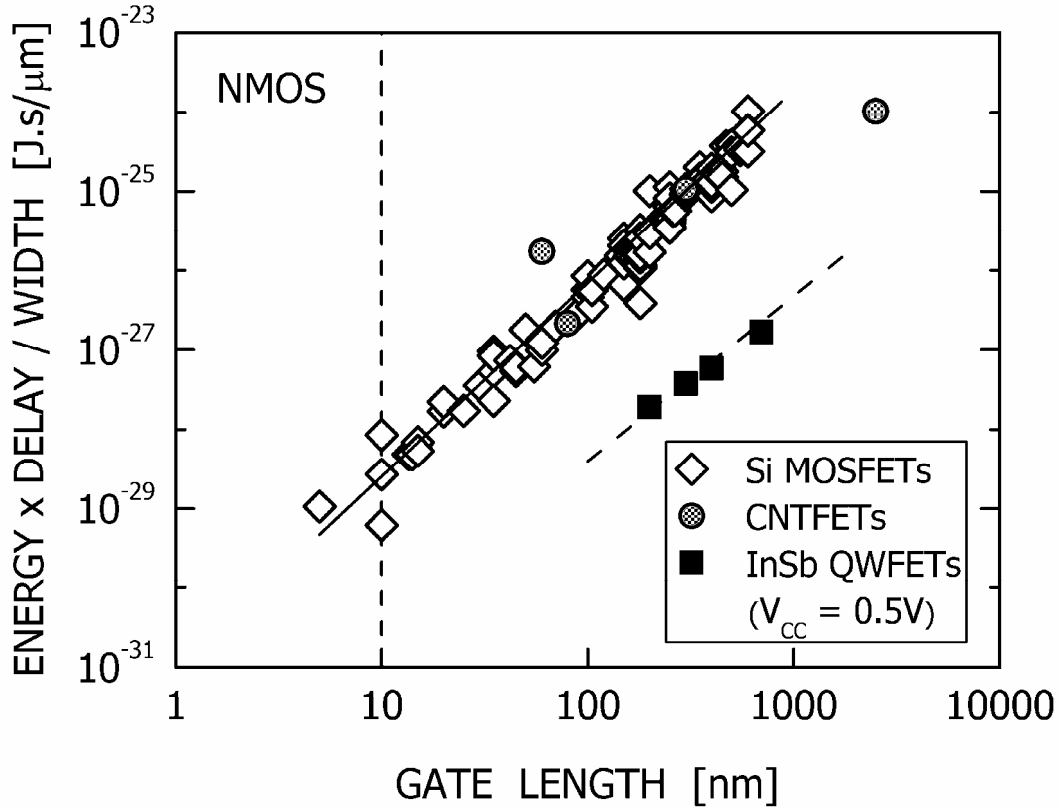
- CNTs use metal-CNT Schottky contacts to form source and drain, which leads to ambipolar conduction
- One of the technical challenges in CNT is to make conventional implanted or diffused PN junctions to form source and drain

Intrinsic Gate Delay CV/I for NMOS



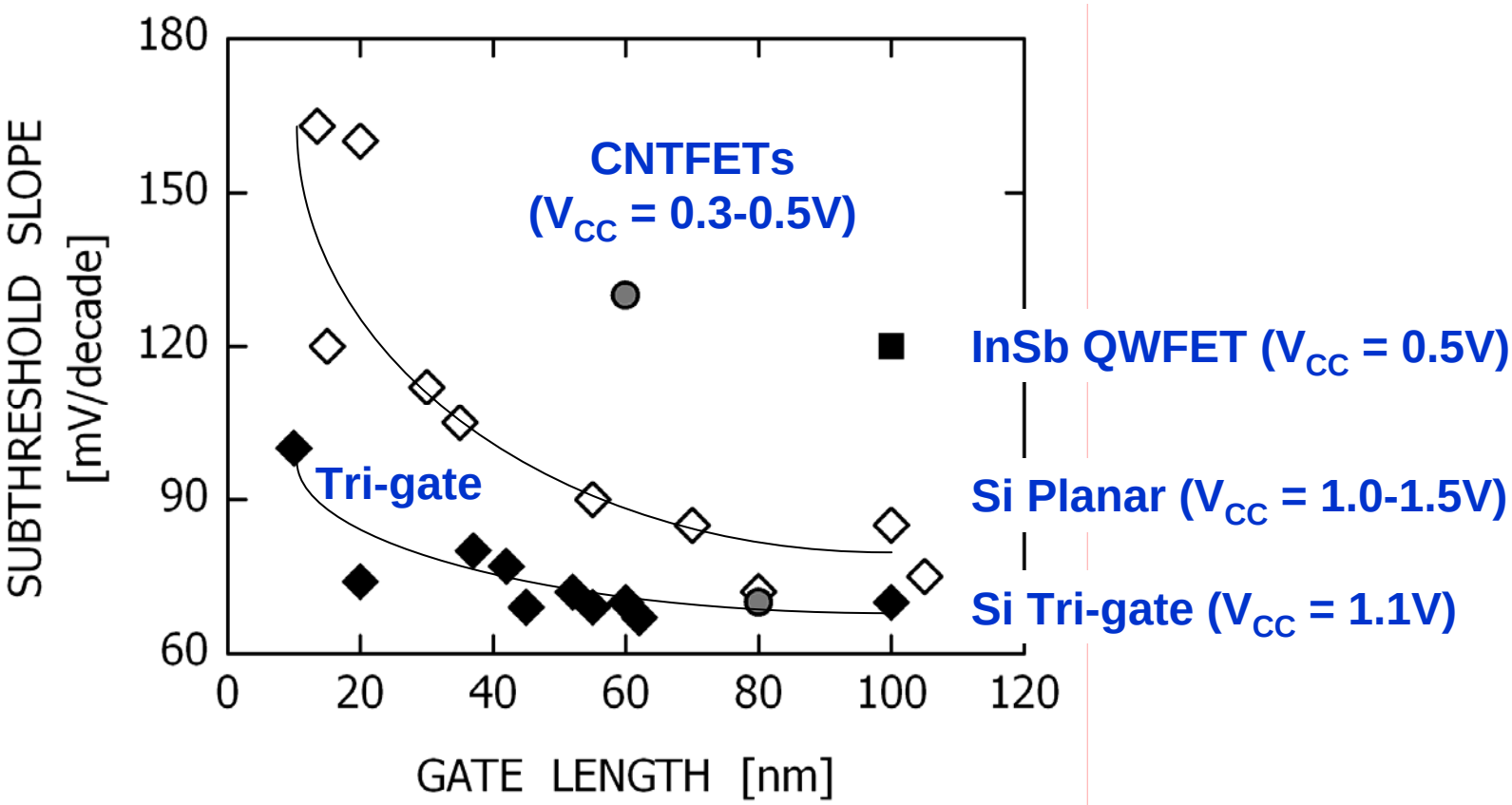
- n-channel CNT not as well established as p-channel CNT
- III-V (e.g. InSb) devices show significant CV/I improvement over Si
  - III-V devices have >50X higher effective n-ch mobility than Si
  - III-V devices operated at low VCC = 0.5V

Energy-Delay Product for NMOS

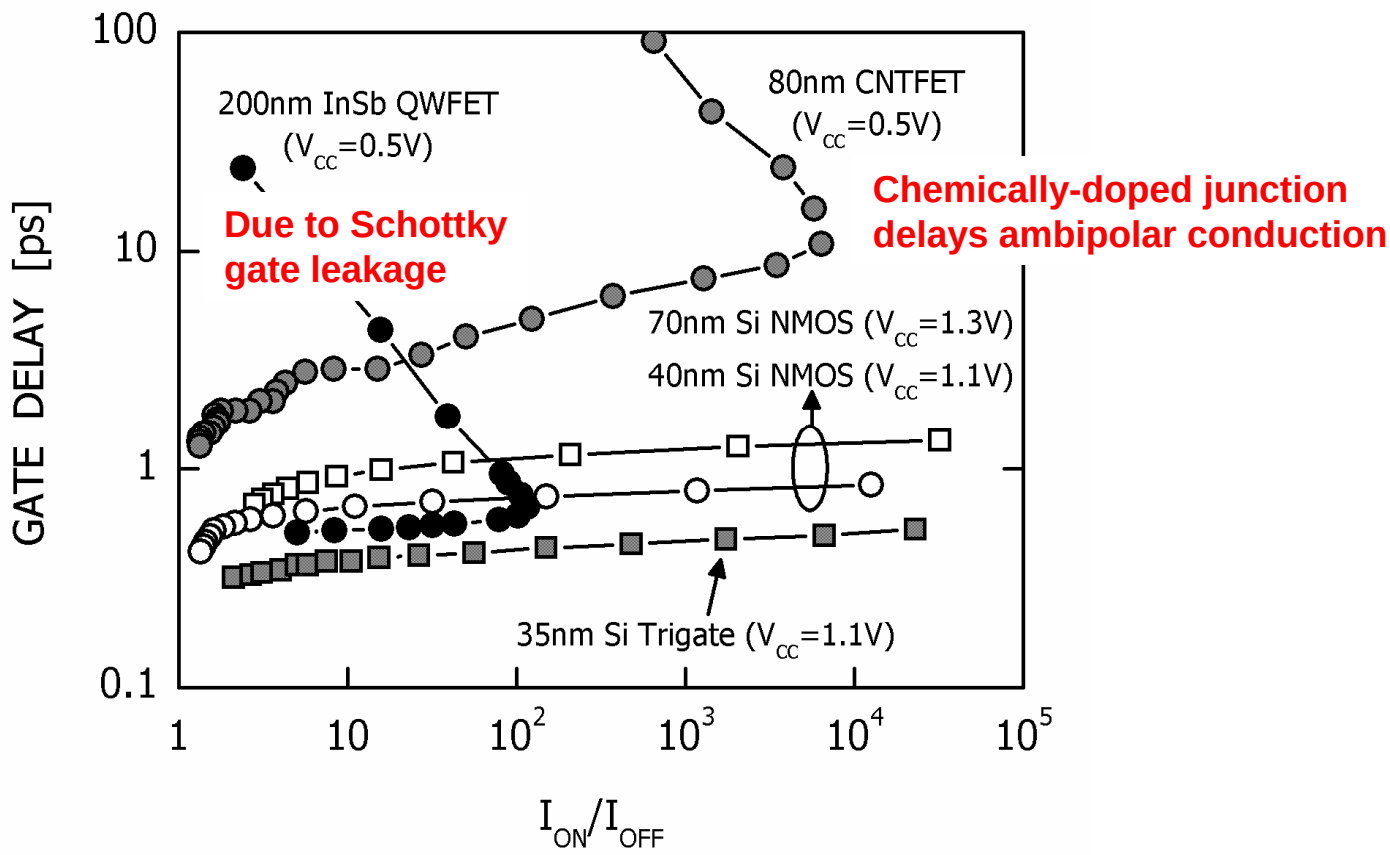


- III-V (e.g. InSb) devices show significant energy-delay product improvement over Si due to >50X higher effective mobility and lower V_{CC} = 0.5V used

Subthreshold Slope vs L_G for NMOS



NMOS CV/I versus I_{ON}/I_{OFF} Ratio



- Use of chemically-doped junctions delays the ambipolar conduction in the CNTFET despite poor gate delay performance at present
- I_{ON}/I_{OFF} ratio of InSb QWFET is limited by Schottky gate leakage

Summary

- Need to diligently benchmark emerging nanoelectronic devices against state-of-the-art Si data to
  - identify potential device strengths and shortcomings, and
  - to gauge research progress

- Emerging non-Si nanoelectronic devices show both challenges and opportunities for future logic transistor applications

References

- R. Chau, S. Datta, M. Doczy, B. Doyle, B. Jin, J. Kavalieros, A. Majumdar, M. Metz, and M. Radosavljevic, “Benchmarking Nanotechnology for High-Performance and Low-Power Logic Transistor Applications”, IEEE Transactions on Nanotechnology, vol. 4, pp. 153-158, 2005.

- R. Chau, J. Brask, S. Datta, G. Dewey, M. Doczy, B. Doyle, J. Kavalieros, B. Jin, M. Metz, A. Majumdar, and M. Radosavljevic, “Emerging Silicon and Non-Silicon Nanoelectronic Devices: Opportunities and Challenges for Future High-Performance and Low-Power Computational Applications”, Proceedings of Technical Papers, 2005 IEEE VLSI-TSA International Symposium on VLSI Technology, Hsinchu, Taiwan, pp. 13-16, April 25-27, 2005.