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Design investigation of nanoelectronic circuits using crossbar-based nanoarchitectures

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ABSTRACT

Nanowire crossbar is an efficient nanoscale architecture which can be used for logic circuit design. In this work, we study and compare different crossbar nanoarchitectures and their application in logic circuit implementation. To evaluate the performance of crossbar architecture compared to the conventional CMOS logic design, we have implemented logic circuits using both approaches. The equivalent circuit models of the crossbar-based circuits are then extracted and simulated using HSPICE. The CMOS circuits are also simulated using 22-nm technology parameters. Our simulation results show that crossbar-based circuits have much smaller area while CMOS circuits show better performance in terms of delay. We implemented area optimized cell libraries based on the crossbar architecture which considerably reduces circuit area. Simulation results of benchmark circuits using SIS synthesis tool indicate that the crossbar cells can be combined with CMOS cells to achieve tradeoff between circuit area and speed.

1. Introduction

Today's semiconductor industry uses photolithography techniques to transfer design patterns onto silicon wafers. While CMOS based structures are scaling down in order to maintain the anticipation of Moore's Law, they face challenges due to the quantum effects and manufacturing issues [1]. Today, it is accepted [2] that current lithographic patterning can be hardly used in few nanometer scales, and hence, there is rapidly growing interest in the nanoscale technology to construct memories and logic circuits. There is large interest toward emerging technologies as a replacement of the CMOS technology. These technologies are divided into two sets from a physics point of view [3]: those that are based on the physics similar to CMOS, such as carbon nanotubes (CNTs) and silicon nanowires (SiNWs), and those with different physics, which includes spintronics [4], quantum cellular automata (QCA) [5,6], single electron transistors (SET) [7,8], molecular electronics, DNA and biological computing [9].

One of the most promising nanoscale paradigms is the nanoarray architecture, especially the nanowire crossbar. The nanowire crossbar is a two-dimensional array (nanoarray) consisting of two orthogonal sets of parallel nanoscale wires, such as CNTs and SiNWs [10]. In such architectures, any intersection or crosspoint of two wires within the crossbar architecture can be configured as an electronic device, such as a resistor, a diode, or a transistor. These structures have some favorable characteristics such as small size, high density, and periodic geometry, making them good candidates for the upcoming high-density interconnect and logic circuits implementation [10–14]. Various nanoscale architectures, such as NanoFabric [15], NanoPLA [16], NASIC [17], CMOL [18], 3D nFPGA [19], FPCNA [20] and RDG-CNFET [21], are introduced in the literature. These architectures have different structures, physical parameters, design strategies and fabrication processes, which cause them to have their advantages and disadvantages. The nanowire crossbar has been used in memory architectures because of its periodic structure [13,22]. Although, currently it is not possible to make an electronic circuit by using nanoscale devices, but combining it with CMOS circuits may be considered an interesting idea [23].

In this paper, we have investigated different nanoscale crossbar architectures in terms of their characteristics and properties. Among these, the architecture introduced by HP is the one that was used to physically implement logic circuits [24]. Although, some works have addressed the use of nanowire crossbar architecture for logic implementation [12,24,25] but their performance cannot be evaluated compared to MOSFET circuits. We have implemented some logic circuits using both MOSFET and CMOS-like crossbar architecture to compare their performances in terms of delay and area. The rest of this paper follows with a brief description of crossbar architectures and related technology, which are given in Sections 2 and 3. The nanowire crossbar proposed in Ref. [26], which we have used for our simulations, is described in Section 4. Performance evaluation of

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nanowire crossbar and simulation results are presented in Section 5, and finally a summary and conclusion are given in Section 6.

2. Nanoscale technology

This section gives a review of the nanoscale fabrication technologies. Then, different types of nanoscale devices and nanoscale crossbar architectures including related issues are explained.

2.1. Fabrication technologies

There are two main approaches to fabricate nanostructures; bottom-up and top-down techniques. In the top-down approach, which is currently employed in the silicon industry, devices such as transistors are etched on silicon wafers using the photolithography process. The physical dimensions of these devices are limited by the resolution of the lithography method. Standard photolithography techniques along with accurate control of etching, oxidation and deposition can be used to define small features. The electron-beam lithography is another way to achieve higher resolution than standard photolithography. The spacer patterning technique (SPT) is another top-down technique which exploits photolithography and anisotropic etch of the deposited materials to transform vertical features in the vicinity of a step of a sacrificial layer into horizontal features [27,28]. In Ref. [29] the multi-spacer patterning technique (MSPT) is used to build poly-Si nanowire FETs, which can be put in the crossbar architecture. Alternative techniques use nanoimprint lithography (NIL), in which a nanomold is pressed onto a resist-covered substrate to create desired pattern [30].

As an alternative, bottom-up techniques can be used to implement emerging technologies with nanowires and carbon nanotubes. In the bottom-up approach the devices and the nanowires are synthesized first, and then assembled into functional devices and systems. Different chemical assembly methods including Langmuir–Blodgett films [31–33] flow-based alignment, random assembly, biologically assisted assembly, and catalyzed growth can be used in bottom-up process [34,35]. The assembly can be controlled on an atomic or a molecular scale and hence size limits could be much smaller. Generally, the bottom-up assembly approaches can only produce structures with extreme regularity and high defect rates [36]. One of the bottom-up techniques is the vapor–liquid–solid (VLS) process [37,38], in which crystal growth occurs from the nucleated catalytic seed at the metal–solid interface.

2.2. Nanoscale wires and devices

Two major wire types, CNTs and SiNWs, can be distinguished in nanotechnology. CNTs can be synthesized in nanometer scale, but we cannot control the detailed electrical properties for these nanotubes. SiNWs are other promising building blocks for nanoscale computing systems. The electrical properties of these SiNWs can be controlled with dopants, resulting in semiconducting wires. NWs can be used along with nanotubes, in which their properties complement each another.

The nanowires can be fabricated in two forms: *undifferentiated* or *uniform* nanowires, and *differentiated* or *encoded* nanowires [1]. The uniform nanowires are grown identically, with no specific doping profile, and are differentiated after assembly. The *differentiated* nanowires are grown with different encodings in advance, which results in a certain doping profile. Dopant molecules are added to a gaseous mixture as the nanowires grow. As a result, heavily and lightly doped regions form along the nanowire lengths, depending on the exposure time as shown in Fig. 1a. These two types of nanowires can be used as active devices in different ways. Consider a microwire (MW) at the top of a uniform nanowire. Depositing impurities such as gold particles or depositing a high-κ dielectric at the contact between the microwire and nanowire can lead to a controllable junction, and preventing the deposition of such impurities makes the junction uncontrollable. Applying an electric field on the microwire can control the conductance of the nanowire [39]. A schematic view of such device is shown in Fig. 1b.

3. Nanoscale regular architectures

Semiconductor nanowires (NWs) can be made using different materials including silicon [40], germanium [39], InSb [41], etc. It is possible to assemble these materials into regular arrays using assembly techniques. The crossbar shown in Fig. 2 is a simple network consisting of two orthogonal sets of parallel nanowire layers separated by an interlayer [24]. The interlayer between the two planes of parallel nanowires determines the type of devices that will be configured. Any intersection or crosspoint of two wires within the crossbar can be configured as an electronic device, such as a resistor, a diode, or a transistor; hence, various crossbar circuits are possible. Crossbars can be used to implement interconnect networks, memories, and logic circuits as well (e.g., [12,22,42]).

Various crossbar based architectures are introduced in the literature. In a diode-based crossbar, each crosspoint can be configured as a diode or to an open circuit after fabrication. Though this structure has some inherent limitations, it may be used to implement memory units and logic circuits [25]. Several works have been proposed to build FETs out of carbon nanotubes [43] or silicon nanowires [44]. In the nanowire approach, one nanowire can act as the gate of the transistor to control the other crossing nanowire which forms the source and the drain of the transistor. Using these types of transistors one can build logic gates [12]. Some works have addressed the use of memristors as crosspoint devices to build crossbar architectures [45], as explained in the following subsections. Although all the architectures have crossbar structure, they use different devices and fabrication technology.

3.1. NanoFabric

NanoFabric, which is proposed by Goldstein and Budiu, is based on the chemically assembled electronic nanotechnology (CAEN) [15].

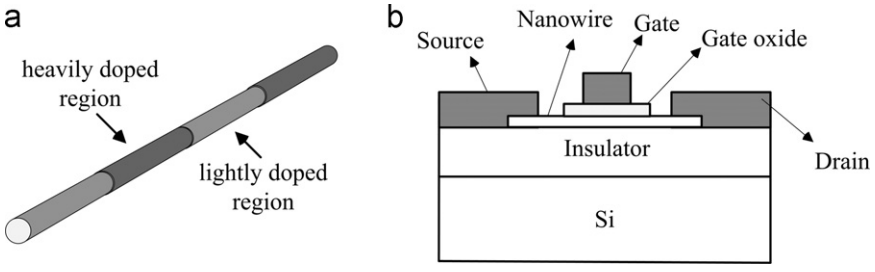

Fig. 1. (a) Encoded nanowire, (b) Schematic of a NWFET device with high-κ dielectric layer.

It consists of nanologic arrays which are interconnected by long nanowires (Fig. 3). The nanologic, also called Nanoblocks, implement a diode-resistor logic since crosspoints act as programmable diodes. The Nanoblock, similar to a configuration logic block (CLB) in FPGA, can be configured to perform logic functions. The Nanoblocks can also be used as routing switches to provide interface between adjacent Nanoblocks. The long nanowires allow signal transmission between Nanoblocks without going through any switches. A Nanoblock can be programmed after fabrication to implement logic functions.

3.2. NanoPLA

In 2004, André DeHon proposed the nanoscale programmable logic array (NanoPLA) architecture which is composed of nanowire crossbars with programmable diodes for logic function implementations [16] (Fig. 4). This is a PLA-like architecture which uses the NOR–NOR logic style. To overcome the restoration and inversion limitations of diode logic the authors propose to insert nanowire FETs between diode stages. They used a special decoder [46] to solve the nano/CMOS interface problem for addressing the nanowires through microwires. The reconfiguration technique is used for defect tolerance of the architecture.

3.3. CMOS-like architecture

Snider et al. presented a crossbar architecture with configurable FETs and switches which is used to implement CMOS-like logic [24]. The basic building block of the architecture, shown in Fig. 5, consists of two orthogonal sets of parallel nanowires in separate planes. The horizontal nanowires are metallic and the vertical ones are semiconductors, with p-type in the left half and n-type in the right half. Any crosspoint can be configured to be a p-FET or n-FET at the left or right sides, respectively. The gate of a FET is implemented with the horizontal wire and the source and drain are implemented with the vertical wire. The wires at the bottom of the figure can be configured as 'open' or 'closed' switches. Any logical function can be implemented by the selective configuration of junctions in each of the quadrants. The uniformity and redundancy of components in the crossbar are used for defect tolerant mapping.

3.4. NASIC

Moritz et al. proposed a nanoarchitecture that can be tuned toward an application domain, known as nanoscale application-specific integrated circuit (NASIC) [17]. The basic block of the NASIC

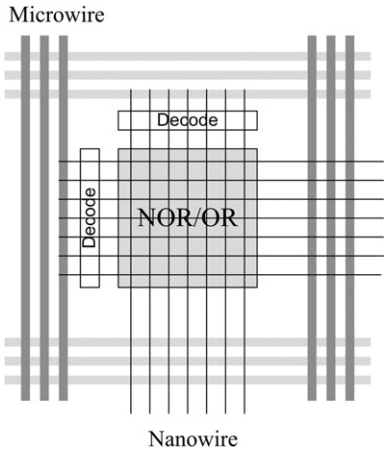

Fig. 4. NanoPLA architecture (reproduced from Ref. [16]).

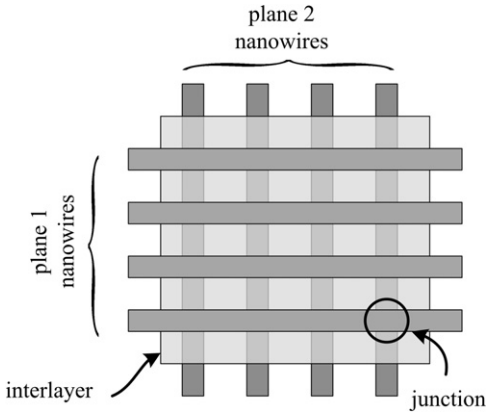

Fig. 2. Schematic view of a nanowire crossbar.

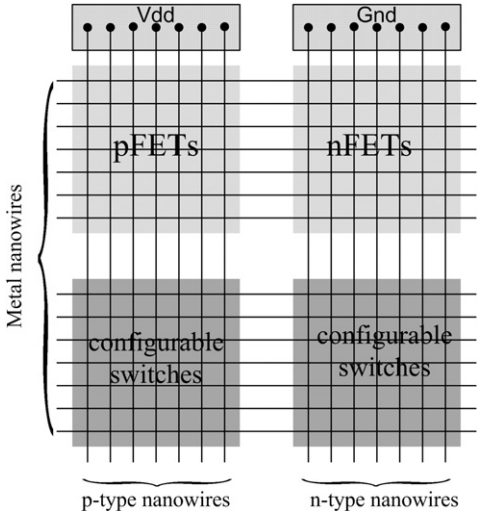

Fig. 5. Basic block of CMOS-like architecture (reproduced from Ref. [24]).

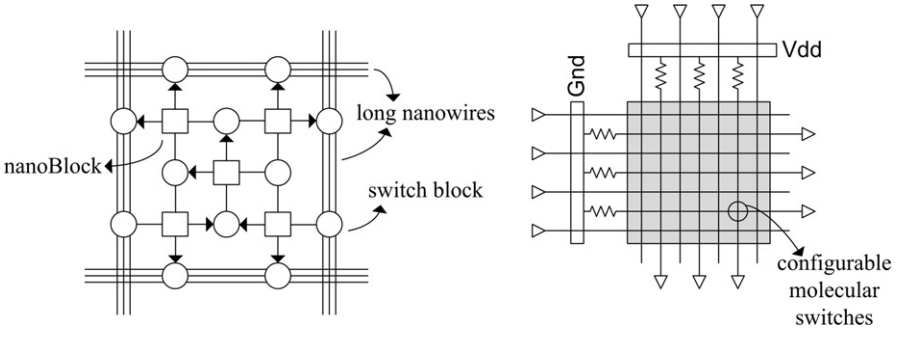

Fig. 3. Schematic view of NanoFabric, (a) a cluster of NanoFabric, (b) schematic of a nanoBlock (reproduced from Ref. [15]).

fabric is built up as a crossbar silicon nanowire grid with crossed nanowire field-effect transistors (xnwFETs) at certain crosspoints (Fig. 6). The channel of an xnwFET is aligned along one NW while the perpendicular NW above it, acts as a gate. Each basic block can be used to implement any arbitrary logic circuit. Peripheral thick lines are microwires carrying VDD, VSS, communication, and configuration signals. The author showed a 2-level logic combination of AND–OR and NOR–NOR to achieve a denser implementation [47]. This architecture has the possibility to be manufactured using only one type of FET to reduce the manufacturing requirements [48]. The structural redundancy based techniques, such as Triple Modular Redundancy (TMR) [49,50], are used to make the NASIC a defect tolerant architecture. A new generation of NASIC, called N3ASIC, is introduced in Ref. [51] in which active devices are formed at nanowire array crosspoints, and then is connected to a 3-D CMOS routing metal stack through area-distributed interfaces.

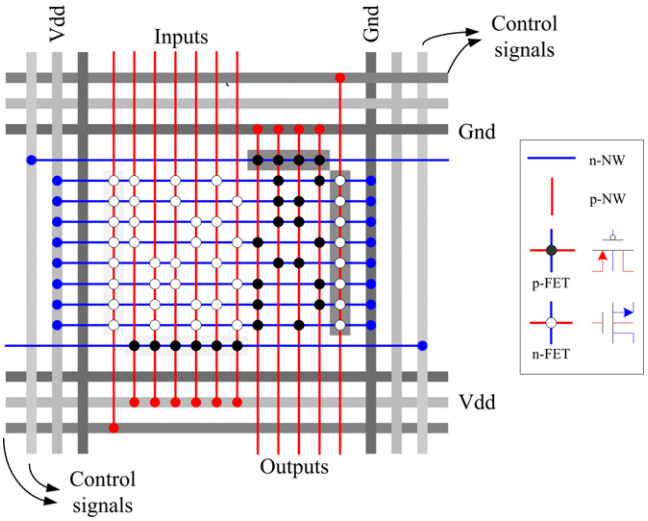

Fig. 6. NASIC building block (reproduced from Ref. [52]).

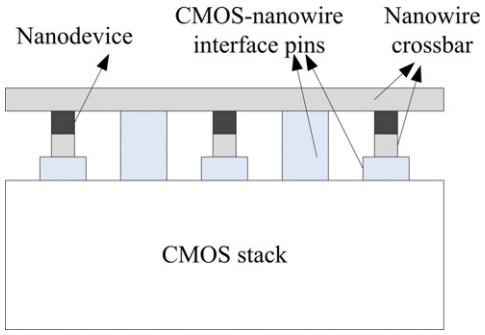

Fig. 7. CMOL architecture.

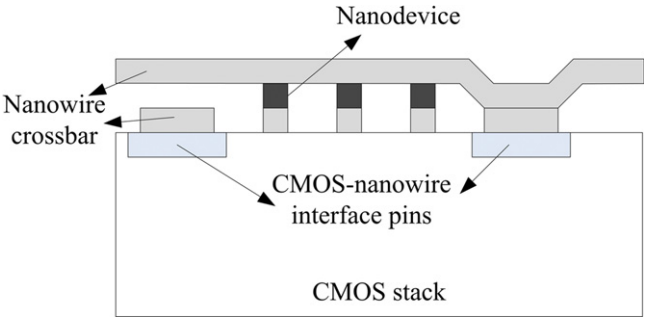

Fig. 8. FPNI structure.

3.5. CMOL

Likharev et al. introduced CMOL architecture [18], which uses nano crossbars on top of CMOS cells to increase the device density. This approach is used to implement reconfigurable logic [53], memory, and neuromorphic networks [18]. In CMOL, the nanowire crossbar with molecular nanodevice at every crosspoint are fabricated on top of the CMOS die as shown in Fig. 7. The nanowire crosspoint provides programmable interconnects and wired-OR logic, while its underneath CMOS cell acts as an inverter for signal inversion and gain. This arrangement is suitable to implement basic logic and memory cells with programmable capabilities. The connection between CMOS and junction devices is made through two sets of metal pins which penetrate into the nanowire crossbar layer to connect the top and bottom nanowires to the CMOS layer respectively (see Fig. 7). These interface pins are the challenging part of the CMOL fabrication. The CMOL architecture uses reconfiguration as a defect tolerance technique. As an extension, a 3D-CMOL is introduced in Ref. [54] which has two upper and lower CMOS stacks and one crossbar layer in between. In 3D-CMOL, each CMOS stack only needs to contact with the neighbor nanowire layer of the crossbar. This removes the need for special interface pins of the two-dimensional CMOL, enabling a feasible fabrication process.

3.6. FPNI

Snider and Williams introduced the field-programmable nanowire interconnect (FPNI) [55] in order to solve the special pin problem of CMOL. The FPNI is a generalized form of CMOL which trades off some of the advantages of CMOL, such as density and defect tolerance, in exchange for easier fabrication, lower power dissipation and easier routing. In FPNI, a nanowire crossbar is placed on top of CMOS logic gates (Fig. 8). Any arbitrary logic computation can be performed in CMOS cells, which are not restricted to inverters as in CMOL. The nanowire crosspoints in FPNI are resistive junctions, which can only be used for signal routing unlike CMOL. FPNI uses large nano-pads to contact with the CMOS stack, leading to a fabrication with high defect-tolerance. However, due to the large size of pads, a low device density is resulted. Like the CMOL the reconfiguration is used to tolerate the defects of FPNI circuits.

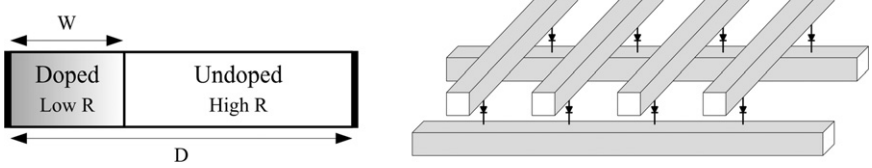

Fig. 9. (a) Schematic view of memristor [57], (b) memristor based crossbar with serial diodes.

Table I
Comparison of different crossbar architectures.

	NanoFabric	NanoPLA	CMOS-like	NASIC, N3ASIC	CMOL	FPNI	RDG-CNFET-based	FPCNA
Structure	2D-NW array	2D-SiNW, MW	2D-SiNW array	2D, 3D-NW array	2D, 3D-NW array on CMOS transistors	3D-CMOS cell array on crossbar NWs	2D-CNT array	2D-CNT array
Cross points	Molecular switch (programmable diode)	Programmable diode	nFET or pFET transistors	FET transistors or P–N diodes	Programmable diode	Programmable diode	RDG-CNFET transistors	CNFET devices
Function of Nanodevices	Circuit implementation, routing	NOR–NOR logic	Arbitrary circuit, interconnect, I/O	Arbitrary circuit, interconnect	NOR logic, routing, memory array	Routing, interconnect	Combinational logic	Logic blocks, routing
Function of CMOS devices	Clock, power, GND, Configuration signals, I/O	Addressing, routing, Configuration signals	–	Addressing, control and configuration signals,	Inversion, demultiplexing, gain	Arbitrary circuit, (NAND, Flip Flop, …)	–	–
Application	FPGA	PLA	Functional logic, memory, …	Processor	Memory, FPGA	FPGA	Functional logic, memory, …	FPGA like
Nanofabrication technology	NanoPore templates	NW catalyst	Nanoimprint lithography	–	Nanoimprint lithography	Nanoimprint lithography	Top-down lithography	Array based CNT growth
Logic implementation	Nanoscale wired-OR	Nanoscale wired-OR	CMOS like logic	NAND NOR	Nanoscale wired-NOR	Lithoscale (n)and2	CMOS static lookup table based	Lookup table
CMOS to NW interface	–	Coded nanowire	–	Coded nanowire	Crossbar tilt, conical pins	Crossbar tilt, CMOS pins	–	–
Signal restoration	RTD latch	NW FETs	NW transistors		CMOS	CMOS	–	-
CAD tools	current FPGA tools	PLAMAP, NPR	Nano-Xax	Madeo	T-VPACK	Maze router	–	SIS, DAOmap, T-VPACK
Fault tolerant technique	Reconfiguration	Reconfiguration, rollback recovery	Circuit redundancy	Self-healing circuits	Reconfiguration	Reconfiguration	Adaptive configuration technique	Using CNT ribbons, FPGA reconfiguration

3.7. Memristor-based architecture

A memristor is the fourth fundamental circuit element that was proposed and described by Leon Chua in 1971 [56]. Memristor was physically realized by Stan Williams' group at HP Labs in 2008 [57]. The memristor consists of a thin film of TiO_2 of thickness D sandwiched between two metal contacts, as shown in Fig. 9a. This thin-film is divided into O^{+2} doped region of width W having low resistance R_{ON}, and an undoped region with much higher resistance R_{OFF}. Applying an external bias voltage across the device drifts the charge dopants, resulting in the movement of the boundary between the two regions. This will change the resistance of the device, even after removing the bias voltage.

Some researchers have addressed the use of memristors in crossbars [45,58]. Memristor crossbars include two perpendicular arrays of metal lines with a memristor device at the crosspoints. A fundamental problem for memristor arrays is the sneak current paths, which correspond to parasitic current paths through off state switches. To solve this problem, either rectifying diodes can be serially connected with each memristor element [59] as shown in Fig. 9b, or self-rectifying diodes can be employed [60]. A hybrid memristor crossbar array/CMOS system is proposed in Ref. [61], in which a memristor crossbar array is vertically integrated on top of a CMOS chip.

3.8. CNT-based architectures

As an alternative to CMOS transistors, carbon nanotube field effect transistors (CNFETs) are promising candidates for the building blocks of nanoelectronic circuits. Different kinds of CNT based transistors have been proposed, such as the Schottky barrier based carbon nanotube field effect transistor (SB-CNFET), MOSFET-like CNFET, and band-to-band tunneling carbon nanotube field effect transistor (T-CNFET) [62]. A carbon nanotube based FPGA architecture called FPCNA is proposed in Ref. [20], which includes a lookup table (LUT) to make up its programmable logic. This architecture uses MOSFET-like CNFETs, in which a semiconducting CNT forms the conducting channel between the source and the drain contacts, and is controlled by a gate electrode. Liu in Ref. [21] introduced a reconfigurable double gate CNFET (RDG-CNFET), which is constructed by three overlapping orthogonal carbon nanotubes. The top and the bottom carbon nanotubes form the front gate and the back gate, while the doped carbon nanotube in the middle layer forms the source and the drain of an n- or p-type MOSFET-like CNFET. This RDG-CNFET is reconfigurable to be open, short, FET, or via. Bao constructed a

Fig. 10. FET-based crossbar architecture (reproduced from Ref. [26]).

crossbar architecture with RDG-CNFET at each carbon nanotube crosspoint, that can be used to implement all logic families.

3.9. Comparison of different crossbar based architectures

Table I compares nanoscale crossbar architectures in different aspects. Most of the architectures employ the CMOS-based structure to complement the overall functionality of the architecture. Some of the architecture can be used to implement any computational function, while some others are targeted as FPGA, memory or processor. Another important issue is the fabrication and physical implementation possibility. Some architectures are not feasible to implement, such as the CMOL idea which is not physically implemented yet [3]. The CNT-based crossbars are also difficult to implement and integrate into CMOS chips. The CMOS-like architectures, which use nanowire FETs at the crosspoints, are promising candidates for future nanoscale electronics, as the nanowires fabrication is more controllable and well-studied. Moreover, the conventional lithography process can be used to fabricate a crossbar consisting of nanowire FETs. Memristor based architectures are other potential candidates for nanoelectronic circuit design, since these are more feasible to implement as shown by fabrication reports [61]. A common problem of nanoscale architectures is the high defect rate and fault densities, which requires investigation of the fault models and

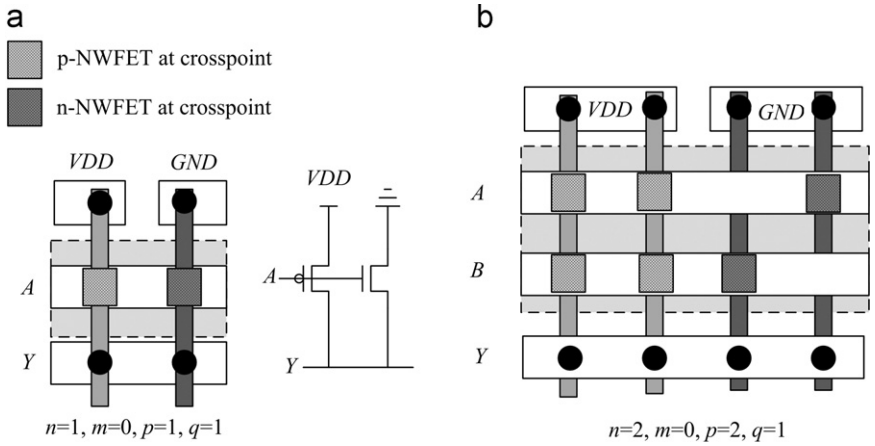

Fig. 11. Logic gate implementation using nanowire crossbar, (a) inverter and its equivalent circuit, (b) 2-input NOR gate (reproduced from Ref. [26]).

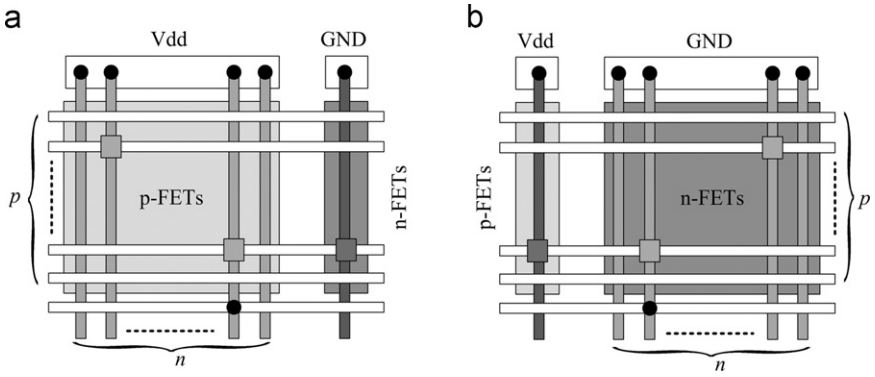

Fig. 12. Asymmetric nano architecture, (a) NAND-based structure, (b) NOR-based structure.

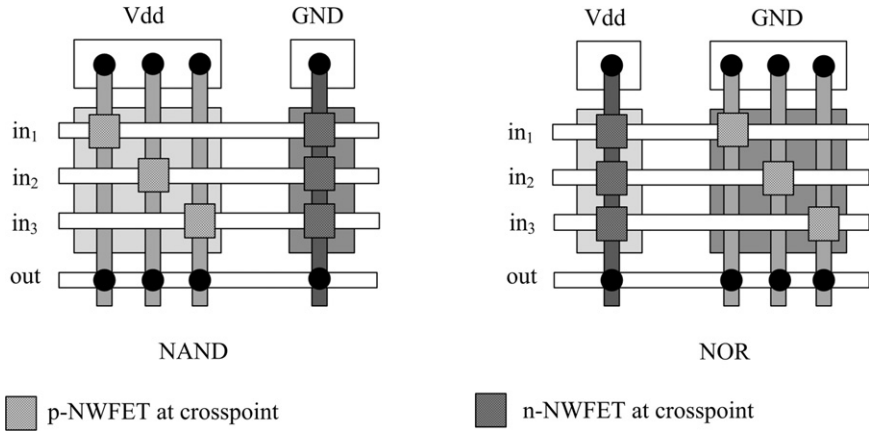

Fig. 13. Logic gate implementation using asymmetric nano-crossbar.

employing defect tolerant techniques. Another characteristic of different architectures is the logic implementation strategy. For example, NanoPLA uses NOR–NOR, while NASIC proposes to implement different logic styles. Another major issue is to interface a crossbar with a decoder to the outer CMOS circuits, as CMOL uses special interface pins to connect nanowire crossbar to CMOS stage.

4. Logic implementation using nanowire crossbar

Among the different crossbar architectures, the CMOS-like is more feasible to implement using nanowire transistors, because of its regular and uncomplicated construction. In this crossbar architecture any crosspoint can be considered as an n-channel nanowire FET (n-NWFET) or p-channel nanowire FET (p-NWFET). The basic block diagram of such a crossbar architecture consisting of n-NWFET and p-NWFET arrays for creating logic circuits is illustrated in Fig. 10 [24,26]. The schematic architecture in this figure consists of p horizontal metallic and $2n$ vertical silicon nanowires located in two separate layers. The vertical wires in the left and right part of the architecture are p-type and n-type, respectively. The middle vertical wires are layer 2 metallic wires used for local interconnection. Each junction in the left and right top sections can be a p-NWFET and n-NWFET, respectively. The q wires in the bottom part along with the vertical wires can be configured as switches to make the required connections for output and local interconnects. In this architecture, silicon nanowires and metallic wires are separated by a low-κ insulator layer, and a NWFET can be formed at the crosspoint of these wires. The area of the whole crossbar can be calculated as $\text{Area} = (2n+m)(1+p+q)P_{nw}^2$ [26]. An example of a logic implementation using this crossbar is shown in Fig. 11.

Since the structure of Fig. 10 has symmetric P-NWFET and N-NWFET planes, there would be parallel paths for series stack transistors in multi-input gates. This can be seen in the P-NWFET plane of the NOR gate of Fig. 11, which consists of two parallel paths of pull-up (PU) network. Although the parallel path increases the speed of the PU network, it increases the input capacitance load and the gate area. Using the new asymmetric architecture of Fig. 12, which contains only one pull-down or Pull-down (PD) network, the circuit area will be reduced to $\text{Area} = (n+1)(n+2)P_{nw}^2$. Such architectures can be employed to design fully NOR- and NAND-based circuits. Fig. 13 shows the 3-input NOR and NAND gates implemented using asymmetric nanocrossbar architecture.

Table II
SPICE parameters of the crossbar.

Parameter description	Parameter name	Value
Nanowire pitch	P_{nw}	60 nm
Nanowire width	W_{nw}	20 nm
Equivalent ON resistance of n-NWFET	$R_{on,n}$	10.67 kΩ
Equivalent ON resistance of p-NWFET	$R_{on,p}$	26.67 kΩ
Equivalent OFF resistance of n-NWFET	$R_{off,n}$	15 GΩ
Equivalent OFF resistance of p-NWFET	$R_{off,p}$	15 GΩ
Resistance of n-type Nanowire	$R_{nw,n}=r_{nw,n}\times P_{nw}$	2.99 kΩ
Resistance of p-type Nanowire	$R_{nw,p}=r_{nw,p}\times P_{nw}$	7.48 kΩ
Contact resistance	R_c	1 kΩ
Gate-source capacitance	C_{gs}, C_{gd}	70.8 aF
Nanowire capacitance	$C_{nw}=c_{nw}\times P_{nw}$	2.18 aF
Threshold voltage of n-NWFET	V_{tn}	0.35 V
Threshold voltage of p-NWFET	V_{tp}	−0.38 V
Voltage source	V_{dd}	0.8 V

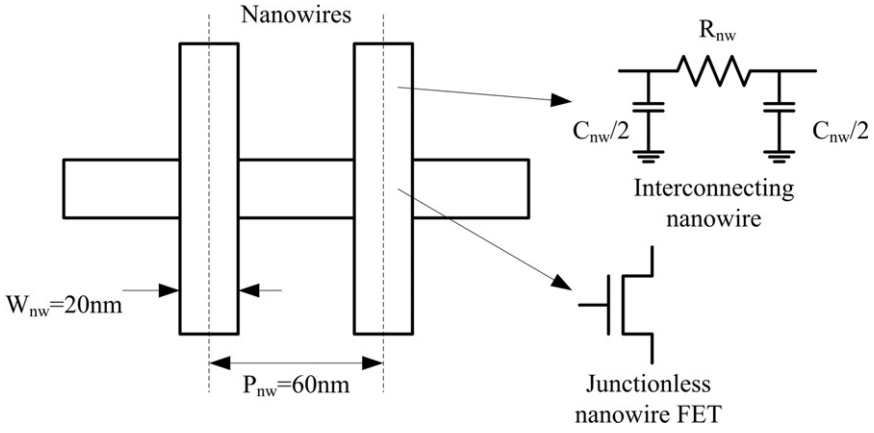

Fig. 14. Geometery and modeling of the nanowire crossbar.

Table III
Simulation results of basic logic gates.

	Cell library	INV	NAND2	NAND3	NAND4	NOR2	NOR3	NOR4
Worst case delay (ps)	C	4.01	7.26	12.10	19.20	12.40	24.50	39.50
	NWC	7.86	18.40	24.30	31.10	18.00	20.70	23.80
	ANWC	7.86	17.90	21.40	30.10	34.10	55.90	82.10
Area (μm^2)	C	0.097	0.116	0.155	0.194	0.116	0.155	0.194
	NWC	0.022	0.058	0.108	0.173	0.058	0.108	0.173
	ANWC	0.022	0.043	0.072	0.108	0.043	0.072	0.108
EDP (1e–30 Js)	C	3.73	11.52	30.68	56.30	21.14	47.84	70.54
	NWC	5.74	17.71	24.95	28.31	16.55	13.97	9.20
	ANWC	5.74	23.20	36.37	28.42	37.15	40.42	51.17

C: CMOS, NWC: nanowire crossbar, ANWC: asymmetric nanowire crossbar.

5. Implementation and simulation results

In order to compare the performance of the nanowire crossbar with conventional CMOS circuits, we have implemented some logic elements and circuits using these approaches. This section gives the implementation details and simulation results. We used the crossbar architectures shown in Figs. 10 and 12 in our circuit implementations. Vertical silicon nanowires are defined using the commercial SOI wafers and electron-beam lithography, with the width and thickness of a few tens of nanometers. After growing the gate oxide and ion implantation, junctionless nanowire transistors will be formed at the crosspoints [63]. The NWFETs are modeled in HSPICE using the output and the current-voltage characteristics along with the values given in Ref. [63]. The interconnecting nanowire can be modeled as a $\prod$-type wire shown in Fig. 14. Parameters of the crossbar used in our SPICE simulations are given in Table II. To make a fair comparison we have used 22-nm CMOS technology parameters from the predictive technology model (PTM) [64]. Transistor sizes were selected as $(W/L)=44$ nm/22 nm for both n-channel and p-channel MOSFETs. We created three cell libraries: CMOS library (C), nanowire crossbar library (NWC) and asymmetric nanowire crossbar library (ANWC). Each library consists of some basic logic

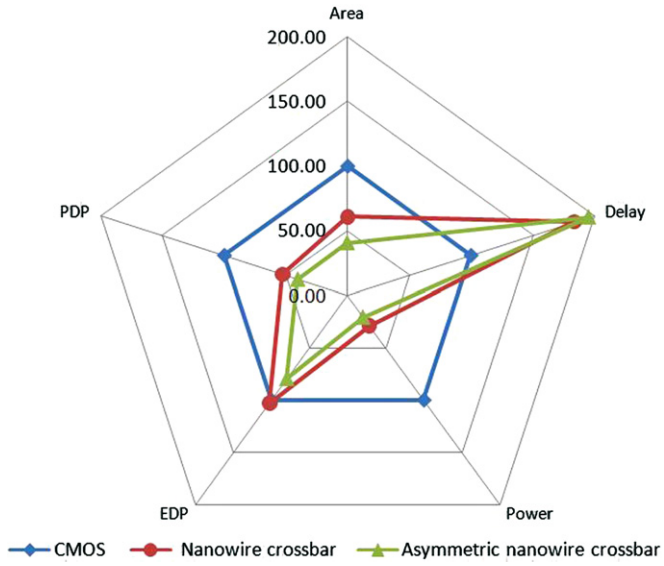

Fig. 16. Performance comparison of benchmark circuits for different architectures (values are in percent relative to CMOS).

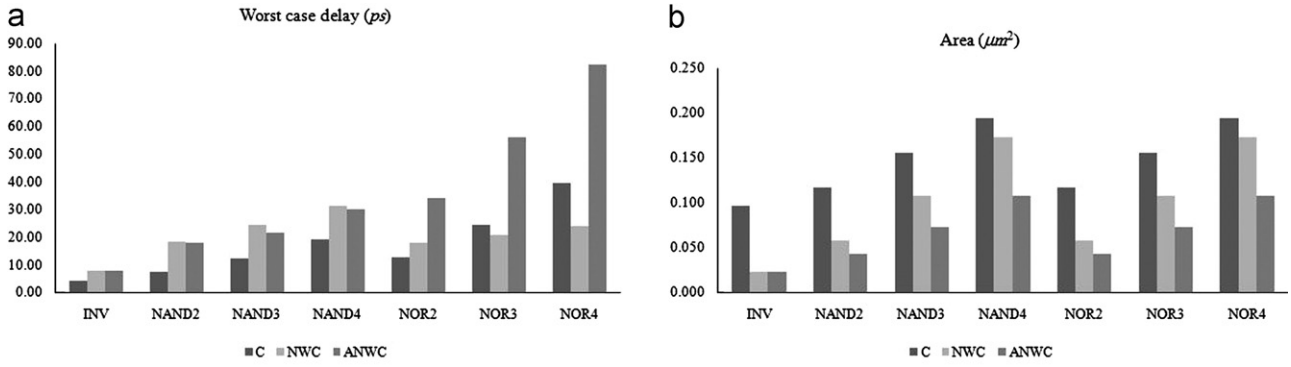

Fig. 15. Simulation results of basic logic gates, (a) worst case delay, (b) gate area.

Table IV
Simulation results of benchmark circuits.

Circuit	Area (μm^2)			Critical path delay (ps)			EDP (1e–23 Js)		
	C	NWC	ANWC	C	NWC	ANWC	C	NWC	ANWC
alu4	383	228	160	180	244	275	10.68	7.26	6.21
apex2	495	282	199	192	252	306	9.97	7.49	6.73
apex4	266	188	126	123	186	228	2.91	2.35	2.25
clma	2374	1348	920	367	681	685	113.33	108.41	82.53
diffeq	616	387	249	302	650	649	33.03	37.21	27.76
elliptic	1566	998	637	450	962	965	129.77	139.99	106.28
ex1010	934	660	433	178	248	308	7.00	5.05	5.06
ex5p	278	173	118	142	232	270	3.33	2.68	2.48
frisc	1473	922	605	585	1306	1325	132.85	152.09	116.20
misex3	372	216	150	142	223	257	5.82	5.07	4.37
pdc	1297	761	526	195	306	338	10.91	8.64	7.11
s298	465	294	204	339	523	615	26.52	21.51	19.18
S38417	2547	1548	1020	238	475	481	108.81	111.42	85.09
s38584.1	2277	1371	908	217	431	430	82.39	86.47	65.02
seq	470	268	186	146	212	250	7.42	5.74	5.43
spla	1037	615	416	185	270	314	9.10	6.78	6.09
tseng	587	331	216	288	644	651	27.99	31.63	23.93
Average	1025.71	622.94	416.06	251.12	461.47	491.00	42.46	43.52	33.63
Ratio (%)	100.00	60.73	40.56	100.00	183.77	195.53	100.00	102.49	79.20

gates including inverter (INV), 2-, 3-, and 4-input NAND and NOR gates (NAND2, NAND3, NAND4, NOR2, NOR3, and NOR4). The simulation results for $V_{dd}=0.8$ V and the load capacitance equal to the input capacitance of an inverter gate are given in Table III.

As it can be seen from the table, the crossbar cells have a smaller area since they exploit nanowire FETs which are smaller compared to MOSFETs. For example, the area of a 3-input NAND gate in the three libraries can be calculated as:

$$\text{CMOS}: \quad \text{Area} = 32\lambda \times 40\lambda, \quad (2\lambda = 22 \text{ nm})$$

$$\text{Nanowire crossbar}: \quad \text{Area} = (2n+m)(1+p+q)P_{nw}^2 = 30P_{nw}^2$$

$$\text{Asymmetric nanowire crossbar}: \quad \text{Area} = (n+1)(n+2)P_{nw}^2 = 20P_{nw}^2$$

The delay of the crossbar cell, as shown in Fig. 15a, is larger than the delay of CMOS cells in most gates, except for the 3- and 4-input CMOS NOR gates which have large input capacitance and many p-FETS in stack. The crossbar delay is directly related to n, dimension of nanowire crossbar [26], and increases with circuit complexity [65]. It is important to limit the dimension of logic cells to reduce the delay. The NAND gates implemented with the ANWC have smaller delay than their NWC counterparts, as shown in Fig. 15a. This is due to the fact that removing the PD parallel paths reduces the input capacitance while has no considerable effect on the PD circuit speed, since the n-FETS are fast enough. For the ANWC NOR gates, on the other hand, removing the parallel PU paths increase the gate delay. The area of the CMOS cells is larger than both NWC and ANWC cells (see Fig. 15b).

We used Toronto benchmark circuits and the SIS [66] synthesis tool to compare the performance of the crossbar and CMOS logics. We used our previously defined libraries: C, NWC and ANWC. As reported in Table IV nanowire crossbar architectures have smaller area compared to CMOS, while they have larger delay. The ANWC has better energy delay product (EDP) and power delay product (PDP) compared to CMOS and NWC circuits (see Fig. 16).

As can be inferred from the results, in a CMOS based circuit we can replace the elements in the non-critical paths with their crossbar cell counterparts to reduce circuit area and power consumption [26]. In addition, crossbar cells have lower capacitances, which in turn introduce lower load capacitance on the critical path. We have investigated the performance of the combination of CMOS and crossbar libraries for the benchmark circuits. We create three combined libraries as:

C-NWC: library of CMOS and nanowire crossbar cells,
C-ANWC: library of CMOS and asymmetric nanowire crossbar cells,
NWC-ANWC: library of nanowire crossbar and asymmetric nanowire crossbar cells.

Simulation results are given in Table V. As it can be seen from Fig. 17 the performance of the circuits improves with the combined libraries. The average area and EDP decrease using the C-NWC library

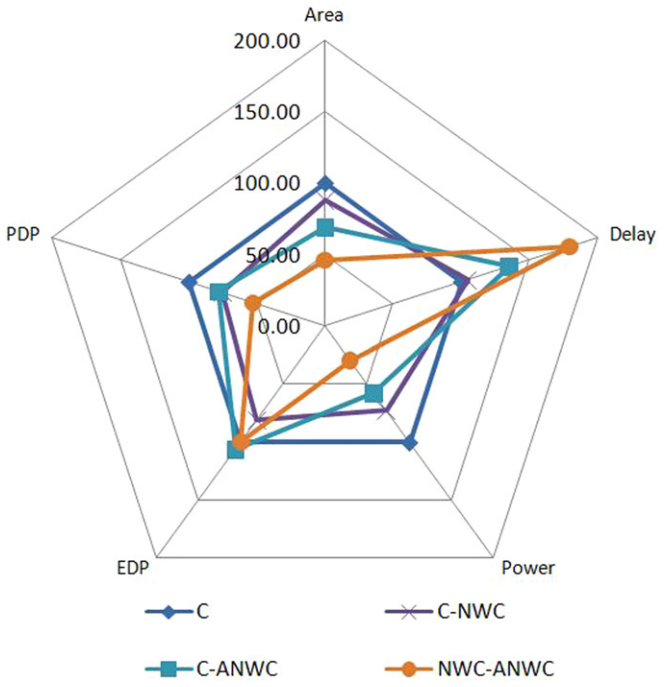

Fig. 17. Performance comparison of benchmark circuits for combined libraries (values are in percent relative to CMOS).

Table V
Simulation results of benchmark circuits using combined libraries.

Circuit	Area (μm^2)				Critical path delay (ps))				EDP (1e–23 Js			
	C	C-NWC	C-ANWC	NWC-ANWC	C	C-NWC	C-ANWC	NWC-ANWC	C	C-NWC	C-ANWC	NWC-ANWC
alu4	383	340	284	189	180	171	216	230	10.68	7.27	9.53	6.73
apex2	495	412	342	239	192	176	246	247	9.97	7.16	10.94	6.63
apex4	266	236	181	165	123	127	182	183	2.91	2.59	3.60	2.27
clma	2374	2159	971	1047	367	403	693	662	113.33	94.96	170.68	105.61
diffeq	616	540	472	273	302	315	399	642	33.03	26.79	33.85	36.79
elliptic	1566	1378	1182	700	450	439	464	957	129.77	93.33	102.08	138.41
ex1010	934	869	613	558	178	172	240	222	7.00	5.42	7.52	4.65
ex5p	278	244	192	140	142	153	202	237	3.33	2.74	3.78	2.92
frisc	1473	1296	1131	677	585	653	736	1272	132.85	111.88	129.08	146.20
misex3	372	309	253	178	142	143	203	214	5.82	5.02	7.15	5.09
pdc	1297	1209	1032	596	195	190	261	302	10.91	7.85	11.21	8.49
s298	465	393	338	245	339	364	480	506	26.52	21.00	29.01	20.13
s38417	2547	2147	1895	1114	238	266	330	467	108.81	92.17	115.48	110.23
s38584.1	2277	1923	1599	1018	217	244	296	411	82.39	71.52	88.55	81.22
seq	470	393	319	225	146	142	189	208	7.42	5.86	7.95	5.75
spla	1037	969	824	474	185	176	238	257	9.10	6.50	9.49	6.47
tseng	587	493	437	234	288	318	400	642	27.99	22.83	29.20	32.30
Average	1025.71	900.59	709.71	474.82	251.12	261.88	339.71	450.53	42.46	34.41	45.24	42.35
Ratio (%)	100.00	87.80	69.19	46.29	100.00	104.29	135.28	179.41	100.00	81.03	106.55	99.73

at the cost of 4% increase in the delay. With the C-ANWC library the area can be reduced about 30% at the expense of larger delay. Using the combined NWC-ANWC library will results in more than 50% area reduction, though its large delay may not be acceptable in most circuits.

6. Summary and conclusions

In this paper, we have addressed the application of the nanowire crossbar architecture in logic circuit implementation. Different crossbar nanoarchitectures are studied and compared. A comparative study has been then performed to evaluate the performance of the crossbar architecture compared to the traditional CMOS logic design. We have implemented some logic circuits using both FET-based crossbar array and CMOS approaches. The equivalent models of crossbar-based circuits have been simulated using HSPICE. The corresponding CMOS circuits have been also simulated using the 22-nm technology parameters with similar conditions. A comparison of simulation results show that the crossbar-based circuits have a much smaller area than their CMOS counterparts, while they show a higher delay. The area can be more reduced using the modified asymmetric nanowire crossbar architecture. The combined libraries of crossbar architecture and CMOS cells can exhibit better performance in terms of area and power with only small delay increase.

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