Update on Process Integration, Devices, & Structures (PIDS)

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Hsinchu, Taiwan

Rich Liu, Macronix

PIDS Roster

C=Chair, CC=Co-Chair, VC=Vice-Chair

US
Ng, Kwok[C]
Chang, Chorng-Ping[VC]
Antoniadis, Dimitri
Bhavnagarwala,Azeez
Brewer, Joe
Bersuker, Gennadi
Cheung, Kin (Charles)
Dellin, Ted
Fonseca, James
Gallagher, Bill
Henderson, Christopher
Hutchby, Jim
Klimeck, Gerhard
Krishnan, Shrikanth
Lam, Chung
Maszara, Witek
Ning, Tak
Potbhare, Siddharth
Prall, Kirk
Salmani Jelodar, Mehdi
Stathis, James
Tsai, Wilman
Wong, Philip
Xu, Yanzhong
Yeap, Geoffrey
Yu, Scott
Zeitzoff, Peter

Japan
Wakabayashi, Hitoshi[C]
Inoue, Hirofumi[VC]
Akasaka, Yasushi
Futatsugi, Toshiro
Gohou, Yasushi
Hayashi, Yoshihiro
Hiramoto, Toshiro
Hisamoto, Digh
Ida, Jiro
Iwamoro, Kunihiko
Kasai, Naoki
Koga, Akihiro
Kurata, Hajime
Mogami, Tohru
Niwa, Masaaki
Oda, Hidekazu
Ohguro, Tatsuya
Sugii, Toshihiro
Takagi, Shinichi
Tanaka, Tetsu
Yoshimi, Makoto

Europe
Boeuf, Frederic[C]
Burenkov, Alex
DeMeyer, Kristin
Jurczak, Malgorzata
Kuper, Fred
Lander, Robert
Poiroux, Thierry
Schulz, Thomas

Taiwan
Liu, Rich[CC]
Pan, Sam[CC]
Oates, Tony
Tsai, Cheng-tzung

Korea
Jeong, Moon-Young[C]
Oh, Sang Hyun
Park, Jongwoo

Outline

- PIDS Mission and Technical Sub-Groups
  1. Logic
  2. Memory: DRAM
  3. Memory: Non-Volatile Memory
  4. Reliability
- 2012 (minor) Edition Update
- Plans for 2013 (major) Edition

- **PIDS** =
  Process **I**ntegration, **D**evices, & **S**tructures
- Mission:
  - Forecast device technologies (15 years) in main-stream manufacturing and device specs, for digital/logic and memory technologies.
  - Provide physical and electrical requirements, and solutions to sustain scaling.
  - Scopes:
    - Performance (speed, density, power…)
    - Structures
    - Process-integration challenges
    - Reliability

PIDS Technical Sub-Groups

- Logic (Leads = Ng and Cheung)
  - HP = High Performance (speed) (e.g., μP…)
  - LOP = Low Operating (Dynamic) Power (e.g., notebook…)
  - LSTP = Low Standby (Static) Power (e.g., cellular…)
  - III-V/Ge = Alternate channel for low dynamic power and high speed

	HP	LOP	LSTP	III-V/Ge
Speed (I/CV)	Ref	lower	Lowest	Higher
Dynamic Power (CV^2)	Ref	Lowest	Lower	Lowest
Static Power (I_{off})	Ref	Lower	Lowest	Ref

- Memory: DRAM (Lead = Inoue)
- Memory: Non-volatile (Leads = Liu and Inoue) (Device types in next page)
- Reliability (Lead = Cheung)

Types of NVM

- 3-terminal charge-storage FET
  - Floating-gate (NOR and NAND)
  - Charge-trapping (NOR and NAND) (SONOS, MNOS…)
- 2-terminal non-charge-based
  - FeRAM
  - PCRAM
  - MRAM
  - STT-MRAM

2012 Update: Logic

- Per market announcement, pulled in FD-SOI and multi-gate (FinFET) to 2012.
- Below is for HP. Same done for LOP and LSTP.

Table PIDS2 High-performance (HP) Logic Technology Requirements

Year of Production	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*	*2023*	*2024*	*2025*	*2026*
L_g: Physical Lgate for HP Logic (nm) [1]	*22*	*20*	*18*	*17*	*15.3*	*14.0*	*12.8*	*11.7*	*10.6*	*9.7*	*8.9*	*8.1*	*7.4*	*6.6*	*5.9*
$I_{d,sat}$: NMOS Drive Current (μA/μm) [14]															
Extended Planar Bulk	1,367	1,422	1,496	1,582	1,670	1,775									
FD SOI		1,475	1,530	1,591	1,654	1,717	1,791	1,847	1,942						
MG				1,628	1,685	1,744	1,805	1,858	1,916	1,976	2,030	2,087	2,152	2,228	2,308
Revised for 2012 update															
Year of Production	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*	*2023*	*2024*	*2025*	*2026*
L_g: Physical Lgate for HP Logic (nm) [1]	*22*	*20*	*18*	*17*	*15.3*	*14.0*	*12.8*	*11.7*	*10.6*	*9.7*	*8.9*	*8.1*	*7.4*	*6.6*	*5.9*
$I_{d,sat}$: NMOS Drive Current (μA/μm) [14]															
Extended Planar Bulk	1,367	1,422	1,496	1,582	1,670	1,775									
FD SOI	1,415	1,475	1,530	1,591	1,654	1,717	1,791	1,847	1,942						
MG	1,469	1,520	1,573	1,628	1,685	1,744	1,805	1,858	1,916	1,976	2,030	2,087	2,152	2,228	2,308

2012 Update: DRAM

Based on survey performed by Japan PIDS, completed in March 2012.

- Half pitch unchanged (compared to 2011 version).
- Cell size factor transition from $6F^2$ to $4F^2$ in 2014, delayed by 1 year.
- Vertical channel transistor will be launched in 2014, in place of recessed channel, delayed by 1 year, and continues till end of roadmap.

Table PIDS7 DRAM Technology Requirements

		Year in Production	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026
	ITRS 2012	DRAM ½ Pitch (nm) [1]	31	28	25	22	20	18	16	14	13	12	11	10	9	7	6
WAS	*ITRS 2011*	DRAM cell FET structure [6]	FinFET	VCT	VCT	VCT	VCT	VCT	VCT	VCT	VCT	VCT	VCT	VCT	VCT		
IS	*ITRS 2012*		RCAT+Fin	RCAT+Fin	VCT	VCT	VCT	VCT	VCT	VCT	VCT	VCT	VCT	VCT	VCT	VCT	VCT
WAS	*ITRS 2011*	Cell Size Factor: a [11]	6	4	4	4	4	4	4	4	4	4	4	4	4	4	4
IS	*ITRS 2012*		6	6	4	4	4	4	4	4	4	4	4	4	4	4	4

2012 Update: Non-Volatile Memory

Based on survey performed by Japan PIDS, completed in March 2012, together with market observations.

- Compared to 2011 Edition, half-pitch scaling is unchanged.
- Some revisions for FeRAM (cell size, switching charge density…).

NAND Flash														
Year of Production	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*	*2023*	*2024*	*2025*
Uncontacted poly 1/2 pitch (nm)	**20**	**18**	**17**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**8**	**8**	**8**
Number of word lines in one NAND string	**64**	**64**	**64**	**64**	**64**	**64**	**64**	**64**	**64**	**64**	**64**	**64**	**64**	**64**
Dominant Cell type	**FG**	**FG**	**FG/CT**	**FG/CT**	**CT-3D**	**CT-3D**	**CT-3D**	**CT-3D**	**CT-3D**	**CT-3D**	**CT-3D**	**CT-3D**	**CT-3D**	**CT-3D**
Maximum number of bits per chip (SLC/MLC)					**128G / 256G**	**256G / 512G**	**256G / 512G**	**512G / 1T**	**512G / 1T**	**512G / 1T**	**1T / 2T**	**1T / 2T**	**1T / 2T**	**2T / 4T**
Minimum array 1/2 pitch - F(nm) [15]					**32nm**	**32nm**	**32nm**	**28nm**	**28nm**	**28nm**	**24nm**	**24nm**	**24nm**	**18nm**
Number of 3D layers for array at minimum 1/2 array pitch [16]					**8**	**16**	**32**	**32**	**64**	**64**	**98**	**98**	**98**	**128**

2012 Update: Non-Volatile Memory

Based on survey performed by Japan PIDS, completed in March 2012, together with market observations.

- Compared to 2011 Edition, half-pitch scaling is unchanged.
- Some revisions for FeRAM (cell size, switching charge density…).

	A. FeRAM (Ferroelectric RAM)															
	Year of Production	*2012*	*2013*	*2014*	*2015*	*2016*	*2017*	*2018*	*2019*	*2020*	*2021*	*2022*	*2023*	*2024*	*2025*	*2026*
Was	*FeRAM technology node – F (nm) [1]*	180	130	130	130	130	90	90	90	90	65	65	65	65	65	65
Is		130	130	130	130	90	90	90	90	90	65	65	65	65	45	45
Was	*FeRAM cell size – area factor a in multiples of F2 [2]*	22	16	16	16	16	14	14	14	14	12	12	12	12	12	12
Is		23	23	23	23	22	22	22	22	22	15	15	15	15	13	13
Was	*FeRAM cell size (µm2)*	0.713	0.27	0.27	0.27	0.27	0.113	0.113	0.113	0.113	0.051	0.051	0.051	0.051	0.051	0.051
Is		0.71	0.71	0.71	0.71	0.4	0.4	0.4	0.4	0.4	0.169	0.169	0.169	0.169	0.081	0.081
Was	*FeRAM capacitor structure [4]*	stack	stack	stack	stack	stack	3D	3D	3D	3D	3D	3D	3D	3D	3D	3D
Is		stack	stack	stack	stack	stack	stack	stack	stack	stack	3D	3D	3D	3D	3D	3D
Was	*FeRAM capacitor footprint (µm2) [5]*	0.33	0.106	0.106	0.106	0.106	0.041	0.041	0.041	0.041	0.016	0.016	0.016	0.016	0.016	0.016
Is		0.423	0.423	0.423	0.423	0.234	0.234	0.234	0.234	0.234	0.087	0.087	0.087	0.087	0.039	0.039
Was	*FeRAM capacitor active area (µm2) [6]*	0.33	0.106	0.106	0.106	0.106	0.1	0.1	0.1	0.1	0.069	0.069	0.069	0.069	0.069	0.069
Is		0.423	0.423	0.423	0.423	0.234	0.234	0.234	0.234	0.234	0.175	0.175	0.175	0.175	0.155	0.155
Was	*FeRAM cap active area/footprint ratio [7]*	1	1	1	1	1	2.46	2.46	2.46	2.46	4.25	4.25	4.25	4.25	4.25	4.25
Is		1	1	1	1	1	1	1	1	1	2	2	2	2	4	4
Was	*Ferro capacitor voltage (V) [8]*	1.5	1.2	1.2	1.2	1.2	1	1	1	1	0.7	0.7	0.7	0.7	0.7	0.7
Is		1.5	1.5	1.5	1.5	1.2	1.2	1.2	1.2	1.2	1.0	1.0	1.0	1.0	1.0	1.0
Was	*FeRAM minimum switching charge density (µC/cm2) [9]*	13.5	34	34	34	34	30	30	30	30	30	30	30	30	30	30
Is		8.5	8.5	8.5	8.5	12.0	12.0	12.0	12.0	12.0	13.0	13.0	13.0	13.0	11.5	11.5

2012 Update: Reliability

No change.

Plans for 2013 Edition

- To address low-power requirement, and with chip clock frequency increase-per-year has slowed down, transistor speed CV/I slope will be decreased from 13%/yr. Consequences: Lower V_{dd} and/or relaxed gate length.
- Start to use Purdue University TCAD tools (NanoHub) to project device characteristics, along with MASTAR.
- New websites within NanoHub will be created for interactive tools and files for public access.
- LOP will be dropped. LSTP will be renamed as LP (Low power), the only low-power technology.
- Consider adding new parameter in logic to reflect layout advantage (higher current per area) of FinFET, by $V_{dd}/I_{on}/W_{footprint}$.
- Longer-term: Compact models are considered to be added for circuit simulation.

Some Take-Away Comments

Logic:

- No theoretical scaling limit seen yet for Si (to 2026, gate length ~6 nm).
- Power is the limiting factor, not speed. Device speed requirement is relaxed from circuit perspectives.
- Alternative channel III-V/Ge can offer lower power with similar speed.
- Low V_{dd} near end of roadmap (~0.5 V) posts noise/variability challenges.
- Series resistance can be a practical limitation.

DRAM:

- Capacitor scaling increasingly difficult.
- $4F^2$ is the limit for cell size.

NVM:

- Many cell versions:
  - 3-terminal (charge-based): Floating-gate and charge-trapping FETs still dominate. 3-D projected.
  - 2-terminal (non-charge-based): FeRAM, PCRAM, MRAM, STT-RAM, for more diverse applications. Efficient selection device needs to be developed and integrated.

End