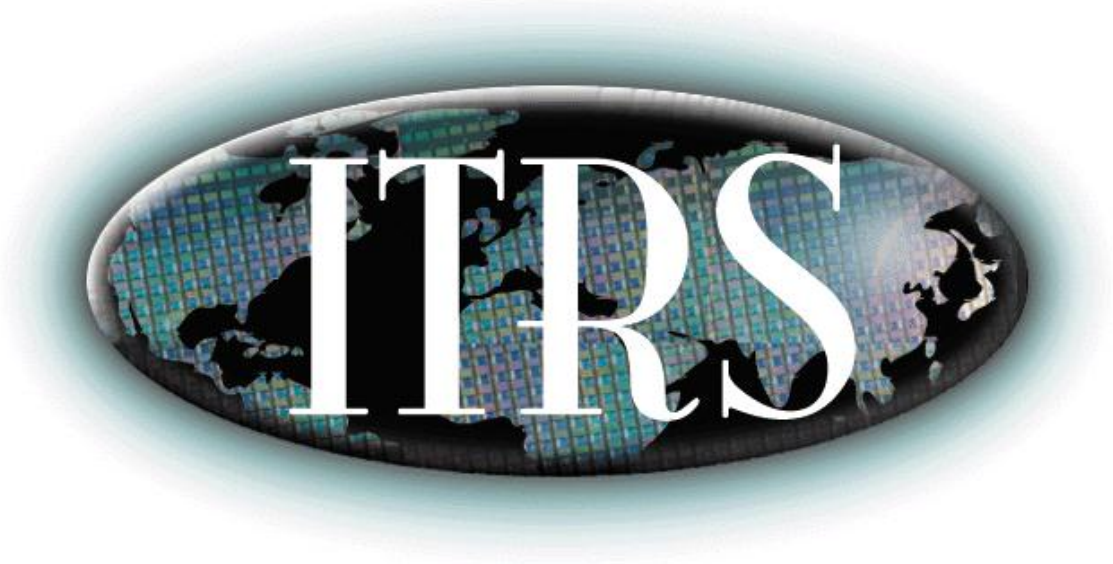

INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS

2012 UPDATE OVERVIEW

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Semiconductor Industry Association

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INTERNATIONAL ROADMAP COMMITTEE

◈*Europe*—Patrick Cogez, Mart Graef, Bert Huizing, Reinhard Mahnkopf
◈*Japan*—Hidemi Ishiuchi, Junji Shindo
◈*Korea*—Siyoung Choi, Jae Hoon Choi,
◈*Taiwan*—Carlos H. Diaz, Yee Chaung See
◈*U.S.A.*—Bob Doering, Paolo Gargini, Taffy Kingscott, Ian Steff

TECHNOLOGY WORKING GROUP KEY CONTRIBUTORS

2012 Cross TWG Study Group (Technology Pacing)—Alan Allan, Joel Barnett, Roger Barth, Herb Bennett, Bill Bottoms, Juan-antonio Carballo, David Chan, Carlos Diaz, Alain Diebold, Bob Doering, Paul Feeney, Mike Garner, Dan Herr, Jim Hutchby, Hirofumi Inoue, Raj Jammy, Scott Jones, Andrew Kahng, Mike Lercel, Rich Liu, Jurgen Lorenz, Mark Neisser, Kwok Ng, Jack Pekarik, Lothar Pfitzner, Gopal Rao, Thomas Skotnicki, Hitoshi Wakabayashi, Mike Walden, Linda Wilson, Osamu [Sam] Yamazaki, Victor Zhirnov, Paul Zimmerman

2012 Cross TWG Study Group (More than Moore)—Herbert Bennett, Bill Bottoms, Michel Brillouët, Juan-Antonio Carballo, Patrick Cogez, Michael Gaitan, Mart Graef, Bert Huizing, Andrew Kahng, Reinhard Mahnkopf, Jack Pekarik

System Drivers and Design—Yoshimi Asada, Valeria Bertacco, Colin Bill, Ralf Brederlow, Yu Cao, Juan Antonio Carballo, John Darringer, Wolfgang Ecker, Dale Edwards, Eric Flamand, Paul Franzon, Masaharu Imai, Kwangok Jeong, Bill Joyner, Andrew Kahng, Masaru Kakimoto, Jong Ho Kang, Victor Kravets, Frederic Lalanne, Jingwei Lu, Vinod Malhotra, Masami Matsuzaki, Alfonso Maurelli, Nikil Mehta, Katsutoshi Nakayama, Sani Nassif, Nobuto Ono, Sam Pa, Ralf Pferdmenges, Shishpal Rawat, Wolfgang Rosenstiel, Toshitada Saito, Jean Pierre Schoellkopf, Gary Smith, Peter Van Staa, Leon Stok, Shireesh Verma, Maarten Vertregt, Alfred Wong, David Yeh, Hak soo Yu, Ichiro Yamamoto

Test and Test Equipment—Kenichi Anzou, Dave Armstrong, John Aslanian, Roger Barth, Yi Cai, Krishnendu Chakrabarty, Tapan Chakraborty, Sreejit Chakravarty, Wendy Chen, William Chui, Steve Comen, Zoe Conroy, Adam Cron, Al Crouch, Ted Eaton, Stefan Eichenberger, Bill Eklow, Paul Emmett, Ira Feldman, Francois-Fabien Ferhani, Shawn Fetterolf, Paul Franzon, Piergiorgio Galletta, Anne Gattiker, Sandeep Goel, Kazumi Hatayama, Hirokazu Hirayama, Hisao Horibe, Shuichi Ito, Hongshin Jun, Masahiro Kanase, Rohit Kapur, Toshiaki Kato, Brion Keller, Ajay Khoche, Satoru Kitagawa, Marc Knox, Masashi Kondo, Ken Lanier, Lenny Leon, Marc Loranger, Erik Jan Marinissen, Peter Maxwell, Cedric Mayor, Teresa McLaurin, Milanjan Mukherjee, Takeshi Nagasaka, Masaaki Namba, Naoaki Narumi, Phil Nigh, Akitoshi Nishimura, Hermann Obermeir, Jayson Park, Mike Peng-Li, Frank Poehl, Chris Portelli-Hale, Bill Price, Herb Reiter, Mike Ricchetti, Michael Rodgers, Tomonori Sasaki, Keno Sato, Masayuki Sato, Yasuo Sato, Ryuji Shimizu, Yoichi Shimizu, Fumio Sonoda, Hiroyoshi Suzuki, Tetsuo Tada, Satoru Takeda, Steven Tilden, Erik Volkerink, Adam Wright, Yervant Zorian

Process Integration, Devices, and Structures—Yasushi Akasaka, Dimitri Antoniadis, Gennadi Bersuker, Azeez Bhavnagarwala, Frederic Boeuf, Joe Brewer, Alex Burenkov, Chorng-Ping, Kin (Charles) Cheung, Ted Dellin, Kristin DeMeyer, James Fonseca, Toshiro Futatsugi, Bill Gallagher, Yasushi Gohou, Yoshihiro Hayashi, Christopher Henderson, Toshiro Hiramoto, Digh Hisamoto, Jim Hutchby, Jiro Ida, Hirofumi Inoue, Kunihiko Iwamoro, Moon-Young Jeong, Malgorzata Jurczak, Naoki Kasai, Gerhard Klimeck, Akihiro Koga, Shrikanth Krishnan, Fred Kuper, Hajime Kurata, Chung Lam, Robert Lander, Rich Liu, Witek Maszara, Tohru Mogami, Kwok Ng, Tak Ning, Masaaki Niwa, Tony Oates, Hidekazu Oda, Sang Hyun Oh, Tatsuya Ohguro, Sam Pan, Jongwoo Park, Thierry Poiroux, Siddharth Potbhare, Kirk Prall, Mehdi Salmani Jelodar, Thomas Schulz, James Stathis, Toshihiro Sugii, Shinichi Takagi, Tetsu Tanaka, Cheng-tzung Tsai, Wilman Tsai, Hitoshi Wakabayashi, Philip Wong, Yanzhong Xu, Geoffrey Yeap, Makoto Yoshimi, Scott Yu, Peter Zeitzoff

Radio Frequency and Analog/Mixed-signal Technologies—Carsten Ahrens, Kamel Benaissa, Herbert Bennett, Bobby Brar, Wayne Burger, Pascal Chevalier, David Chow, Steve Cosentino, Julio Costa, Mattias Dahlstrom, Hormoz Djahanshahi, Ali Eshraghi, Emerson Fang, Natalie Feilchenfeld, Toshiro Futatsugi, Brian Gerson, Evgeni Gousev, Yoshihiro Hayashi, Digh Hisamoto, Anthony Immorlica Jr., Snezana Jenei, Jay John, Michael Judy, Alex Kalnitsky, Tom Kazior, Taffy Kingscott, Ginkou Ma, Jan-Erik Mueller, Wibo van Noort, Hansu Oh, Tatsuya Ohguro, Douglas Pattullo, Jack Pekarik, Ed Preisler, Jean-Olivier Plouchart, Mina Rais-Zadeh, David Robertson,

Michael Schroeter, Sam Shichijo, Kaneyoshi Takeshita, Sorin Voinigescu, Albert Wang, Dawn Wang, Craig Wilson, Geoffrey Yeap, David Yeh, Ian Young, Peter Zampardi, Jiangkai Zuo

Microelectromechanical Systems (MEMS)—Chris Apanius, Matt Apanius, Stephen Bart, Raji Baskaran, Herbert Bennett, Steve Breit, Scott Bryant, Kevin Chau, Wendy Chen, Asif Chowdhury, Edward Chu, Mark Crockett, Roberto de Nuccio, Ingrid De Wolf, Stephane Donnay, Wei Leun Fang, Alissa Fitzgerald, Koji Fukumoto, Nakazawa Fumihi, Michael Gaitan, Brian Gerson, Raj Gupta, Buzz Hardy, Ron Horwath, Dave Howard, Brian Jamieson, Akihiro Koga, Rakesh Kumar, Ron Lawes, Karen Lightman, Pete Loeppert, Erik Jan Lous, Mary Ann Maher, Jainmin Miao, Takashi Mihara, Veljko Milanovic, Josh Molho, Arthur Morris, Jim Mrvos, Yasutaka Nakashiba, Goro Nakatani, Rob O'Reilly, Fabio Pasolini, Mervi Paulasto-Kröckel, Jack Pekarik, Dimitrios Peroulis, Christian Rembe, Sascha Revel, Chuck Richardson, Philippe Robert, John Rychcik, Patric Salomon, Dominique Schinabeck, Jim Spall, Tony Stamper, Monica Takacs, Tetsu Tanaka, Wallace Tang, Robert Tasi, Steve Tilden, Hiroshi Toshiyoshi, Joost van Beek, Henne van Heeren, Chris van Hoof, Fabrice Verjus, Randy Wagner, Steve Walsh, Marcie Weinstein, Xiaoming Wu, Jaesung Yoon

Emerging Research Devices—Hiro Akinaga, Tetsuya Asai, Yuji Awano, George Bourianoff, Geoffrey Burr, Michel Brillouet, John Carruthers, Ralph Cavin, Chorn-Ping Chang, An Chen, U-In Chung, Byung Jin Cho, Sung Woong Chung, Luigi Colombo, Shamik Das, Antoine Khoueir, Simon Deleonibus, Bob Doering, Tetsuo Endoh, Bob Fontana, Paul Franzon, Akira Fujiwara, Mike Garner, Dan Hammerstrom, Wilfried Haensch, Tsuyoshi Hasegawa, Shigenori Hayashi, Dan Herr, Mutsuo Hidaka, Toshiro Hiramoto, Jim Hutchby, Adrian Ionescu, Kiyoshi Kawabata, Seiichiro Kawamura, Suhwan Kim, Hyoungjoon Kim, Atsuhiro Kinoshita, Dae-Hong Ko, Gwan-hyeob Koh, Hiroshi Kotaki, Franz Kreupl, Mark Kryder, Zoran Krivokapic, Kee-Won Kwon, Jong-Ho Lee, Lou Lome, Matthew Marinella, Hiroshi Mizuta, Kwok Ng, Fumiyuki Nihei, Dmitri Nikonov, Kei Noda, Ferdinand Peper, Yaw Obeng, Yutaka Ohno, Dave Roberts, Shintaro Sato, Barry Schechtman, Sadas Shankar, Kaushal Singh, Takahiro Shinada, Masayuki Shirane, Thomas Skotnicki, Satoshi Sugahara, Shin-ichi Takagi, Ken Uchida, Thomas Vogelsang, Yasuo Wada, Rainer Waser, Jeff Welser, Frans Widershoven, Philip Wong, Dirk Wouters, Kojiro Yagami, David Yeh, In-Seok Yeo, Hiroaki Yoda, In-K Yoo, Victor Zhimov

Emerging Research Materials—Hiro Akinaga, Jesus de Alamo, Dimitri Antoniadis, Nobuo Aoi, Masakazu Aono, Bernd Appelt, Koyu Asai, Asen Asenov, Yuji Awano, David Awschalom, Rama Ayothi, Kaustav Banerjee, Chris Bencher, Agnès Barthélémy, Daniel-Camille Bensahel, Kris Bertness, Stacey Bent, Mikael Björk, August Bosse, Bill Bottoms, George Bourianoff, Rod Bowman, Alex Bratkovski, Robert Bristol, Ahmed Busnaina, Jeff Calvert, John Carruthers, Bernie Capraro, David Chan, An Chen, Eugene Chen, Zhihong Chen Joy, Cheng, Toyohiro Chikyow, Byung Jin Cho, U-In Chung, Jonathan Coleman, Luigi Colombo, Johann Coraux, Hongjie Dai, Ralph Dammel, Juan DePablo, Anton Devilliers, Thibaut Devolder, B. Dieny, Jean Dijon, Athanasios Dimoulas, Geraud Dubios, Catherine Dubourdieu, John Ekerdt, Tetsuo Endoh, James Engstrom, Thomas Ernst, Michael Flatte, Glenn Fredrickson, Nathan Fritz, Gregory Fuchs, Satoshi Fujimura, C. Michael Garner, Emmanuel Giannelis, Andrew Grenville, Niti Goel, Michael Goldstein, Suresh Golwalkar, Guido Groeseneken, Roel Gronheid, Wilfried Haensch, Cliff Henderson, Daniel Herr, Hiro Hibino, Marc Hillmyer, Bill Hinsberg, Toshiro Hiramoto, Judy Hoyt, Greg Hughes, Jim Hutchby, Harold Hwang, Hyunsang Hwang, K. Inoue, Takamasa Ishigaki, Saori Ishizu, Nobuyuki Ishiwata, Yoshio Ishiwata, Kohei Ito, Taisuke Iwai, Ajey Jacob, Raj Jami, David Jamieson, Ali Javey, James Jewett, Berry Jonker, Xavier Joyeux, Yeon Sik Jung, Ted Kamins, Zia Karim, Takashi Kariya, Takashi Kariya, Masashi Kawaski, Leo Kenny, Richard Klein, Choong-un Kim, Philip Kim, Sang Ouk Kim, Sean King, Atsuhiro Kinoshita, Paul Kohl, Gabriel Kotliar, Michael Kozicki, Victor Krivokapic, Mark Kryder, Yi-Sha Ku, Hiroshi Kumigashira, Nabil Laachi, Roger Lake, Steve Lange, Jang Ein Lee, Yi Jun Lee, Harry Levinson, Chenhsin Lien, Liew Yun Fook, Scott List, Lloyd Litt, Chi Chun Liu, Wei-Chung Lo, Louis Lome, Timothy E. Long, Gerry Lucovsky, Mark Lundstrom, Yale Ma, Allan MacDonald, Blanka Magyari-Kope, Prashant Majhi, Arun Majumdar, Francois Martin, Lane Martin, Witek Maszara, Jennifer McKenna, Fumihiro Matsukura, Nobuyuki Matsuzawa, Claudia Mewes, Dan Millward, Yoshiyuki Miyamoto, Stephane Monfray, Andrea Morello, Mick Morris, Azad Naeemi, Boris Naydenov, C. Gomez-Navarro, Paul Nealey, Kwok Ng, Mark Niesser, Fumiyuki Nihey, Mizuhisa Nihey, Yoshio Nishi, Kei Noda, Yaw Obeng, Chris Ober, Matsuto Ogawa, Katsumi Ohmori, Yutaka Ohno, Laurent Pain, Ray Pearson, Jeff Peterson, Mark Phillips, Er-Xuan Ping, Joel Plawski, Alexei Preobrajenski, Victor Pushparaj, Ganapati Ramanath, Ramamoorthy Ramesh, Nachiket Raravikar, Ben Rathsack, Curt Richter, Heike Riel, Dave Roberts, Sven Rogge, Jae Sung Roh, Ricardo Ruiz, Thomas Russell, Tadashi Sakai, Gurtej Sandhu, Krishna Saraswat, Chandra Sarma, Hideyuki Sasaki, Mitusru Sato, Shintaro Sato, Barry Schechtman, Thomas Schenkel, Jan Seidel, Sadasivan Shankar, Matthew Shaw, Takahiro Shinada, Michelle Simmons, K. Singer, Kaushal K. Singh, Jon Slaughter, Mark Slezak, Bruce Smith, Tom Smith, Mark Somervell, Mark Stiles, Tsung-Tsan Su, Maki Suemitsu, Naoyuki Sugiyama, Chun-Yung Sung, Raja Swaminathan, Michiharu Tabe, Hidenori Takagi, Shin-ichi Takagi, Masahiro Takemura, Koki Tamura, Shinji Tarutani, Jim Thackeray, Raluca Tiron,

Yoshihiro Todokoro, Yasuhide Tomioka, Peter Trefonas, Ming-Jinn Tsai, Wilman Tsai, Vincent Tung, King Tu, Mark Tuominen, Ken Uchida, Marc Ulrich, Philippe Vereecken, Yasuo Wada, Vijay Wakharkar, Kang Wang, Weie Wang, Zhong Lin Wang, Rainer Waser, Jeff Welser, Lars-Erik Wernersson, Andrew Whittaker, Grant Willson, C.P. Wong, H.S. Philip Wong, Dirk Wouters, Wen-Li Wu, Hiroshi Yamaguchi, Toru Yamaguchi, Chin-Tien Yang, Kenji Yoshimoto, Yi-Sha Yu, SC Zhang, Yuegang Zhang, Jiro Yugami, Shigeru Yamada, Victor Zhirnov, Paul Zimmerman, Chuck Zmanda

Front End Processes—Mauro Alessandri, Sehgal Aksey, John Arnold, Souvik Banerjee, Joel Barnett, Twan Bearda, Meridith Beebe, Steve Benner, Ivan (Skip) Berry, Chris Borst, John Boyd; Ian Brown, Arifin Budihardio, George Celler, Luke Chang, Victor Chia, Ho Jin Cho, Phil Clark, Lee Cook, Jeffrey Cross, Adrien Danel, Suman Datta, Carlos H. Diaz, Paul Feeney, Nicholas Fuller, Mike Fury, Yehiel Gotkis, Mike Goldstein, Christina Gottschalk, Aomar Halimaoui, Qingyuan Han, Chris Hobbs, Andrew Hoff, Yoshimasa Horii, Dick James; Raj Jammy, Andreas Kadavanich, Ravi Kanjolia, Hyungsup Kim, Simon Kirk, Brian Kirkpatrick, Hiroshi Kitajima, Martin Knotter, Daniel Koos, Hwasung Kyunggi-Do, Larry Larson, Jeff Lauerhaas, Yannick Le Tiec, Kuntack Lee, Jooh Yun Lee, Tom Lii, Hong Lin, Wei-Yip Lo, Prashant Majhi, Tom McKenna, Kevin McLaughlin, Paul Mertens, Katsuhiko Miki, Ichiro Mizushima, Mansour Monipour, Paul Morgan, Anthony Muscat, Sadao Nakajima, Yasuo Nara, Bich-Yen Nguyen, Masaaki Niwa, Toshihide Ohgata, Hiroshi Oji, Jin-Goo Park, Friedrich Passek, Eric Persson, Darryl Peters, Gerd Pfeiffer, Er-Xuan Ping, Jagdish Prasad, Srini Raghavan, Maud Rao, Rick Reidy, Karen Reinhardt, Hwa-sung Rhee, Rob Rhoades, Marcello Riva, Jae-Sung Roh, Akira Sakai, Archita Sengupta, YugYun Shin, James Shen, Wolfgang Sievert, Chris Sparks, Robert Standley, Sing-Pin Tay, Bob Turkot, Allan Upham, Steven Verhaverbeke, Rita Voss, Hitoshi Wakabayashi, Mike Walden, Masaharu Watanabe, Han Xu

Lithography—Chris Bencher, Tatsuo Chijimatsu, Will Conley, Nigel Farrar, Ted Fedynyshyn, Heiko Feldmann, Reiner Garreis, Cesar Garza, Bob Gleason, Frank Goodwin, Roel Gronheid, Naoya Hayashi, Iwao Higashikawa, Rik Jonckeere, Franklin Kalk, Kunihiko Kasama, Y.C. Ku, Keishiro Kurihara, Jongwook Kye, David Kyser, Michael Lercel, ChangMoon Lim, Lloyd Litt, Greg McIntyre, Hiroaki Morimoto, Seiji Nagahara, Hideo Nakashima, Mark Neisser, Katsumi Ohmori, Yasushi Okubo, Masahiko Okumura, Eric Panning, Moshe Preil, Doug Resnick, Morty Rothschild, Masaru Sasago, Osamu Suga, Kazuhiro Takahashi, Serge Tedesco, Walt Trybula, Takayuki Uchiyama, Fumikatsu Uesawa, Mauro Vasconi, Keiji Wada, Phil Ware, John Wiesner, Jim Wiley, Grant Willson, Stefan Wurm, Jiro Yamada, Tetsuo Yamaguchi, Anthony Yen, JeongHo Yeo, John Zimmerman

Interconnect—Nobuo Aoi, Lucile Arnaud, Koji Ban, Hans-Joachim Barth, Eric Beyne, Boyan Boyanov, Jon Candelaria, Chung-Liang Chang, Hsien-Wei Chen, Wen-Chih Chiou, Gilheyun Choi, Jinn-P. Chu, Mike Corbett, Alexis Farcy, Paul Feeney, Takashi Hayakawa, Paul Ho, Cheng-Chieh Hsieh, Masayoshi Imai, Atsunobu Isobayashi, Raymond Jao, Shin-Puu Jeng, Morihiro Kada, Sibum Kim, Nobuyoshi Kobayashi, Kaushik Kumar, Nohjung Kwak, Hyeon Deok Lee, Anderson Liu, Didier Louis, James Lu, Toshiro Maekawa, David Maloney, Akira Matsumoto, Azad Naeemi, Mehul Naik, Tomoji Nakamura, Yuichi Nakao, Akira Ouchi, Sesh Ramaswami, Hideki Shibata, Michele Stucchi, Zsolt Tokei, Thomas Toms, Manabu Tsujimura, Kazuyoshi Ueno, Osamu Yamazaki, Paul Zimmerman

Factory Integration—Niall Aughney, Daniel Babbs, Jonathan Chang, Al Chasey, Gino Crispieri, Peter Csatary, Boyd Finlay, Francesca Illuzzi, Leo Kenny, Shige Koyabashi, Les Marshall, Supika Mashiro, Dan Mcculley, Reiner Missale, Steve Moffatt, James Moyne, Andreas Neuber, Richard Oechsner, Markus Pfeffer, Gopal Rao, Eric-Paul Schat, Jan-Willem Scheijgrond, Michael Schilp, Dan Stevens, Harry Thewissen, Makato Yamamoto

Assembly and Packaging—Sai Ankireddi, Bernd Appelt, Thomas Baer, Muhannad S. Bakir, Souvik Banarjee, Hans-Joachim Barth, Steve Bezuk, W.R. Bottoms, William Burdick, Yi-jen Chan, Carl Chen, William Chen, Sonjin Cho, Yulkyo Chung, Bob Chylak, Horst Clauberg, Krishor Desai, Dan Evans, Bradford Factor, Tatsuhiro Fujiki, Michel Garnier, Steve Greathouse, Tom Gregorich, Richard Grzybowski, George Harman, Tomoo Hayashi, Willem Hoving, Mike Hung, John Hunt, T. S. Hwang, Kazuyuki Imamura, Dan Kilper, Mitchitaka Kimura, Shoji Kitamura, Tzu-Kun Ku, Choon Heung Lee, Ricky S W Lee, Rong-Shen Lee, Russell Lewis, Sebastian Liau, Weichung Lo, Debendra Mallik, Kaneto Matsushita, Stan Mihelcic, David Miller, Hirofumi Nakajima, Keith Newman, Gary Nicholls, Grace Omalley, John Osenbach, Richard F. Otte, Bob Pfahl, Gilles Poupon, Klaus Pressel, Gamal Refai-Ahmed, Charles Reynolds, Charles Richardson, Philippe Robert, Peter Robinson, Bernd Roemer, Mark De Samber, Gurtej Sandu, Robert Sankman, Naoto Sasaki, Shahriar Shahramian, Vern Solberg, Kaoru Sonobe, Simon Stacey, Freek Van Straten, Yoshiaki Sugizaki, Teresa Sze, Coen Tak, Patrick Thompson, Andy Tseng, Shigeyuki Ueda, Henry Utsunomiya, Kripesh Vaidyanathan, Julien Vittu, James Wilcox, Max Juergen Wolf, Jie Xue, Hiroyoshi Yoshida

Environment, Safety, and Health—Laurie Beu, Hans-Peter Bipp, Paul Connor, Reed Content, Shane Harte, Bob Helms, Dan Herr, Nausikaa Van Hoornick, Jim Field, Terry Francis, Mike Garner, Tom Huang, FM Hsu, Francesca Illuzzi,

Debra Kaiser, Leo Kenny, Alan, Knapp, SJ Ko, Hsi-An Kwong, Chris Lee, Slava Libman, Joey Liu, Mary Majors, Dave Maloney, Supika Mashiro, Toshi Matsuda, Steve Moffatt, Andreas Neuber, Alain Pardon, Gopal Rao, Reyes Sierra, Dave Speed, Masahiro Takemura, Harry Thewisson, Pete Trefonas, Ken Wei, Kurt Werner, Walter Worth, Paul Zimmerman

Yield Enhancement—Scott Anderson, Dwight Beal, David Blackford, Yannick Bordel, Marc Camezind, Jan Cavelaars, Jeff Chapman, Hubert Chu, Robert Clark, John DeGenova, Charley Dobson, Arnaud Favre, Guiseppe Fazio, Francois Finck, Dan Fuchs, Takashi Futatsuki, Guillaume Gallet, Delphine Gerin, Astrid Gettel, Rick Godec, Milton Goldwin, Barry Gotlinsky, Mathias Haeuser, Asad Haider, Jeff Hanson, Teruyuki Hayashi, Christoph Hocke, Masahiko Ikeno, Francesca Illuzzi, Hans Jansen, Jost Kames, Barry Kennedy, Keith Kerwin, Suhas Ketkar, Y.J. Kim, Katsunobu Kitami, Kaoru Kondoh, Naoki Kotani, John Kurowski, Sumio Kuwabara, Bob Latimer, Ravi Laxman, Slava Libman, Rushikesh Matkar, Yasuhiko Matsumoto, Fumio Mizuno, William Moore, Chris Muller, Hiroshi Nagaishi, Andreas Neuber, Kazuo Nishihagi, Andreas Nutsch, Kevin Pate, Dilip Patel, Ruben Pessina, Lothar Pfitzner, Larry Rabellino, Dieter Rathei, Rich Riley, David Roberts, Biswanath Roy, Koichiro Saga, Hideyuki Sakaizawa, Tony Schleisman, Yoshimi Shiramizu, Drew Sinha, Terry Stange, Isamu Sugiyama, Paul Tan, Yoshitaka Tatsumoto, Ines Thurner, Hiroshi Tomita, Takahiro Tsuchiya, Ken Tsugane, Dan Wilcox, Hubert Winzig

Metrology—Carlos Beitia, Mark Berry, Ben Bunday, Alain Diebold, Christina Hacker, Karey Holland, Masahiko Ikeno, Eiichi Kawamura, Adrain Kiermasz, Delphine LeCunff, Scott List, Philippe Maillot, Yaw Obeng, David Seiler, Vic Vartanian, Yuichiro Yamazaki

Modeling and Simulation—Nobutoshi Aoki, Jean-Charles Barbe, Francis Benistant, Augusto Benvenuti, Jaehoon Choi, Mauro Ciappa, Derren Dunn, Andreas Erdmann, Roman Gafiteanu, Wladek Grabinski, Tibor Grasser, An De Keersgieter, Yongwoo Kwon, Wolfgang Demmerle, Ronald Gull, Bert Huizing, Herve Jaouen, Dick Klaassen, Gerhard Klimeck, BongHoon Lee, Wilfried Lerch, Jürgen Lorenz, Rainer Minixhofer, Wolfgang Molzer, Victor Moroz, Chandra Mouli, Aneesh Nainani, Yon-Sup Pang, Hwasik Park, Jin-Kyu Park, Paul Pfäffli, Peter Pichler, Shigeo Satoh, Yi-Ming Sheu, Vivek Singh, I.C. Yang.

REGIONAL SUPPORT TEAMS

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- Europe—Nancy Schepers, Carine Cosemans-Slegers, Anja Jansen-Beysen
- Japan—Mina Sekiguchi
- Korea—BaeKeun Jun, Jae-Min Jun, In-Hee Jung, J.W. Ko
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- USA— Agnes Cobar; Devi Keller, Barbara Pebworth, Yumiko Takamori, Linda Wilson

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INTRODUCTION

OVERVIEW

For five decades, the semiconductor industry has distinguished itself by the rapid pace of improvement in its products. The principal categories of improvement trends are shown in Table 1 with examples of each. Most of these trends have resulted principally from the industry's ability to exponentially decrease the minimum feature sizes used to fabricate integrated circuits. Of course, the most frequently cited trend is in integration level, which is usually expressed as Moore's Law (that is, the number of components per chip doubles roughly every 24 months). The most significant trend is the decreasing cost-per-function, which has led to significant improvements in economic productivity and overall quality of life through proliferation of computers, communication, and other industrial and consumer electronics.

Table 1 Improvement Trends for ICs Enabled by Feature Scaling

TREND	*EXAMPLE*
Integration Level	**Components/chip, Moore's Law**
Cost	**Cost per function**
Speed	**Microprocessor throughput**
Power	**Laptop or cell phone battery life**
Compactness	**Small and light-weight products**
Functionality	**Nonvolatile memory, imager**

All of these improvement trends, sometimes called "scaling" trends, have been enabled by large R&D investments. In the last three decades, the growing size of the required investments has motivated industry collaboration and spawned many R&D partnerships, consortia, and other cooperative ventures. To help guide these R&D programs, the Semiconductor Industry Association (SIA) initiated The National Technology Roadmap for Semiconductors (NTRS), which had 1992, 1994, and 1997 editions. In 1998, the SIA was joined by corresponding industry associations in Europe, Japan, Korea, and Taiwan to participate in a 1998 update of the Roadmap and to begin work toward the first International Technology Roadmap for Semiconductors (ITRS), published in 1999. Since then, the ITRS has been updated in even-numbered years and fully revised in odd-numbered years. The overall objective of the ITRS is to present industry-wide consensus on the "best current estimate" of the industry's research and development needs out to a 15-year horizon. As such, it provides a guide to the efforts of companies, universities, governments, and other research providers or funders. The ITRS has improved the quality of R&D investment decisions made at all levels and has helped channel research efforts to areas that most need research breakthroughs.

The ITRS represents a dynamic process, as evidenced by the evolution of the ITRS documents. For example, the ITRS now reflects both geometrical scaling and "equivalent scaling." Geometrical scaling [enabling Moore's Law] has guided R&D targets for many years and will continue in many aspects of chip manufacture. Equivalent scaling targets, such as improving performance through innovative design, software solutions, and new materials/structures, increasingly guide the semiconductor industry in the current era. Since 2001, the ITRS has responded by introducing new chapters on System Drivers (2001), Emerging Research Devices and Radio Frequency and Analog/Mixed-signal Technologies for Wireless Communications (2005) [which now includes Analog technology emphasis and enhancements], Emerging Research Materials, to better reflect this evolution of the semiconductor industry (2007), and, in 2011, a Microelectromechanical Systems (MEMS) chapter [also aligned with the international Electronics Manufacturing Initiative (iNEMI) Roadmap]. Similarly, this 2012 ITRS Update contains seven special "timing-update" topics, ranging from the overall definition of "production timing" to the estimated schedule for 450mm manufacturing.

Since its inception in 1992, a basic premise of the Roadmap has been that continued scaling of electronics would further reduce the cost per function (historically ~25–29% per year) and promote market growth for integrated circuits (historically averaging ~17% per year, but maturing to slower growth in more recent history). Thus, the Roadmap has been put together in the spirit of a challenge—essentially, "What technical capabilities need to be developed for the industry to stay on Moore's Law and the other trends?"

Since 2007, the ITRS has addressed the concept of *functional diversification* under the title "More than Moore" (MtM). This concept addresses an emerging category of devices that incorporate functionalities that do not necessarily scale according to "Moore's Law," but provide additional value to the end customer in different ways. The MtM approach typically allows for the non-digital functionalities (e.g., RF communication, power control, passive components, sensors, actuators) to migrate from the system board-level into a particular package-level (SiP) or chip-level (SoC) system solution. The new Microelectromechanical Systems (MEMS) chapter also supports the ITRS MtM analysis with guidance for sensor and actuator technologies. It is also hoped that, by the end of this decade (2020), it will be possible to augment the capabilities of CMOS by introducing new devices that will realize some "beyond CMOS" capabilities. However, since these new devices may not totally replace CMOS functionality, it is anticipated that either chip-level or package-level integration with CMOS may be implemented.

FROM THE LESSONS LEARNED IN THE PAST DECADE TO BEYOND 2020

One of the fundamental lessons derived for the past successes of the semiconductor industry comes for the observation that most of the innovations of the past ten years—those that indeed that have revolutionized the way CMOS transistors are manufactured nowadays—were initiated 10–15 years before they were incorporated into the CMOS process. Strained silicon research began in the early 90s, high-κ/metal-gate initiated in the mid-90s and multiple-gate transistors were pioneered in the late 90s. This fundamental observation generates a simple but fundamental question: "*What should the ITRS do to identify now what the extended semiconductor industry will need 10–15 years from now?*"

As we look at the years 2020–2025 we can see that many physical dimensions are expected to be crossing the 10 nm threshold. It is expected that as dimensions approach the 5–7 nm range it will be difficult to operate any transistor structure that is utilizing the MOS physics as the basic principle of operation. Of course, we expect that new devices, like the very promising tunnel transistors, will allow a smooth transition from traditional CMOS to this new class of devices to reach these new levels of miniaturization. However, it is becoming clear that fundamental geometrical limits will be reached in the above timeframe. By fully utilizing the vertical dimension, it will be possible to stack layers of transistors on top of each other and this 3D approach will continue to increase the number of components per mm^2 even when horizontal physical dimensions will no longer be amenable to any further reduction. It seems then important that we ask ourselves a fundamental question: "*How will we be able to increase the computation and memory capacity when the device physical limits will be reached?*"

It appears that it becomes necessary to reexamine how we can get more information in a finite amount of space. The semiconductor industry has thrived on Boolean logic; after all, for most applications, the CMOS devices have been used as nothing more than an "on-off" switch. It becomes then of paramount importance to develop new techniques that allow the use of multiple (i.e., more than 2) logic states in any given and finite location. This immediately evokes the magic of "quantum computing" looming in the distance. However, short of reaching this ultimate goal, it may be possible to increase the number of states to a moderate level, let's say 4–10 states as an example, and, perhaps, increase the number of "virtual transistors" by 2 every 2 years ("Multiple States Law").

This is a field already explored by several investigators, and the ITRS should begin to pay attention.

On the other hand, during the blazing progress propelled by Moore's Law of semiconductor logic and memory products, many other technologies have progressed as well, even though at a slower pace. Nevertheless, as outlined in the More than Moore section, many new capabilities are now available because of these "complementary" technologies becoming available. A variety of wireless devices contain typical examples of this confluence of technologies (e.g., logic and memory devices, display, MEMS, RF, etc.). It appears that heterogeneous integration of multiple technologies has generated completely new applications in multiple applications beyond the traditional semiconductor logic and memory products that had lead the semiconductor industry from the mid 60s to the 90s. As noted above, the ITRS has incorporated More than Moore and RF/AMS chapters in the main body of the ITRS, but *is this sufficient to encompass the multiple facets of the new drivers of the semiconductor industry and the plethora of associated technologies now entangled into modern products*? After all, consumers have now become the real drivers of a proliferation of products that are now "pliable" in the sense of being individually molded into unique identities for consumers demanding "Custom Functionality."

In summary, heterogeneous integration, including wireless remote communications and unique combinations individual applications, has established the field of "custom functionality." The ITRS should consider how to address this fundamental change in the industry drivers.

The participation and continued consensus of semiconductor experts from Europe, Japan, Korea, Taiwan, and the U.S.A. ensure that the 2012 ITRS Update remains the definitive source of guidance for semiconductor research as we strive to

extend the historical advancement of semiconductor technology and the integrated circuit market. The complete ITRS 2012 Update and past editions of the ITRS are available for viewing and printing as electronic documents at *http://www.itrs.net*.

OVERALL ROADMAP PROCESS AND STRUCTURE

ROADMAPPING PROCESS

As indicated in the overview, the Roadmap has been created in the spirit of defining what technical capabilities the industry needs to develop in order to stay on Moore's Law and the other trends, and when. So the ITRS is not so much a high level forecasting exercise as a way to indicate where research should focus to continue Moore's law. In that initial "challenge" spirit, the Overall Roadmap Technology Characteristics (ORTC) team updates key high level technology needs, which establish some common reference points to maintain consistency among the chapters. The high level targets expressed in the ORTC tables are based in part on the compelling economic strategy of maintaining the historical high rate of advancement in integrated circuit technologies.

Over the years, however, the Roadmap has sometimes been seen as a self-fulfilling prophecy. To a certain extent this is also a valid view, as companies have benchmarked each other against the Roadmap, and it proved very effective in providing thrust for research. So it is not unreasonable to use the Roadmap targets, when manufacturing solutions or acceptable workarounds are known, as guidelines to forecasting exercises.

What these targets should never be used for, however, is as basis for legal claims in commercial disputes or other circumstances. In particular, the participation in the ITRS roadmapping process does not imply in any way a commitment by any of the participating companies to comply with the Roadmap targets. We recall that the ITRS is devised and intended for technology assessment only and is without regard to any commercial considerations pertaining to individual product or equipment.

THE MEANING OF ITRS TIME OF INTRODUCTION

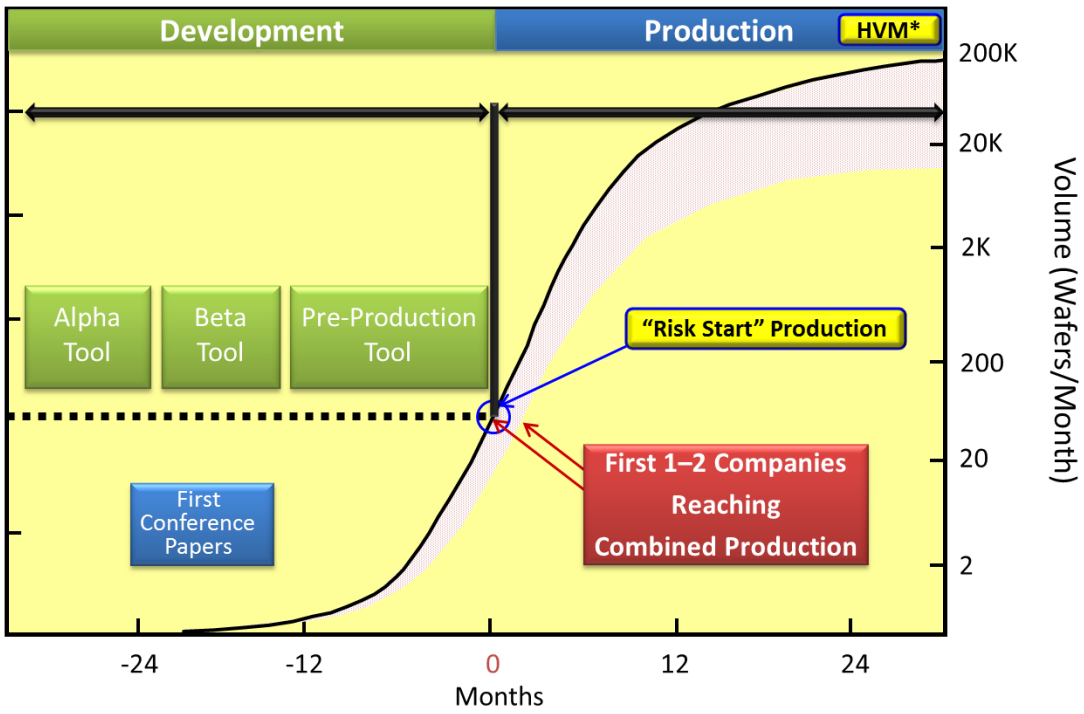
The ORTC and technology requirements tables are intended to indicate current best estimates of introduction time points for specific technology requirements. Ideally, the Roadmap might show multiple time points along the "research-development-prototyping-manufacturing" cycle for each requirement. However, in the interests of simplicity, usually only one point in time is estimated. The default "Time of Introduction" in the ITRS is the "Year of Production." which is defined in Figure 1a.

Figure 1a was first revised in the 2011 ITRS to no longer include reference to volume parts per month, due to the variability of different product die sizes for first production targets. Therefore, only the typical industry high volume ramp scale is retained in the 2011 and 2012 roadmaps. After additional work on the 2012 Update, it was decided by the IRC that the timing of production could refer to one leading IDM or foundry company (representing many fabless companies) that would also represent a significant volume ramp of capacity and additional companies would follow that lead. A note was added to the ITRS timing graphic to describe this new change in definition of ITRS Production.

A graphical note was included, at the request of the Emerging Research Devices (ERD) and Emerging Research Materials (ERM) TWGs as seen in Figure 1b. The note is a reminder of the very wide time range required to capture early research activities that may result in potential solutions items for the ITWG Difficult Challenges. It has become increasingly important to communicate a broad horizon encompassing both the period preceding the first manufacturing alpha tools and materials and also the period that extends to the classic ITRS 15-year horizon and even beyond.

The preceding horizon is required to capture the period of the very first technical conference paper proposals until the start of development activities; at which point typically a transfer from ERD/ERM to PIDS/FEP ITWGs occurs. The early research horizon also reminds the readers and the ITRS participants of the influence of the National Technology Roadmap for Semiconductors (NTRS: 1991–1998) and the International Technology Roadmap for Semiconductors (ITRS: 1998 to present), as the work of the roadmaps tracked and influenced the manufacturing technology needs and priorities of industry R&D long before they turn into production. Many academic and industry studies have examined and commented on the uniqueness and the impact of pre-competitive cooperation provided by the International Technology Roadmap for Semiconductors.

For more explicit clarification, see Figure 1b, in which an example is shown for a new gate structure potential solution (III/V hi mobility gate) targeted for 2019 production. In this example, the first research papers appear in 2007, and the potential solution technology was transferred to PIDS during the 2011 ITRS roadmap work, when more detailed line item characteristics were defined by the PIDS ITWG in their 2011 work, and also included in the PIDS 2012 Update work.



Fewer leading IDM companies requires adaption of definition to allow one IDM company or a foundry representing many fabless companies to lead a technology production ramp timing

Figure 1a A Typical Technology Production "Ramp" Curve (within an established wafer generation)[1]

The "production" time in the ITRS refers to the time when the first leading company brings a technology to production. Typically, a second company follows within a short period of time, and ideally as soon as three months; however sometimes there is a longer time for the second company to get into production, especially when considering alternative "equivalent scaling" technology pathway options (see Equivalent Scaling topic). Additional complexity of timing occurs when rapid accelerations occur and a leading company will go into production ahead of the ITRS Roadmap timing targets. This happened in the case of MugFET production announcements in 2011 (from 2015), and there is the possibility of III/V Ge technology acceleration to 2015 (from 2019). It remains to be seen how rapidly "fast following" companies provide their own announcements in response to production accelerations, and updates on this topic have been discussed by the IRC and is included in the 2012 Update. (Refer to the Equivalent Scaling topic.)

For further clarification, "production" means the completion of both process and product qualification. The product qualification means the approval by customers to ship products, which may take one to twelve months to complete after product qualification samples are received by the customer. Preceding the production, process qualifications and tool development need to be completed. Production tools are developed typically 12 to 24 months prior to production. This means that alpha and succeeding beta tools are developed preceding the production tool.

Also note that the Production "time zero" in Figures 1a and 1b can be viewed as the time of the beginning of the ramp to full production wafer starts. For a fab designed for 20K wafer-starts-per-month (WSPM) capacity or more, the time to ramp from 20 WSPM (also called "risk starts" in industry jargon) to full capacity can take nine to twelve months. As an example, this time would correspond to the same time for ramping device unit volume capacity from 6K units (samples/"risk starts") to 6M units per month [for the example of a chip size at 140 mm^2 (430 gross die per 300 mm wafer × 20K WSPM × 70% total yield from wafer starts to finished product = 6M units/month)].

In addition, note that the ITRS ramp timing in this example is in reference to the ramp of a technology cycle within a given wafer generation. Now that the industry is approaching the time for a new 450 mm wafer generation transition, additional scrutiny has been given to the historical ramp rate for a technology cycle that has been ramped in two wafer generations of the first leading companies at the same time. It is during that transition of a technology cycle coexisting

[1] *See Figure 1b below for ERD/ERM Research and PIDS Transfer timing*

within two wafer generations that the economic productivity gain modeling is also examined. (Refer to the 450 mm topic.)

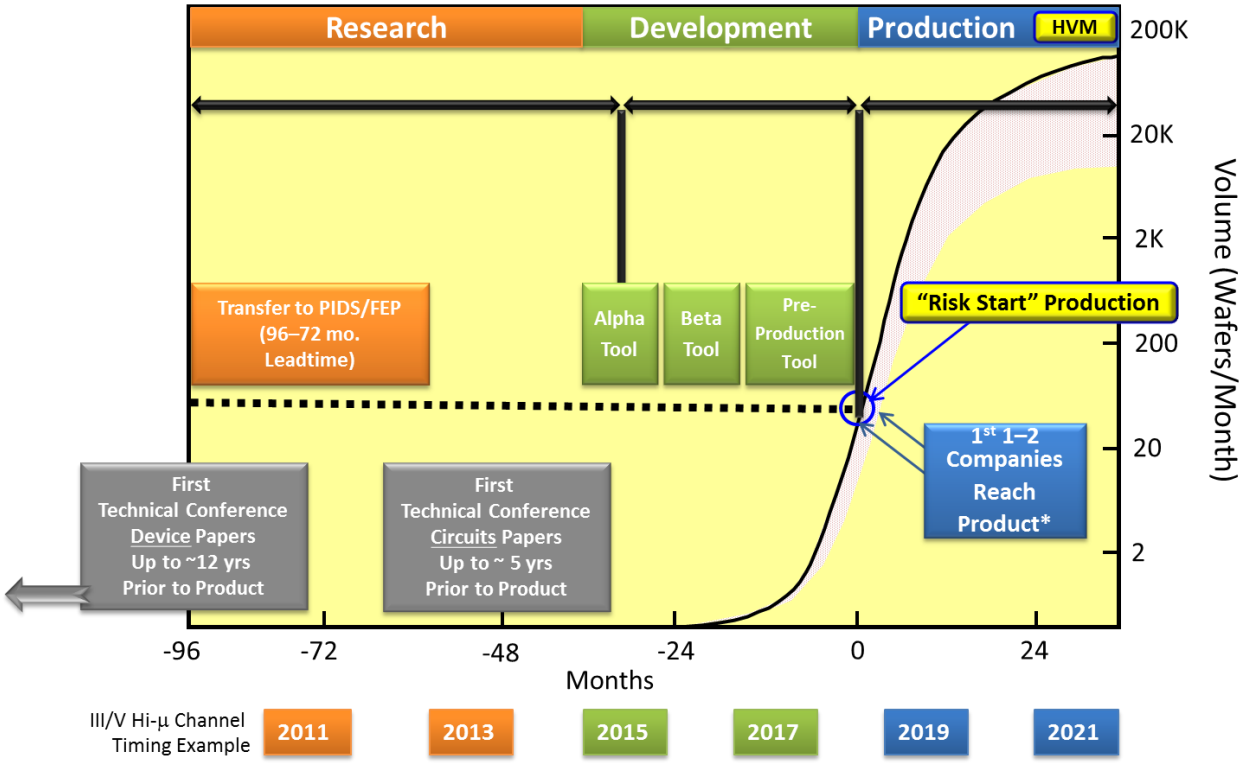


Figure 1b A Typical Technology Production "Ramp" Curve for ERD/ERM Research and PIDS Transfer Timing (including the example of III/V Hi-Mobility Gate Technology Timing Scenario)[2]

[2] *See also "Equivalent Scaling" topic*

MORE THAN MOORE (MTM) UPDATE

As a reminder, the "More than Moore" industry trend encompasses functionalities that do not necessarily scale according to "Moore's Law," but provide additional value to the end customer in different ways. It does not compete with miniaturization, but instead complements it, thus allowing the development of value-added systems, as depicted in the Figure 2 below.

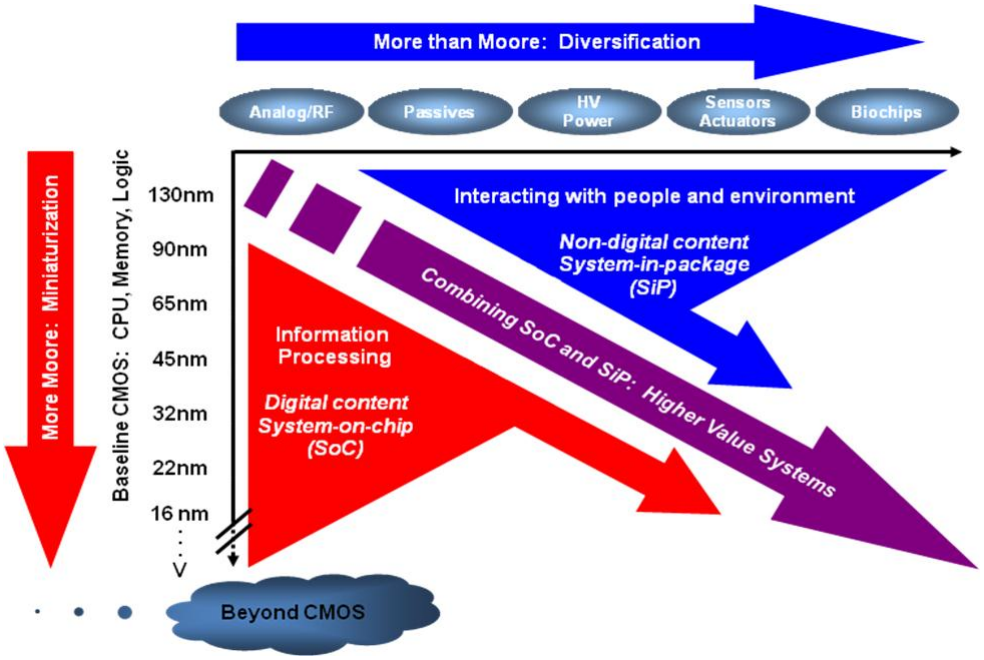


Figure 2 Moore's Law and More

The importance of this industry trend was recognized in the ITRS 2005 edition, and the potential benefits of developing roadmap(s) for "More than Moore" technologies is now well established. It is, however, not an easy task, given the variety of technologies and physical phenomena involved. As mentioned in the *white paper*, (elaborated in 2010 to propose a methodology to identify those MtM technologies for which a roadmapping effort is feasible and desirable), the ITRS community needs to depart from the traditional "technology push" approach that it has followed for roadmapping the continuation of Moore's law (i.e., linear scaling), and involve new constituencies in its activities.

This new approach already materialized in 2011, when the 2011 ITRS added a MEMS chapter to the roadmap, and also aligned it with previous work included in the 2011 international Electronics Manufacturing Initiative (iNEMI) roadmap. In 2012, this link with iNEMI was further reinforced: after a cross-TWG study group had identified health care, automotive, energy and lighting as lead markets which could drive roadmaps for More that Moore technologies, iNEMI representatives participated to the ITRS Spring and Summer meetings, in order to share with the ITRS community their views on the evolution of those markets.

The cross-TWG study group on More than Moore further refined its approach to identify technologies worth being roadmapped, resulting in the process described in the Figure 3 below.

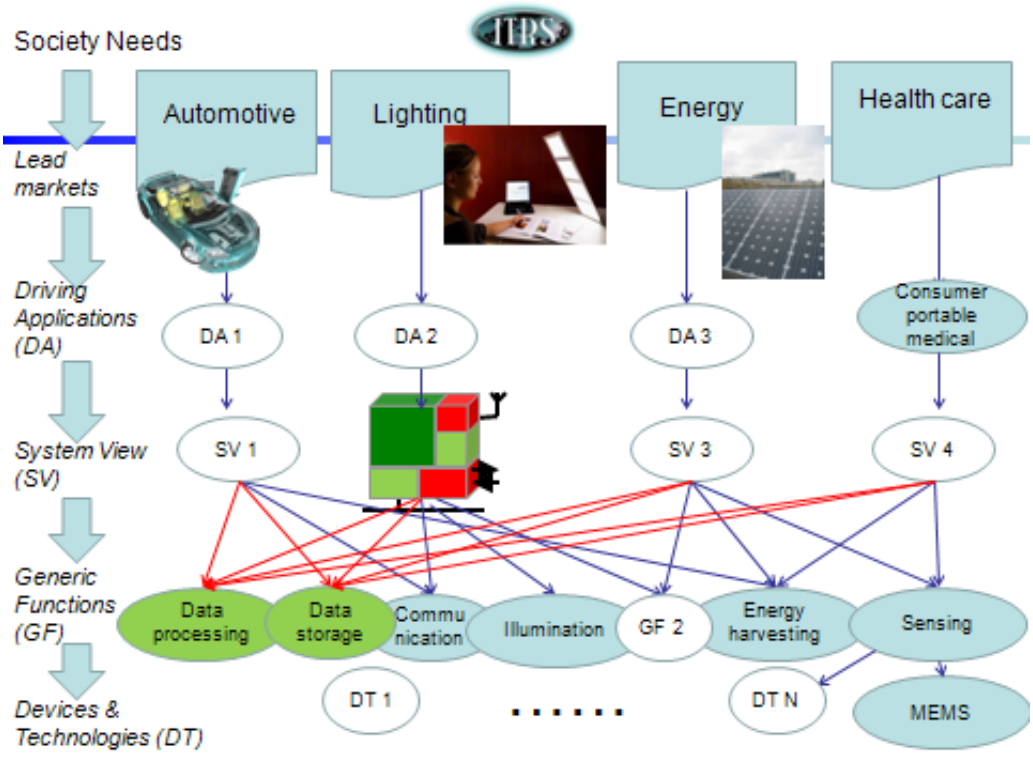


Figure 3 Proposed Roadmapping Process for More than Moore Technologies

For each of the markets mentioned earlier (health care, automotive, energy, and lighting), it is proposed to identify a driving application, broad enough to require many of the technologies that the market will likely need. For example, a consumer portable medical device will encompass many functionalities such as sensing, communicating, energy management, signal processing, data storage, and so on. Building the system views of these driving applications will allow listing the functions that they rely upon. Some of those functions will be present across many applications and can therefore be dubbed "generic." The devices and technologies performing these generic functions will presumably be the ones for which a roadmapping effort is most useful, if feasible). The driving applications will dictate the performance roadmaps of these generic functions, which in turn can be met by various technologies and devices.[3] To clarify further this distinction between functions on the one hand, and technologies and devices on the other hand, one can note that functions answer a "what" question ("*what needs to be performed?*"), while technologies and devices answer a "how" question ("*how is it performed?*").

A good illustration of this approach is given by the MEMS ITWG, which already, in its 2011 chapter, chose to align its effort towards MEMS technologies associated with "mobile internet devices," a driving application broad enough to incorporate many existing and emerging MEMS technologies.

The respective roles of the ITRS community and of the other bodies active in roadmapping efforts in various application domains, such as iNEMI or European Center for Power Electronics (ECPE), become clear when looking at this picture: ITRS expertise deals with generic functions and their embodiments in technologies and devices while the expertise of application-oriented roadmapping organizations covers systems and functions. The two communities meet and can exchange in a fruitful manner at the level of the functions. The ITRS can propose candidate generic functions, based on its a *priori* knowledge of future technological evolutions and the other roadmapping organizations can express their needs and give feedback on the ITRS proposals. It is expected that, through this process of mutual adjustment, the ITRS will achieve a good understanding of which generic functions are most likely to emerge, and of the expected evolution of their performances over time, leading to roadmaps of key underlying technologies.

[3] *Note that this process also covers the functions traditionally performed by More Moore technologies: data storage and processing. But for those, a market-pull approach is not required.*

2012 ITRS SPECIAL TOPICS

TRANSITION TO 450 MM—A STATUS UPDATE FOR THE 2012 ITRS

The rationale for a transition to 450 mm diameter wafer is productivity—one of the enablers of Moore's law. This is the ability to decrease the manufacturing cost of each mm^2 of IC by the use of larger diameter wafers. Based on economic considerations, during the 2007 ITRS roadmap development, the International SEMATECH Manufacturing Initiative (ISMI) had determined that to stay on this productivity curve, the industry needed to achieve 30% cost reduction and 50% cycle time improvement in manufacturing, which in their opinion would be achievable only by a transition to 450 mm (while the cost reduction goal has been achieved through previous wafer generation changes, the cycle time goal is new). The need for 450 mm wafer generation transition productivity was reinforced in 2007 by the conclusions of an analysis of potential 300 mm improvements, which showed that the so-called "300 mm Prime" program had cycle time opportunity but fell short of the traditional cost reduction required to stay on Moore's Law. This realization prompted ISMI to kick-off the 450 mm initiative in July 2007.

Subsequently, Intel, Samsung, and TSMC (International SEMATECH) announced in May 2008 that they would work together with suppliers, other semiconductor players, and ISMI to develop 450 mm with the original goal set in 2008 for a consortium pilot line in 2012, which would support integrated device manufacturers (IDM) and foundry pilot line development in the 2013–14 timeframe, followed by first production ramps in the 2015–16 timeframe.[4] The 2008 public announcement and assessment was the statement of record by these three companies and ISMI and used in the writing of the ITRS 2009 and 2010 editions. Additionally, it was subject to revision based on future statements and required updating to the latest status and approach of the consortium. See Figure 4.

Taking lessons from the past, it can be observed that each wafer size transition has been different from any of the previous ones. The conversion to 300 mm wafer can be characterized by fact that for the first time the consortia (I300I and Selete) led the whole industry effort. The well-tested consortium effort is now also the chosen approach for enabling the 450 mm wafer size conversion. SEMI participation was also essential in the 300 mm wafer size conversion since for the first time "provisional standards" were agreed upon by the whole industry before the final manufacturing equipment was fully developed. In particular, the industry solved a fundamental problem by agreeing on adopting full wafer transport automation. All the suppliers abandoned their proprietary solutions to wafer transport, port design, and load size in favor of the agreed front opening unified pod (FOUP)/ overhead solution.

In this respect, the 450 mm wafer size transition is taking full advantage of the work previously done to standardize the 300 mm wafer transport by having already adopted the same whole automation scheme with only minor upgrades, thus placing the 450 mm silicon standards and automation schedule ahead of the corresponding 300 mm wafer size conversion schedule with respect both to automation and also to silicon material standards. During the interim consortium work since the 2009 ITRS publication, consortium progress has resulted in the completion of international standards for 450 mm carriers, loadports, and developmental test wafers. These advances were enabled by extensive prototyping and interoperability/cycle testing in cooperative development between component suppliers, SEMI, and ISMI.

During 2011, significant development progress was achieved by consortia and is ongoing, as is dialogue between semiconductor manufacturers and suppliers to assess standards and productivity improvement options on 300 mm and 450 mm generations. Economic analysis of option scenarios was also advanced in order to examine the required R&D cost, benefits, and return-on-investment, along with funding mechanism analysis and proposals from companies, and different regional consortia and governments.

In 2011 witnessed the move of the SEMATECH 450 mm program moved from Austin, Texas, to Albany, New York, where a new consortium clean room has been completed on schedule for the planned 2012 consortium demonstration line for continued alpha and beta tool development and preparation for IDM and foundry pilot line demonstrations. In addition, the European EEMI 450 mm consortium initiative continued to make progress and report to the IRC of their plans for targets for 450 mm development in new facilities in IMEC in Belgium.

Also, the previously-announced private consortium initiative, the Global 450 mm Consortium (G450C), among five major industry players—Intel, Samsung, TSMC, GLOBALFOUNDRIES, and IBM—in cooperation with the state of New York, has begun to invest $4.4B to advance 450 mm manufacturing and technology development. Although much work remains over the next several years, these announced large investment commitments, and with potentially more

[4] *Source: "May 2008"/"Oct 2008 ISMI symposium"/Dec'08 ISMI 450 mm Transition Program Status Update for ITRS IRC, Seoul, Korea*

coming from the EEMI 450 mm consortium, will go far to support the globally-coordinated effort needed to ensure a cost-effective and timely transition to the next wafer size.

Given all of the above, (and with possible advancements based on the ongoing work of continuous improvements and technology upgrades of 300 mm equipment which might eventually also be applicable to 450 mm processing), and based on status updates from G450C and also the latest public industry announcements mentioned below, the ITRS IRC now expects that consortium development and demonstration work will continue, supporting the development of material and manufacturing tools to be available between 2013 to 2014 for IDM and foundry pilot lines. If the announced targets by IDM and foundry pilot lines remain on track for 2015–16, then the ITRS target for 450 mm early "risk starts" in 2016, and production manufacturing ramps from 2017–2018 should also be possible, subject to the production readiness of tools and 450 mm wafer high volume availability. The IRC continues to recommend that wafer diameter should not be tied to technology generations. Leading edge technologies will run both in 300 and 450 mm technologies in parallel, as happened with the 300 mm wafer generation ramp on two succeeding technology cycles in the 2001–2003 (180 nm–130 nm M1 half-pitch) timeframe.

To support the latest industry status in the 2012 ITRS Executive Overview, an updated version of the 450 mm Production Ramp-up Model Graphic has been proposed for the 2013 ITRS. See Figure 5. This illustrates the special dual "S-curve" timing required when a new wafer generation is being introduced [again modeled after the experience with the 300 mm wafer generation ramp on two succeeding technology cycles in the 2001–2003 (180 nm–130 nm M1 half-pitch) timeframe].

Note that the proposal for the 2013 ITRS revision wafer generation timing targets for the 450 mm generation IDM and foundry pilot lines are now delayed about 2 years (2015–16, versus the previous 2013–14 target indicated in the 2009 through 2011 ITRS).

In the 2009-11 ITRS editions, the IRC had originally placed the timeframe for 450 mm volume production ramp for early product sampling (also known by industry jargon as "risk starts" pre-production) in the 2015–2016 time frame. The 450 mm "risk starts" range is now targeted for 2016 and the latest ramp range is now labeled "High Volume Manufacturing" (HVM). High volume manufacturing is now targeted for 2017-18 in this proposal for the 2013 ITRS Renewal work and labeled as such in the timing graphic.

Although the timing targets for 450 mm, IDM and foundry pilot line and production ramp timing are now revised (2017–2018 production) in the 2013 ITRS proposal, clarifications added to the consortium (G450C) work timing targets remain unchanged, which now includes a full pilot-line-ready beta tool set of 450 mm equipment development and demonstration, but does not include a full-flow pilot line at the consortium.

Due to updates to the ITRS IRC from the new G450C consortium, it is now believed by the consortium IDM and foundry members that only demonstration support is required from the consortium and that final full-flow beta and production development should occur in IDM and foundry company pilot lines in the 2015–16 timeframe. Announced plans continue to support the original targets for "risk starts" 450 mm production ramp in the 2016 timeframe for 1× node technology manufacturing (14–15 nm Flash Poly half-pitch and 19–20 nm M1 ("10 nm node") half-pitch DRAM and MPU/ASIC 2011 ITRS technology targets).

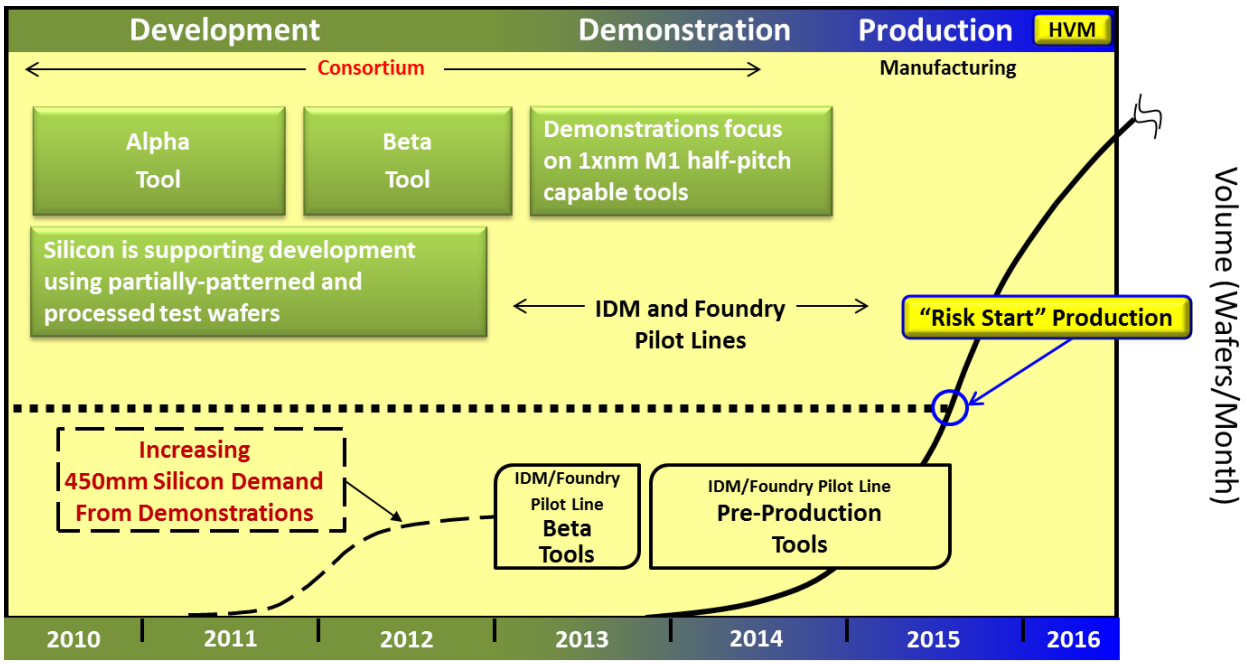


Figure 4 A Typical Wafer Generation Pilot Line and Production "Ramp" Curve applied to Forecast Timing Targets of the 450 mm Wafer Generation

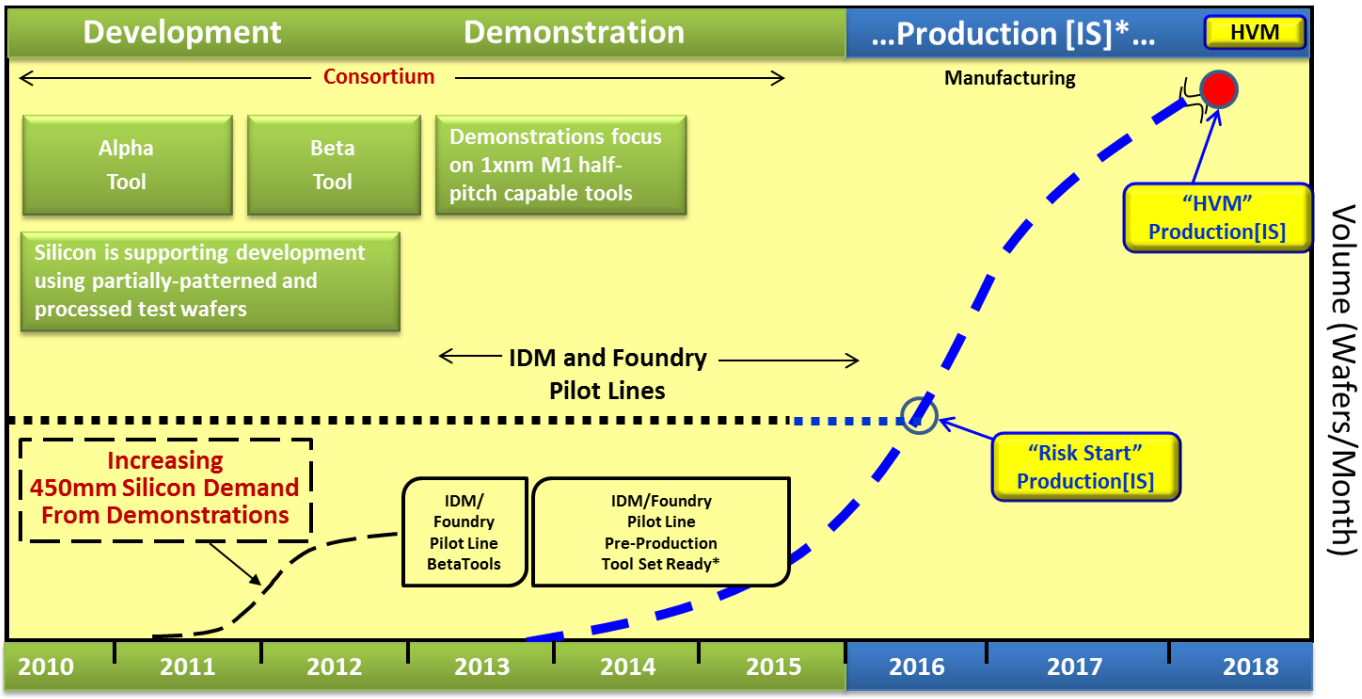


Figure 5 2013 Proposal: A Typical Wafer Generation Pilot Line and Production "Ramp" Curve applied to Forecast Timing Targets of the 450 mm Wafer Generation

For completeness of the 2011 and 2012 Update ITRS 450 mm status, and as a service to the readers, it should also be noted that significant progress on economic modeling scenarios was also achieved by SEMATECH/ISMI, including updating and enhancing the ISMI Industry Economic Model (IEM); and also including contracting with a well-known industry consultant, IC Knowledge (ICK)[5] to develop a strategic-range model of equipment demand. That original ISMI and ICK model work was based on the ITRS 2009 ITRS and 2010 Update, and is now available as a commercial subscription (*www.icknowledge.com*), updated to the latest published 2011 ITRS (*www.itrs.net*).

BACKGROUND AND UPDATES TO THE 2012 ITRS OVERALL ROADMAP TECHNOLOGY CHARACTERISTICS (ORTC)

"Moore's Law," established five decades ago by Gordon Moore of Intel Corporation, is a concept that states that market pressures drive semiconductor chip functional density to double on a periodic basis; and the cycle of that period is set by the technological advancement of manufacturing process capability. In addition to the functional density, the "Moore's Law" concept also included the concept of affordability, observing that technology introduced too soon could increase the cost/function, causing the chip to be unaffordable to the market.

For many decades of technology advancement, the drive to meet the requirements of "Moore's Law" also had synergistic benefits due to the physics of semiconductor operation, which caused shrinking dimensions of the transistor gate thickness and channel length to reduce the voltage and power required for reliable operation of both switching and storage operations, while at the same time also increasing the speed of operation of the device.

This "triumvirate" of functionality, higher performance, and lower power market benefits to consumers continued into the early 2000's; when, passing through nano-scale dimensions, the shrinking of technology began to approach molecular and atomic levels (in the case of gate and channel thickness and length). The result was that voltage levels could no longer reduce due to causing breakdown and high current drain, both operating and standby.

As a result the usual dimensional reduction of the scaling of printed and physical gate length of transistors had to slow, compensated by a tradeoff with what became known as "Equivalent Scaling"—the inclusion of process techniques such as gate strain in the channel, HiK-metal gate materials in the transistor gate; and more recently, transistor 3D architecture called multiple gate FET (MugFET) or FinFET. On the near horizon, new channel materials, such as III/V Germanium, will also enter into manufacturing to benefit performance and power of devices.

Additional chip and system-level architectural and software design "Equivalent Scaling" such as SRAM memory architecture, CPU multiple-core, and power software management enabled the chips, limited by slower voltage decreases and slower speed of operation, to still achieve the needed market low power and high performance requirements of the latest centralized Communications and Cloud Computing high performance and also the Portability and Mobility low power of the latest and future market applications.

These system-level alternative power performance tradeoffs are also enabled by the "Moore's Law" functional density drivers, which are enabled by the dimensional size of the function itself. The size of the function is set fundamentally by the half-pitch of interconnect, in conjunction with the number and size of the vertical wiring levels, ultimately connecting to the finished device by assembly and packaging technology. Additional ITRS definition work on these important "Moore's Law" functional density technology enablers is described in Figure 6. The Interconnect TWG dimensional relationships are demonstrated graphically in Figure 7).

[5] *Special acknowledgment to Scott Jones with IC Knowledge for his contributions towards the 2011 ITRS effort.*

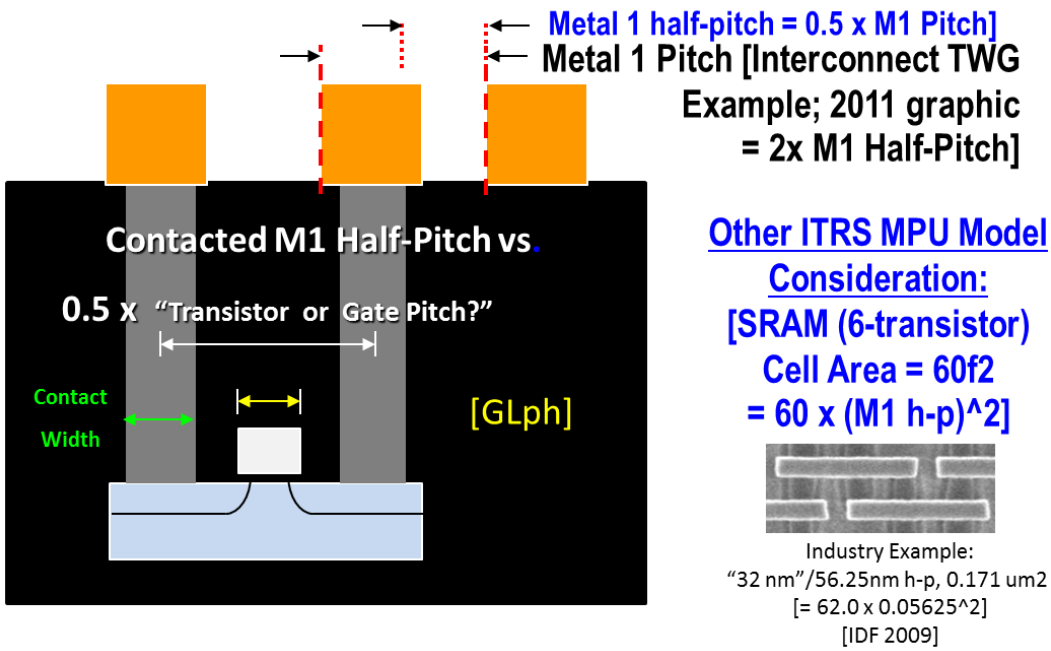
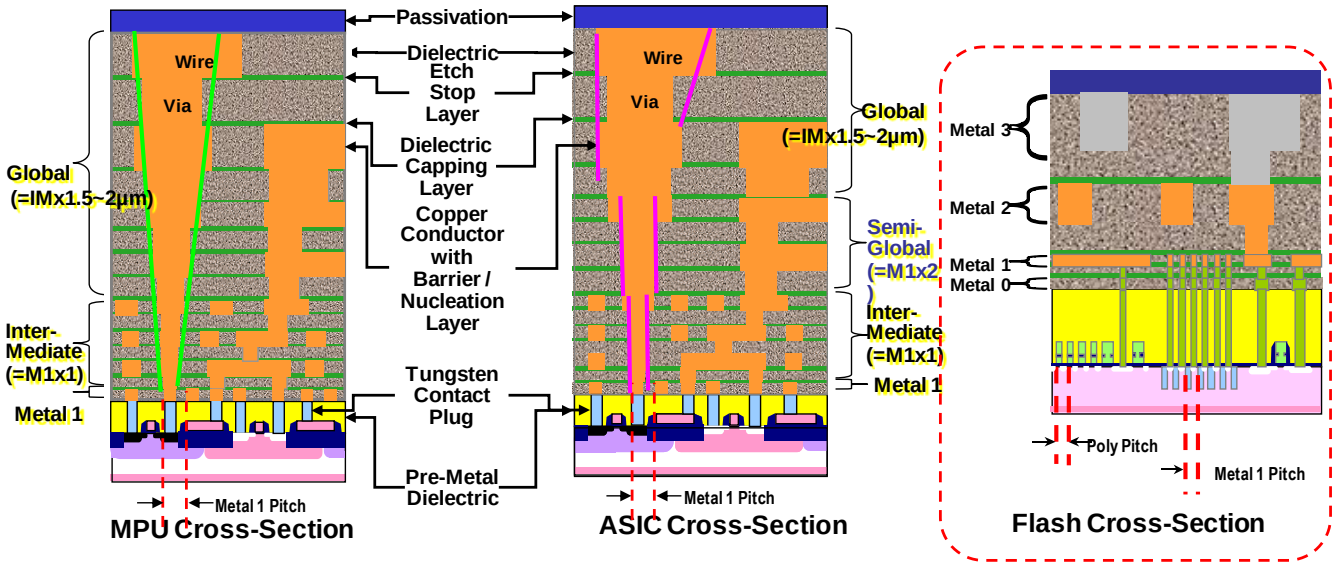


Figure 6 Transistor Dimension Definition 2012/2013 ITRS Work in Progress[6]

[6] *This graphic clarifies the ORTC Table 1 relationship to gate length. It illustrates consistency with Interconnect TWG transistor M1 contacted half-pitch (also known as "transistor pitch" or "gate pitch") versus printed gate length (GLpr) and measurable physical gate length (GLph). This dimension is sometimes compared to critical dimension (CD) for manufacturing process control.*
The ITRS does not utilize any single-product "node" designation reference. Flash Poly and DRAM M1 half-pitch are still lithography drivers; however, other product technology trends may be drivers on individual TWG tables.

2011 Interconnect TWG - Hierarchical Cross Sections



1) MPU: Revised hierarchy
2) ASIC: No drastic change, however semi-global should be kept at 2 x M1
3) Flash: The new technology driver for M1 also?

Figure 7 Interconnect Graphic

The ITRS has guided the research and development community by identifying grand challenges and potential solutions that were narrowed, from the previous typical 12–15 years academic research horizon required lead time, into the 4–8 year manufacturer and equipment and material supplier development period; then ultimately into the production-ready manufacturing solutions available to the market today and in the near future.

Examples of the narrowing of potential solutions from the Lithography ITWG are shown in Figures 8 and 9. Lithography is a critical enabling technology for the manufacturing process capability to create dimensions of both the interconnect and also the printed gate length features of transistors.

Figure LITH3A DRAM and MPU Potential Solutions

	First Year of IC Production	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026
	DRAM ½ pitch (nm) (contacted)	36	32	28	25	23	20.0	17.9	15.9	14.2	12.6	11.3	10.0	8.9	8.0	7.1	6.3
	MPU/ASIC Metal 1 1/2 pitch (nm)	38	32	27	24	21	18.9	16.9	15.0	13.4	11.9	10.6	9.5	8.4	7.5	7.5	7.5
45	193nm Imm																
32	193 nm DP																
22	EUV																
	193nm MP	Narrow Options															
	ML2 (MPU)																
16	EUV																
	193nm MP				Narrow Options												
	ML2																
	DSA + Litho																
	Imprint																
11	EUV higher NA / EUV + DP																
	ML2																
	DSA + Litho								Narrow Options								
	EUV (new wavelength)																
	Imprint																
	Innovation																

MPU / DRAM time line

Figure 8 Lithography TWG DRAM and MPU Potential Solutions

Figure LITH3B Flash Potential Solutions

	First Year of IC Production	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026
	Flash ½ Pitch (nm) (un-contacted Poly)(f)	22	20	18	17	15	14	13	12	11	10.0	8.9	8.0	8.0	8.0	8.0	8.0
32	193 nm DP																
22	193 nm DP																
16	193nm MP																
	EUV	Narrow Options															
	Imprint																
11	EUV higher NA / EUV + DP																
	193nm MP																
	DSA + Litho																
	EUV (new wavelength)					Narrow Options											
	Imprint																
	Innovation																

NAND Flash Time Line

Figure 9 Lithography TWG Flash Potential Solutions

Continuing Moore's Law functional density benefits and managing power and performance tradeoffs remain as the key drivers of the Roadmap grand challenges and potential solutions. Therefore, driving half-pitch reduction, combined with managing and gate-length and "Equivalent Scaling tradeoffs also remain as drivers.

The MPU/hpASIC M1 half-pitch continues to be defined as a stagger-contacted half-pitch the same as DRAM. The trend targets remain unchanged in the 2012 ITRS ORTC Update tables from the 2011 ITRS Roadmap. In the 2011 version, online at *www.itrs.net*, the PIDS ITWG corrected the DRAM trend to 2009/45 nm (a 1-year pull-in versus the ITRS targets from the 2009 and 2010 versions). The MPU/hpASIC M1 half-pitch has remained unchanged on the lagging two-

year cycle trend that crosses DRAM now in 2012/32 nm, and then continues to 2013/27 nm before it turns to a three-year cycle for the balance of the roadmap period, running parallel with DRAM M1 half-pitch targets (See Figures 10 and 11 below).

The Flash product half-pitch, unchanged for the 2012 ITRS ORTC Update, continues to be defined as an uncontacted polysilicon half-pitch; and was also revised in 2011 from the 2009 and 2010 ITRS additions by continuing the two-year cycle trend through 2009/39 nm, then matching the PIDS Flash survey 2010/24 nm before turning to the survey-forecasted 4-year cycle (0.5× per 8 years) through 2020/10 nm. At the 2020 point, the Flash trend is equal to the original 2009 and 2010 version target and Flash survey consensus forecasts the trends to return to a 3-year pace to 2022/8 nm; at which point, the trend remains flat to 2026/8nm due to anticipated Flash cell design limitations (see Figure 10).

The Flash 3D bit layer model, unchanged in 2012 (except for emphasis of the maximum range of layers) was a significant addition to the 2011 ORTC Flash Product technology trend tracking. Adding Flash 3D bit layers, beginning 2016, also includes the trade-off with reduced poly uncontacted half pitch trends, along with the anticipated chip sizes and bit densities that result from the PIDS TWG models of that "equivalent scaling" technology tradeoff. Lithography masks count impact of the Flash 3D bit layers technology is discussed in the 2011 Executive Summary "Lithography Masks Count special topic and also in more detail in the 2011 PIDS chapter.

ITRS "EQUIVALENT SCALING" GRAPHIC UPDATE TIMING AND PIDS PURDUE MODELING UPDATE

Due to trade-offs with "equivalent-scaling" process enhancements (copper and low-κ interconnect, strained silicon, high-κ/metal gate, MugFETs, FDSOI, III/V Ge, etc.), as performance and power management alternatives (see Figures 11 and 12), the *printed* MPU and *physical* gate length trends received major corrections in the 2008 and 2009 ITRS ORTC, which remained unchanged in the 2011 and 2012 ITRS versions. As described above, the physical gate length trend has been aligned with historical and survey data by the PIDS TWG and is on a slower 3.8-year cycle trend beginning 2009/32 nm through 2024/7.5 nm. The printed gate length begins a delayed three-year cycle trend in 2011, and continues through 2026 on a "shrinking" ratio relationship to the physical gate length out to 2024/7.9 nm, just slightly larger than the expected final physical gate length at that time. Refer to Figure 11.

As a result of announcements in 2011 of production of MugFET and FDSOI technology in 2012, PIDS ITWG revised their 2012 Update tables to match new timing of those "equivalent scaling" tradeoff options. PIDS also added a line for III/V Ge gate material (responsibility for developing tables for III/V Ge technology was passed to PIDS from ERD/ERM TWGs as mentioned above in the Roadmap Timing special topic). Due to possible acceleration of III/V Ge from 2019 to 2015, there will need to be work by the TWGs in the 2013 ITRS to deal with the impact of that 4–5-year accelerations of "equivalent scaling" technology (see 2011 ITRS Executive Summary topic on Technology Pacing/Timing and Frequency/Power at *www.itrs.net*).

During their 2012 Update work, and to enable the significant amount of modeling work and resources required to develop future ITRS guidance tables, the ITRS PIDS and Modeling TWGs received approval from the IRC to initiate a partnership with Purdue University. PIDS will assume primary responsibility for interfacing with Purdue to assure alignment of the past ITRS MASTAR static model approach with the new Purdue TCAD long-range dynamic modeling tools output. The ITRS Modeling TWG agreed to hold frequent reviews with the PIDS and Purdue team, and also the Modeling TWG will share Purdue students who will be working on both the Modeling TWG and PIDS TWG teams. Purdue University agreed to support the ITRS for at least a 10 year period to assure long-term continuity of the work, and would allow use of the Purdue online public modeling review resources for additional public discourse and input to the project.

One of the first tasks to be undertaken by the PIDS/Purdue team will be to develop as soon as possible the 2013 PIDS ITWG tables, which model both near term (tied to previous MASTAR modeling results) and long term (tied to Purdue/PIDS TCAD dynamic modeling) intrinsic transistor and ring oscillator characteristic trends. These new trends should support the adjustment of the current PIDS data table 13% intrinsic frequency growth trends down to an 8% trend. That slower trend would be more compatible with the present guidance from the Design ITWG (that only 4% growth of chip frequency is required both near and long term). The 8% PIDS model intrinsic frequency growth should allow adequate "headroom" for designers to plan complex SOC and MPU products over both the near and long term-ranges (see the 2011 ITRS Executive Summary Chip Frequency special topic, online at *www.itrs.net*).

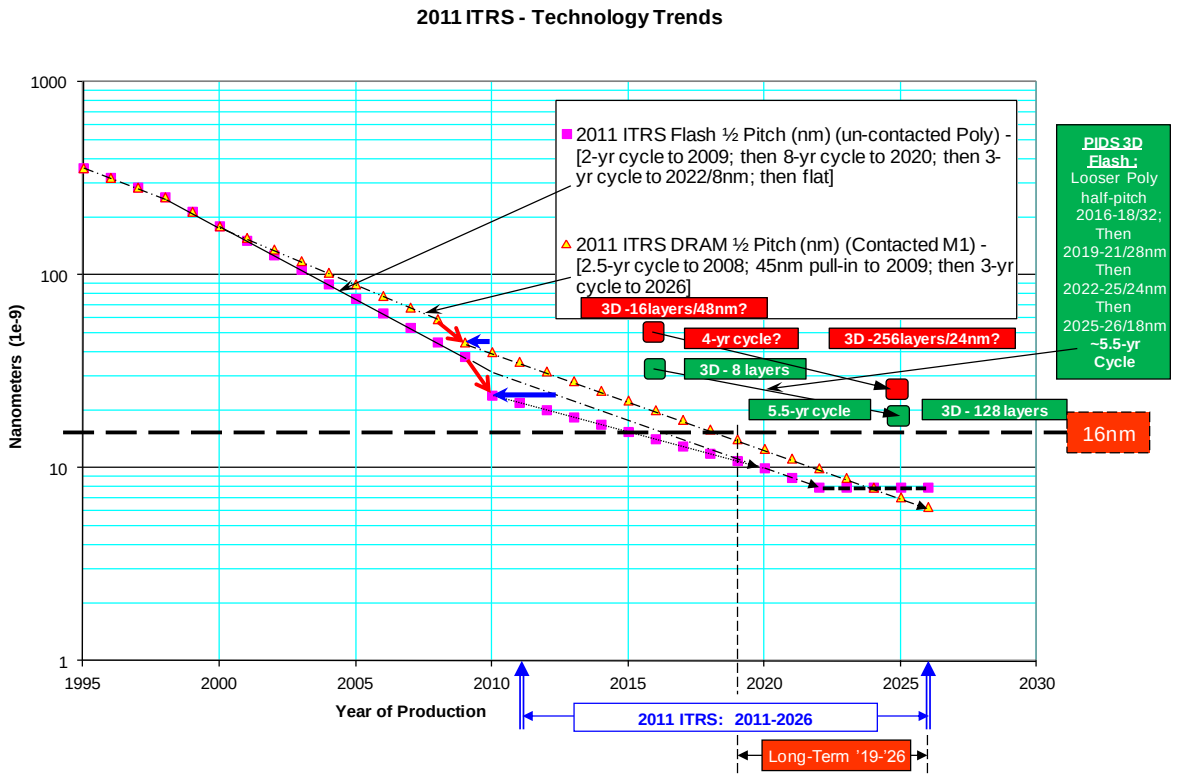


Figure 10 2011 ITRS—DRAM and Flash Memory Half Pitch Trends

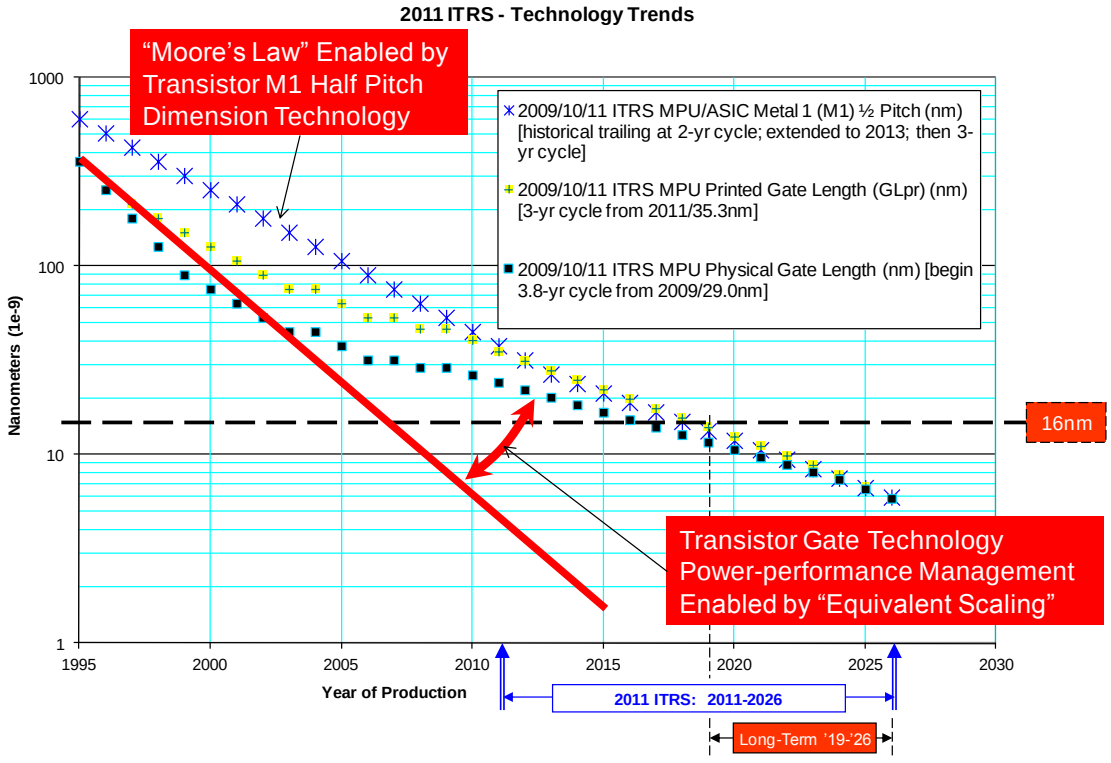


Figure 11 2011 ITRS—MPU/High-performance ASIC Half Pitch and Gate Length Trends

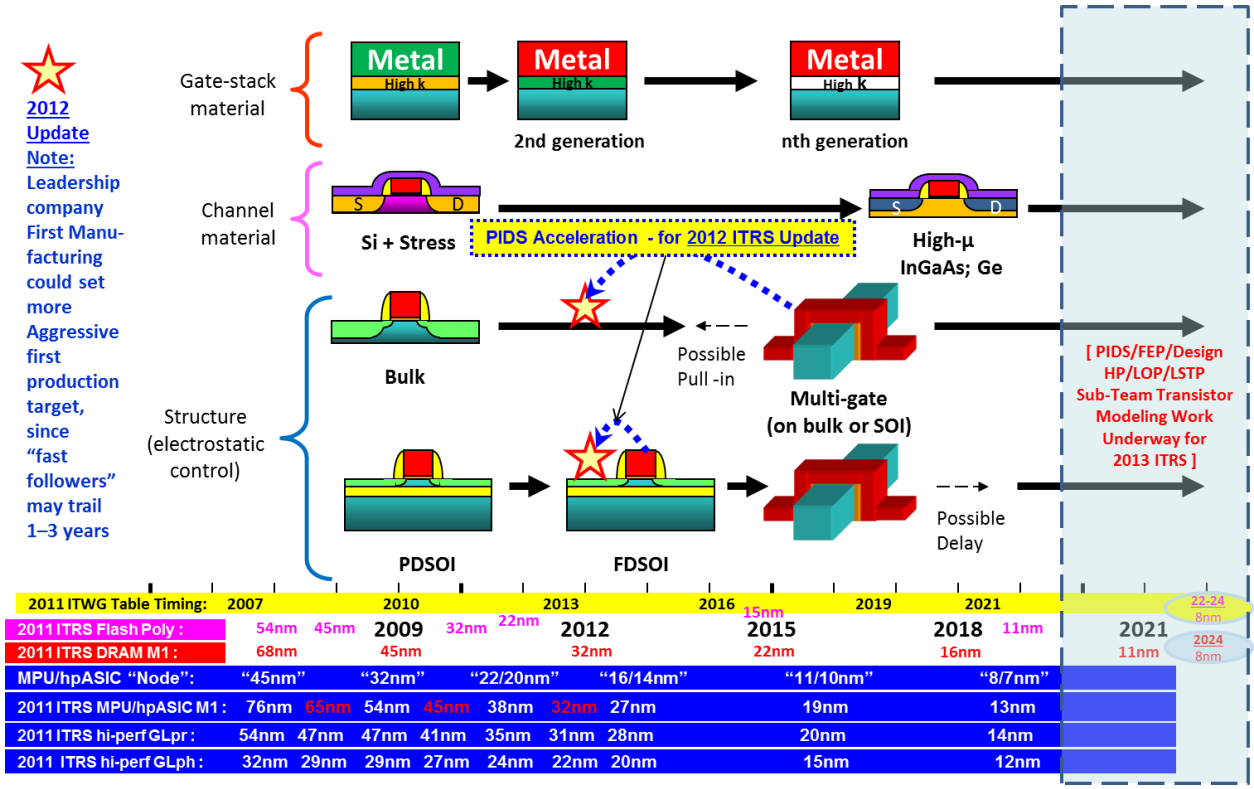


Figure 12 2011 ITRS "Equivalent Scaling" Process Technologies Timing, ORTC MPU/High-performance ASIC Half Pitch and Gate Length Trends and Timing, and Industry "Nodes"[7]

The dimensional and "equivalent scaling" technology accelerations are further evidence that the ORTC metrics are often used by semiconductor companies as a set of targets that need to be achieved ahead of schedule to secure industry leadership. Thus, the highly competitive environment of the semiconductor industry compels ongoing analysis to keep the ORTC and ITRS data current to the industry trends. Thus, the gathering and analysis of actual data, combined with the ITRS annual update process continues to provide sufficiently close tracking of the evolving international consensus on technology directions to maintain the usefulness of the ITRS to the industry.

For example, the data from technology analysis reports and public conference papers, along with company survey data and public announcements were re-evaluated during the year 2012 ITRS Update process, and there may be a need to do additional adjustments to the 450 mm timing and also the technology cycles in some of the individual product technology trends.

To reflect the diversity of product technology cycle needs and to continue close monitoring of future Roadmap trend shifts, it was agreed by the IRC to continue the practice of publishing annual technology requirements in the 2013 ITRS Renewal Work from 2013 through 2020, called the "Near-term Years," and also annual requirements from 2021 through 2028, called the "Long-term years." As seen above in Figures 10 and 11, the long-term years of the 2011 ITRS are now somewhat aligned with the timing of the especially-challenging sub-1× nm technology era (2019/13–14 nm M1 to 2026/6.3–6 nm M1).

[7] *This graphic aligns equivalent scaling projections with the ORTC MPU/high-performance ASIC half pitch and gate length trends and timing and industry "node" naming. I includes proposals for MugFET and III/V Ge acceleration for the 2012 ITRS Update work. See 2011 PIDS, FEP, ERD, and ERM chapters for additional details.*

ITRS "MOORE'S LAW" AND POWER/PERFORMANCE DRIVERS UPDATE

As part of the 2012 ITRS Update and 2013 ITRS Renewal effort, the IRC was encouraged by their regional members to examine other options for ORTC technology trend drivers in the near term years which are typical of available industry data and expectations of the chip IDM and foundry/fabless design communities. Specifically, it was suggested that the ORTC add line items which track and target: SRAM (6-transistor) Cell Area (μm^2); and also Logic (4-transistor) NAND Gate Density (Gates/mm^2)—trends established by Design TWG and ORTC models. This work will align with recommendations for simplification of the tables around PIDS high performance and low power drivers of the 2013 ITRS ITWG work.

The IRC and the Cross-TWG study groups and subteams evaluated recommendations and made proposals that would be suitable to prepare for the 2013 ITRS roadmap work kickoff in HsinChu, Taiwan in December, 2012. This work is underway to address the need to be current to the latest status of industry needs and plans. The near term range industry technology status validation and alignment activities will address the main priorities of the ITRS work mission to create the grand challenges and Potential solutions for the pre-competitive research work by academic and consortia and government laboratories.

EUV TIMING UPDATE

Extending lithography to smaller dimensions has always been difficult and the 2012 effort is no exception. Single optical exposure has reached its limit at roughly 40 nm half-pitch (hp) using 193 nm wavelength (ArF) exposure tools. Flash devices with 32 nm hp are being manufactured today using double patterning (DP) to reduce half-pitch while keeping the existing exposure NA and wavelength. This approach will be pushed harder as DRAM and MPU drive down to the 32 nm hp and Flash starts to test the limits of double patterning at 22 nm hp in 2013. For even smaller dimensions, extreme ultraviolet lithography (EUVL), multiple patterning (MP) or some non-optical lithography must be introduced. EUVL, which uses light with a wavelength of 13.5 nm, is the clear preference of the semiconductor industry for patterning smaller dimensions. EUVL has been gaining significant momentum with several manufacturers running early EUV pilot lines and some manufacturers have announced plans to purchase production tools that will be delivered in 2013.

The key technical issue gating whether EUVL will be ready on time is source power. EUVL source power is currently far behind the originally proposed roadmaps for power scale up. Higher source power is first needed to make EUVL exposure throughput sufficient for pilot process development. Then further source power increases will be needed to make volume manufacturing affordable. The current ITRS roadmap calls for a lithography patterning technology decision for 22 nm hp DRAM and MPU and for 16nm hp flash memory at the end of 2012. So it is clearly urgent to demonstrate a viable source power roadmap and progress along that roadmap. New source power roadmaps are in place from source suppliers that promise to meet this need. But if source power increases fail to meet the roadmap, this will create a cost of ownership crisis for the semiconductor industry. It will either have to adopt expensive and time consuming multiple patterning (MP) for near term nodes; or use EUVL lithography that, because of limited throughput, is much more expensive than anticipated. If EUV source power does progress as hoped, the next challenges will be a volume supply of defect free masks and improving resist materials and processes to meet manufacturing requirements. There is extensive work underway on these challenges but defect levels remain significantly off their target and resists don't meet sensitivity, LWR and photospeed targets simultaneously. The near-term challenges shown below reflect the challenges associated with these two options.

Long term, the industry will have to either extend EUV or adopt some novel patterning technique. Extending EUV would require either higher NAs or a new, shorter wavelength or both. Higher NAs will require more mirrors or constrained optical design. A new wavelength would have fewer photons and resist sensitivity issues. Either option would drive new source power requirements. Multiple patterning could be extended with directed self-assembly (DSA), an alternative patterning technology now the subject of much research and development. DSA uses existing fab tooling, and the molecular structure of the imaging material determines the sub-lithographic feature size. DSA has moved from purely research to active development in many institutions in the past year. DSA currently can only provide very simple patterns, so modified chip designs and complementary lithography techniques need to be developed. Defects are also a worry for DSA. The long term challenges chart shown below reflects the challenges associated with these two options.

Other alternative patterning technologies in the ITRS Lithography roadmap are nanoimprint and ebeam direct write. Nanoimprint is a technique like embossing. It is in development for other industries such as hard disk drive patterning as well as for the semiconductor lithography. It requires 1× masks and has stringent defectivity needs since it is a contact

printing technique. There are prototype tools available, but so far the semiconductor industry hasn't bought many of them. The key issue seems to be defects, especially defects after using a patterning template for many wafers.

Direct write ebeam is a maskless lithography (ML) technique. Since masks can be quite expensive, direct write is especially appealing for prototyping and for small production volume parts. The biggest challenge is achieving sufficient throughput to make it feasible even for small volume parts. Prototype tools with multiple ebeams and massively parallel direct writing promise to give better throughput. They are under development, but none are yet available for use.

In addition to these many challenges is the need for better supporting infrastructure, including metrology tool availability to measure and control key parameters such as critical dimension uniformity (CDU), overlay, material thicknesses, and defects.

Table 2 2012 Lithography Difficult Challenges

	Near Term Challenges (2011–2018) (16 nm Logic/DRAM @ HVM; Flash 11 nm @ optical narrowing with 16 nm in HVM)
1	Cost and cycle time of multiple patterning – especially for more than 2×
2	Optical mask complexity
3	EUV source power Defect "free" EUV masks availability mask infrastructure availability
4	Resist that meets sensitivity, resolution, LER requirements
5	Process control on key parameters such as overlay, CD control, LWR with multiple patterning
6	Retooling requirements for 450 mm transition (Economic & Technology Challenges)

	Long Term Challenges (2019–2025) (11 nm hp @ HVM)
1	Higher source power, increase in NA, chief ray angle change on EUV; Mask material and thickness optimization
2	EUV with multiple exposures for 2D patterns
3	Defect free DSA processing
4	DSA compatible design rules
5	Selection of new EUV wavelength taking resist, mask, source and tool technology into account
6	Metrology tool availability to key parameters such as CDU, thickness control, overlay, defect

WHAT IS NEW FOR 2012— THE WORKING GROUP SUMMARIES

SYSTEM DRIVERS AND DESIGN

Table 3 Major Product Market Segments and Impact on System Drivers

Market Drivers	*SOC*	*Analog/MS*	*MPU*
I. Portable/consumer			
1. Size/weight ratio: peak in 2004	Low power paramount	Migrating on-chip for voice processing, A/D sampling, and even for some RF transceiver function	Specialized cores to optimize processing per microwatt
2. Battery life: peak in 2004			
3. Function: 2×/2 years	Need SOC integration (DSP, MPU, I/O cores, etc.)		
4. Time-to-market: ASAP			
II. Medical			
1. Cost: slight downward pressure (~1/2 every 5 years)	High-end products only. Reprogrammability possible. Mainly ASSP, especially for patient data storage and telemedicine; more SOC for high-end digital with cores for imaging, real-time diagnostics, etc.	Absolutely necessary for physical measurement and response but may not be integrated on chip	Often used for programmability especially when real-time performance is not important
2. Time-to-market: >12 months			Recent advances in multicore processors have made programmability and real-time performance possible
3. Function: new on-chip functions			
4. Form factor often not important			
5. Durability/safety			
6. Conservation/ecology			
III. Networking and communications			
1. Bandwidth: 4×/3–4 years	Large gate counts	Migrating on-chip for MUX/DEMUX circuitry	MPU cores, FPGA cores and some specialized functions
2. Reliability	High reliability		
3. Time-to-market: ASAP	More reprogrammability to accommodate custom functions	MEMS for optical switching.	
4. Power: W/m^3 of system			

Table 3 Major Product Market Segments and Impact on System Drivers

Market Drivers	*SOC*	*Analog/MS*	*MPU*
IV. Defense			
1. Cost: not prime concern	Most case leverage existing processors but some requirements may drive towards single-chip designs with programmability	Absolutely necessary for physical measurement and response but may not be integrated on chip	Often used for programmability especially when real-time performance is not important
2. Time-to-market: >12 months			
3. Function: mostly on SW to ride technology curve			Recent advances in multicore processors have made programmability and real-time performance possible
4. Form factor may be important			
5. High durability/safety			
V. Office			
1. Speed: 2×/2 years	Large gate counts; high speed	Minimal on-chip analog; simple A/D and D/A	MPU cores and some specialized functions
2. Memory density: 2×/2 years			
3. Power: flat to decreasing, driven by cost and W/m^3	Drives demand for digital functionality	Video i/f for automated camera monitoring, video conferencing	Increased industry partnerships on common designs to reduce development costs (requires data sharing and reuse across multiple design systems)
4. Form factor: shrinking size	Primarily SOC integration of custom off-the-shelf MPU and I/O cores	Integrated high-speed A/D, D/A for monitoring, instrumentation, and range-speed-position resolution	
5. Reliability			
VI. Automotive			
1. Functionality	Mainly entertainment systems	Cost-driven on-chip A/D and D/A for sensor and actuators	
2. Ruggedness (external environment, noise)	Mainly ASSP, but increasing SOC for high end using standard HW platforms with RTOS kernel, embedded software	Signal processing shifting to DSP for voice, visual	
3. Reliability and safety			
4. Cost		Physical measurement ("communicating sensors" for proximity, motion, positioning); MEMS for sensors	

A/D—analog to digital ASSP—application-specific standard product D/A—digital to analog DEMUX—demultiplexer DSP—digital signal processing FPGA—field programmable gate array i/f—interface I/O—input/output HW—hardware

Table 4 Overall Design Technology Challenges

Challenges ≥ 22 nm	***Summary of Issues***
Design productivity	System-level: high level of abstraction (HW/SW) functionality spec, platform based design, multi-processor programmability, system integration, AMS co-design and automation
	Verification: executable specification, ESL formal verification, intelligent test bench, coverage-based verification
	Logic/circuit/physical: analog circuit synthesis, multi-objective optimization
	Logic/circuit/physical: SiP and 3D (TSV-based) planning and implementation flows
	Heterogeneous component integration (optical, mechanical, chemical, bio, etc.)
Power consumption	Logic/circuit/physical: dynamic and static, system- and circuit-level power optimization
Manufacturability	Performance/power variability, device parameter variability, lithography limitations impact on design, mask cost, quality of (process) models
	ATE interface test (multi-Gb/s), mixed-signal test, delay BIST, test-volume-reducing DFT
Interference	Logic/circuit/physical: signal integrity analysis, EMI analysis, thermal analysis
Reliability and resilience	Logic/circuit/physical: MTTF-aware design, BISR, soft-error correction
Challenges <22 nm	***Summary of Issues***
Design productivity	Verification: complete formal verification of designs, complete verification code reuse, complete deployment of functional coverage
	Tools specific for SOI and non-static logic, and emerging devices
	Cost-driven design flow
Power consumption	Logic/circuit/physical: SOI power management
	Logic/circuit/physical : Reliability and resilience- and temperature-constrained 3D physical implementation flows
Manufacturability	Uncontrollable threshold voltage variability
	Advanced analog/mixed signal DFT (digital, structural, radio), "statistical" and yield-improvement DFT
	Thermal BIST, system-level BIST
Interference	Interactions between heterogeneous components (optical, mechanical, chemical, bio, etc.)
Reliability and resilience	Autonomic computing, robust design, SW reliability and resilience

EMI—electromagnetic interference ESL—Electronic System-Level HW/SW—hardware/software MTTF—mean time to failure SOI—silicon on insulator

TEST AND TEST EQUIPMENT

There were no major changes to the 2012 Roadmap test tables, but there were a number of added parameters and table adjustments:

- DRAM non-performance wafer test parallelism has been adjusted to full wafer out in time. 450 mm wafer production is assumed starting in 2017. DRAM at speed performance testing has been added to the probe card table for 2012; however performance testing is limited to 32 die in parallel in 2012 and rising to 64 die in parallel out in time.
- Probing force and at performance wafer probing parameters for MPU, NAND, and LCD have also been added to the probing table for 2012.
- The DFT table has been adjusted to reflect the latest learning, delaying some improvements into later years of the roadmap. Memory DFT had been mistakenly dropped from the memory table and has been added.
- The logic table was completely redone in 2011 to include the test data volume implications of built in test architectures as compared to flat scan testing. Most of the logic table is now model based and numerous adjustments occurred as a result of minor changes to the number of gates in the largest core, the average core size and the number of cores. Some calculation errors were also corrected.
- An increase in the number of radio ports is reflected in the RF table to align with the reality that wireless communication is replacing wired connections.

LOOKING TO 2013

Because 3D devices have become a major driver to the test roadmap, 3D test issues and potential solutions will be added to the 2013 edition. Image sensor wafer testing criteria are planned to be added to the probe card table in 2013.

Table 5 Summary of Key Test Drivers, Challenges, and Opportunities

Key Drivers (not in any particular order)	
Device trends	Increasing device interface bandwidth (# of signals and data rates)
	Increasing device integration (SoC, SiP, MCP, 3D packaging)
	Integration of emerging and non-digital CMOS technologies
	Complex package electrical and mechanical characteristics
	Device characteristics beyond one sided stimulus/response model
	3 Dimensional silicon – multi-die and multi-layer
	Multiple I/O types and power supplies on same device
	Fault tolerant architectures and protocols
Increasing test process complexity	Device customization during the test process
	Feedback data for tuning manufacturing
	Dynamic test flows via "adaptive test"
	Higher order dimensionality of test conditions
	Concurrent test
	Maintaining unit level traceability
Continued economic scaling of test	Physical and economic limits of test parallelism
	Managing (logic) test data and feedback data volume
	Managing interface hardware and (test) socket costs
	Balancing general purpose equipment versus multiple insertions for system test and BIST
Difficult Challenges (in order of priority)	
Cost of test (COT) and overall equipment efficiency (OEE)	Continues to be the primary driver for innovation. Traditional drivers for COT are started to be limited by OEE
Test development as a gate to volume production (time to market)	Increasing device complexity driving more complex test development
Detecting systemic defects	Testing for local non-uniformities, not just hard defects
	Detecting symptoms and effects of line width variations, finite dopant distributions, systemic process defects
Screening for reliability	Implementation challenges and effectiveness of burn-in, IDDQ, and Vstress
	Erratic, non-deterministic, and intermittent device behavior
	Mechanical damage during the testing process
	Multi-die stacks/TSV
	Power Management Issues
Future Opportunities (not in any order)	
Test program automation (not ATPG)	Automation of generation of entire test programs for ATE
Scan diagnosis in the presence of compression	Collect better yield improvement and scan debug information
Simulation and modeling	Seamless Integration of simulation and modeling of test interface hardware and instrumentation into the device design process
Convergence of test and system reliability solutions	Re-use and fungibility of solutions between test (DFT), device, and system reliability (error detection, reporting, correction)

ATE—automatic test equipment ATPG—automatic test pattern generation BIST—built-in self test HVM—high volume manufacturing MCP—multi-chip packaging MEMS—micro-electromechanical systems COT—cost of test OEE—overall equipment efficiency

PROCESS INTEGRATION, DEVICES, AND STRUCTURES

SUMMARY

The changes made in this update are minor. They are summarized in their respective sections below.

LOGIC

No change made in all logic technologies, i.e., HP, LOP, LSTP, and III-V/Ge.

DRAM

The only changes are on the DRAM cell FET structure transition to vertical-channel transistor and transition of cell size factor from $6F^2$ to $4F^2$, both are delayed by one year from 2013 to 2014 (Table PIDS7).

NON-VOLATILE MEMORY

The only changes are for FeRAM (ferroelectric RAM, Table PIDS8b). The more noticeable changes are following.

- New nodes are introduced 1–2 years sooner.
- Cell size is increased.
- Capacitor effective area and footprint are increased. Capacitor structure transition from stacked to 3-D is delayed from 2017 to 2021.
- Capacitor voltage is increased.
- Minimum switching charge is decreased.

All other types of non-volatile memories are unchanged.

RELIABILITY

No change in this section.

All other tables remain unchanged as in the 2011 Edition.

FORWARD TO 2013

The major improvement will occur mainly in the Logic section. It is planned that to forecast transistor performance, TCAD modeling will be added to MASTAR which is compact model-based. Secondly, the transistor speed, *I/CV*, increase per year will be relaxed from 13%/year, due to the fact that the clock frequency of circuit slows down recently in increase per year. One of the low-power technologies, low operating power (LOP), will be eliminated, so low standby power (LSTP) will become the only low-power technology (renamed to low power [LP]), with both low dynamic power and low standby power.

DIFFICULT CHALLENGES

The difficult challenges remain similar to those of 2011 and are reproduced in Table 6:

Table 6 Process Integration Difficult Challenges

Near-Term 2011–2018	*Summary of Issues*
1. Scaling Si CMOS	Scaling planar bulk CMOS Implementation of fully depleted SOI and multi-gate (MG) structures Controlling source/drain series resistance within tolerable limits Further scaling of EOT with higher κ materials (κ > 30) Threshold voltage tuning and control with metal gate and high-κ stack Inducing adequate strain in new structures
2. Implementation of high-mobility CMOS channel materials	Basic issues same as Si devices listed above High-κ gate dielectrics and interface states (D_{it}) control CMOS (*n*- and *p*-channel) solution with monolithic material integration Epitaxy of lattice-mismatched materials on Si substrate Process complexity and compatibility with significant thermal budget limitations
3. Scaling of DRAM and SRAM	DRAM— Adequate storage capacitance with reduced feature size; implementing high-κ dielectrics Low leakage in access transistor and storage capacitor; implementing buried gate type/saddle fin type FET Low resistance for bit- and word-lines to ensure desired speed Improve bit density and lower production cost in driving toward $4F^2$ cell size SRAM— Maintain adequate noise margin and control key instabilities and soft-error rate Difficult lithography and etch issues
4. Scaling high-density non-volatile memory	Endurance, noise margin, and reliability requirements Multi-level at < 20 nm nodes and 4-bit/cell MLC Non-scalability of tunnel dielectric and interpoly dielectric in flash memory – difficulty of maintaining high gate coupling ratio for floating-gate flash Few electron storage and word line breakdown voltage limitations Cost of multi-patterning lithography Implement 3-D NAND flash cost effectively Solve memory latency gap in systems
5. Reliability due to material, process, and structural changes, and novel applications.	TDDB, NBTI, PBTI, HCI, RTN in scaled and non-planar devices Electromigration and stress voiding in scaled interconnects Increasing statistical variation of intrinsic failure mechanisms in scaled and non-planar devices 3-D interconnect reliability challenges Reduced reliability margins drive need for improved understanding of reliability at circuit level Reliability of embedded electronics in extreme or critical environments (medical, automotive, grid...)

Table 6 Process Integration Difficult Challenges

Long-Term 2019–2026	***Summary of Issues***
1. Implementation of advanced multi-gate structures	Fabrication of advanced non-planar multi-gate MOSFETs to below 10 nm gate length Control of short-channel effects Source/drain engineering to control parasitic resistance Strain enhanced thermal velocity and quasi-ballistic transport
2. Identification and implementation of new memory structures	Scaling storage capacitor for DRAM DRAM and SRAM replacement solutions Cost effective installation of high density 3-D NAND (512 Gb–4 Tb) Implementing non-charge-storage type of NVM cost effectively Low-cost, high-density, low-power, fast-latency memory for large systems
3. Reliability of novel devices, structures, and materials.	Understand and control the failure mechanisms associated with new materials and structures for both transistor and interconnect Shift to system level reliability perspective with unreliable devices Muon-induced soft error rate
4. Power scaling	V_{dd} scaling Controlling subthreshold current or/and subthreshold slope Margin issues for low V_{dd}
5. Integration for functional diversification	Integration of multiple functions onto Si CMOS platform 3-D integration

RADIO FREQUENCY AND ANALOG/MIXED-SIGNAL TECHNOLOGIES

SUMMARY—STATE OF RF, HF, AND AMS TECHNOLOGIES 2012: ITRS PERSPECTIVE

Radio frequency (RF), high frequency (HF), and analog mixed-signal (AMS) technologies serve the rapidly growing communications and "More-than-Moore (MtM)" markets and represent essential and critical technologies for the success of many semiconductor manufacturers. Communications products and emerging products with functionalities enabled by MtM RF, HF, and AMS technologies are becoming key drivers for volume manufacturing. Consumer products account for over half of the demand for semiconductors. Fourth generation (4G) cellular phones and tablets now have a much higher RF A/MS semiconductor content and now are a very large fraction of the mobile market compared to only 5 % of the market a few years ago. The iPAD for example has more than 19 RF and AMS front-end components.[8] The consumer portions of the RF and AMS markets are very sensitive to cost. With different technologies capable of meeting technical requirements, time to market and overall system cost will govern technology selection.

As compared to the scope of the RF and AMS ITWG chapter for the 2011 ITRS, the scope for the 2012 Update includes both wireless and tethered RF and AMS technologies. The requirements for transceiver ICs are technology drivers that contribute substantially to the recent ITRS-defined More-than-Moore thrust. This 2012 ITRS RF and AMS Chapter Update is divided into the four analog-carrier frequency bands: low frequency (LF) 0.0 GHz–0.4 GHz, radio frequency (RF) 0.4 GHz–30 GHz, millimeter-wave (mm-wave) 30 GHz–300 GHz, and terahertz (THz) greater than 300 GHz. Figure 13 lists a few examples of applications for each of these bands.

Analog – Carrier Frequency Bands			
LF Analog (0–0.4 GHz)	RF (0.4–30 GHz)	mm-wave (30–300 GHz)	THz (> 300 GHz)
Example applications			
Automotive controls	Cellular	60 GHz point-to-point	No products yet
On-chip regulators	WLAN	Imaging	Coordinate with ERD
Power management	SerDes	Automotive radar	
	ADC, DAC	Wireless backhaul	

Figure 13 RF and AMS Scope in Terms of the Analog—Carrier Frequency Bands

Strictly speaking, RF covers, as shown in Figure ITWG1, the 0.4 GHz–30 GHz frequency range. Considering the mm-wave and sub-mm-wave (THz) applications, we should change the generic designation from the present RF to high-frequency (HF) to reflect the much wider spectrum. The members of the ITWG will develop a consensus for this terminology in the next 2013 RFAMS ITRS Chapter.

Four of the technology/devices subgroups cover applications below 10 GHz: CMOS, bipolar, passives, and high-voltage MOS. The fifth subgroup on mm-wave applications focuses on power and low-noise requirements of both III-V compound semiconductor and silicon-based devices used in transceiver ICs.

Some portions of the RF and AMS technologies roadmap pertain more to prototype capabilities rather than usual CMOS volume production of most of the other ITRS Chapters. Production implies applications and markets. But, emerging mm-wave connectivity and imaging applications that are part of the scope for the RF and AMS ITWG currently lag technology and processing capabilities for reliable manufacturing.

Figures of merit (FoMs) for device technologies that relate to those circuit-level FoMs needed to support the performance requirements of systems drive the RF and AMS roadmap. The FoMs included in the RF and AMS roadmap are those FoMs for low-noise amplifiers (LNA), voltage-controlled oscillators (VCO), power amplifiers (PA), analog-to-digital converters (ADC), and serializer-deserializers (SerDes).

***CMOS technologies*—**The 2012 updated technology requirements tables reflect the RF and analog performance metrics needed to support the technology roadmap developed by the ITRS Process Integration, Devices, and Structures (PIDS) working group. These performance metrics include f_T, f_{MAX}, NF_{MIN}, analog gain, flicker noise, and threshold voltage matching. Compared to the 2009 roadmap, f_T increased faster in the 2011 roadmap and in the present 2012 Update

[8] *http://www.bizjournals.com/prnewswire/press_releases/2012/05/28/SP14461, July 30, 2012.*

roadmap. The 2012 updated RF and AMS technology requirements tables have parasitic resistances and capacitances needed to support the ITRS Interconnect and Front End Processing (FEP) roadmaps. The 2013 roadmap will give the above performance FoMs obtained from TCAD-based modeling methods that are similar to those used in the PIDS roadmap, but with the extension of using compact models for predicting *extrinsic* FoMs including the device parasitics relevant to high-frequency analog circuit design. Also, the 2013 RF and AMS roadmap will include more details obtained from TCAD models for realistic layout and the resulting parasitic impedances.

***Group IV bipolar technologies*—**Only minor changes occurred in the 2012 technology requirements tables. These changes are primarily: 1) For high-speed NPN transistors, a one-year delay for the increase in f_T and updating parameters related to f_T such as W_E, BV_{CEO}, BV_{CBO}, J_C at peak f_T, NF_{MIN} and SL_i, and 2) For high-speed PNP transistors, updating the linearity efficiency f_{LE}. The contributors to the roadmap expect major changes for high-speed NPN and PNP bipolar transistors. These expected changes include moving to a roadmap based on TCAD and compact modeling simulations; moving to performance plateaus every 3 to 4 years that are linked to applications and the foregoing system drivers.

***III-V compound semiconductor technologies*—**We have assumed "production" implies that at least one company offers products with "data sheets" or that the technology is available for custom designs from one or more companies as a foundry service. The productions dates for scaled InP HEMT, InP HBT, and GaN HEMT shift by one year earlier. The "pull" for these technologies partly drives this shift. The III-V roadmap truncates at the following expected ends of scaling: GaAs PHEMT in 2015, GaAs power MHEMT in 2019, and InP power HEMT in 2013. However, we expect that low noise GaAs MHEMT and InP HEMT, InP HBT, and GaN HEMT will continue with physical scaling. The 2012 Update, as in the past, has only D-mode FETs. The FoMs depend on technology and will include: f_T, f_{MAX}, g_m, and V_{BD} ; power, gain, and efficiency at 10, 24, 60, 94, 140, and 220 GHz; NF_{MIN} and G_A at 10, 24, 60, and 94 GHz ; LNA NF and G_A at 140 and 220 GHz. We plan to add E-mode devices in the 2013 roadmap.

***High-voltage MOS technologies*—**The HVMOS section that was new in 2011 includes both HVNMOS and HVPMOS devices for power management and display-driver applications. The FoMs presented in this section are BV_{DSS}, R_{ON} x area with the framework of the integrated CMOS node. The 2012 Update HVMOS roadmap is essentially the same as the 2011 roadmap. We expect that the 2013 HVMOS roadmap will include higher voltages and automotive and industrial applications. Because of these additions, the devices and FoMs in revised HVMOS roadmap for 2013 will have an impact on the passive devices roadmap. TCAD based predictions should also be used here, since the HF characteristics of these devices are very sensitive to parasitics.

***On-chip passive device technologies*—**There have been no major revisions since 2011. The updated 2012 technology requirement tables emphasize on-chip passive devices and refresh the values for FoMs as functions of technology nodes (time). We will synchronize the 2013 roadmap for passive devices with the application-based framework of the RF and AMS chapter by capturing the unique requirements of the applications and by reflecting the silicon, III-V, and HVMOS performance metrics needed to support those applications.

Table 7 RFAMS Difficult Challenges

Challenges	***Summary of Issues***
CMOS technologies	Many of the materials-oriented and structural changes being invoked in the digital roadmap degrade or alter RF and analog device behavior. Complex tradeoffs in optimization for RF, HF, and AMS performance occur as different mechanisms emerge as limiting factors. Examples include series resistances at gate, source and drain, that greatly affect parasitic impedances and the impact of such local interconnect parasitics on $f_{MAX.}$ Fundamental changes of device structures, e.g., multiple-gates and silicon-on-insulator (SOI), to sustain continued digital performance and density improvements greatly alter RF and AMS characteristics. Such differences, along with the steady reduction in supply voltages, pose significant circuit design challenges and may drive the need to make dramatic changes to existing design libraries.
Group IV bipolar technologies	Even though it is a challenge for the HS-NPN to increase the unity current gain cut-off frequency f_T by more aggressive vertical profiles, it is less of a challenge to achieve fMAX > f_T. What is unclear today is how large the ratio f_{MAX}/f_T needs to be for future circuit applications. That is, the challenge is to determine what this ratio should be by using the "plateau technologies" for the next roadmap and appropriate benchmark Circuits. A key challenge for the HS-PNP also is increasing f_T by more aggressive vertical profiles. In addition to the inherent minority carrier mobility differences between electrons and holes, shrinking the vertical profile of a SiGe PNP is more challenging because it requires controlling the valence band offsets to avoid the appearance of parasitic barriers. Another challenge for the HS-PNP is the difficulty of the co-integration with HS-NPN and CMOS. This integration always adds more constraints on the HS-PNP fabrication. Since lateral scaling requirements for HBTs are significantly relaxed compared with those for MOSFETs, vertical profile fabrication under the constraints of overall process integration appears to be the bigger challenge. The reduction of imperfections and the increase of current carrying capability of the emitter and collector contact metallization are further challenges that need to be met by process engineers on the way to achieving the physical limits of this and any other technology.
III-V compound semiconductor technologies	The unique challenges are yield (manufacturability), substrate size, thermal management, integration density, dielectric loading, and reliability under high fields. Challenges common with Si-based circuits include improving efficiency and linearity/dynamic range, particularly for power amplifiers. A major challenge is increasing the functionality of power amplifiers in terms of operating frequency and modulation schemes while simultaneously meeting increasingly stringent linearity requirements at the same or lower cost.
High-voltage MOS	Several aspects of high voltage devices and the associated base technology make it difficult and unlikely that the HV roadmap for the future will follow the lithographic shrink seen for CMOS because the HV designs cannot take advantage of the lithography capability to shrink the intrinsic HV device dimensions, analog devices are usually large to improve the noise and mismatch, and the digital content of a HV chip is usually a small fraction of the chip area.
On-chip passive device technologies	The co-integration of active and passive devices introduces process complexity and can lead to manufacturing control and costs challenges. The decreasing overall stack as well as the individual metal heights results in increasing resistive losses and vertical parasitic capacitances and limits the quality-factors of the on-chip integrated inductors, transformers, and capacitors.

MICROELECTROMECHANICAL SYSTEMS (MEMS)

Micro-electro-mechanical systems (MEMS) are fabricated using techniques similar to those used for integrated circuits to create micrometer-sized mechanical structures (suspended bridges, cantilevers, membranes, fluid channels, etc.) that are often integrated with analog and digital circuitry. MEMS can act as sensors, receiving information from their environment, or as actuators, responding to a decision from a control system to change the environment. This first iteration of the ITRS MEMS chapter focused on near-term (5-year) advances in device performance metrics, design and simulation, assembly and packaging, and testing. A major conclusion reached is that while the back-end of MEMS manufacturing (packaging and testing) consumes two thirds of the total manufacturing cost, and continues to rise, virtually all R&D investment has been on the front-end of manufacturing (devices and process development). The development of a consensus opinion that documents possible solutions for the issues facing the industry, which is the primary output from our technology roadmapping, can be used as a tool to optimize R&D investment that meets the critical manufacturing needs to address the issues faced in the back-end of MEMS manufacturing.

SCOPE

The ITRS MEMS technology roadmap focuses on the key technologies associated with mobile internet devices, such as smart phone and tablet computers. The key MEMS device technologies considered are: accelerometers and gyroscopes, microphones, and RF MEMS, including resonators, varactors, and switches. These applications represent the fastest growing segment in MEMS manufacturing, according to 2011 market forecasts by iSuppli, Yole Development, and SEMI. The roadmap considered both the evolution of discrete MEMS devices and integrated MEMS technologies. It also reviews emerging MEMS applications, including optical filters, picoprojectors, the electronic nose, microspeakers, and ultrasound devices.

DISCRETE MEMS ACCELEROMETERS, GYROSCOPES, AND MICROPHONES

Discrete MEMS accelerometers and gyroscopes are expected to see continuous incremental improvement in resolution, bias, and drift, with resolutions improving by a factor of 2, from 100 μg/√Hz to 500 μg/√Hz for accelerometers and 20 m°/s/√Hz to 8 m°/s/√Hz for gyroscopes, by 2017. MEMS microphones are expected to see an improvement in phase noise from -120 dBc/Hz to -160 dBc/Hz at 1 kHz. Challenges faced by manufacturers of discrete MEMS devices come from the required cost, size, and power reductions. The package size of MEMS accelerometers and gyroscopes is forecasted to decrease from 3×1×1 mm to 1×1×1 mm and 3×3×1 mm to 2×2×1 mm 2017, respectively. MEMS gyroscopes require a power reduction in power consumption from 18 mW to 5 mW by 2017, with no known solutions at the present time.

RF MEMS

RF MEMS resonators, varactors, and switches are also expected to see a continuous incremental improvement in performance. The greatest challenge that these devices face in order to penetrate into the mobile internet market is increasing their reliability from the present typical mean times to failure. Meeting this challenge requires advancing knowledge of the physics of failure in materials used in MEMS, reliability simulation tools, and better methods for accelerated lifetime testing. RF MEMS also specifically call out requirements for inductors with quality factors $Q > 50$ integrated at the package level and methods for minimizing package interconnect length and loading.

MEMS INERTIAL MEASUREMENT UNITS (IMUS)

The greatest challenges by manufacturers of integrated MEMS for mobile internet device technologies were in relation to their integration path towards the inertial measurement unit (IMU); a device that incorporates a 3-axis accelerometer, 3-axis gyroscope, 3-axis magnetometer (compass), and a pressure sensor (altimeter). The integration path for the MEMS IMU is forecasted to increase from 9 DoF to 10 DoF by 2014 at the package level and from 6 DoF to 10 DoF by 2015 at the chip level. The greatest cause for concern for multimode sensor technologies relates to testing. The cost of testing has been continuously increasing yet the price of the devices continues to fall; a trend that cannot be sustained. The challenges of testing are further compounded by the increasing complexity of the tests, which require testing the multiple functionalities (acceleration, angular rate, direction, and elevation) of the IMU.

CHANGES IN THE 2012 UPDATE

The MEMS ITWG focused this year on a complete rewrite of the iNEMI MEMS chapter, which includes a new discussion on MEMS for consumer medical applications and a proposes the idea of integration nodes as a path for MEMS sensor fusion modeled after the evolution of the IMU. The 2012 update to the ITRS MEMS Technology Roadmap

leveraged this effort to update device performance metrics and a reorganization of the technology requirements tables. Predicted cost metrics for devices have been dropped from the tables because of a variety of concerns from the manufacturers; instead, cost targets for testing are listed. The integration path for MEMS inertial measurement units has been removed from the accelerometer and gyroscope tables and put into a new table. The integration path for IMUs has been accelerated by 1 year; the 9 DoF device integrated at the package level as well as the 6 DoF device integrated at the chip level were moved from 2013 to 2012. Finally, the RF MEMS tables have been combined into a single table.

DIFFICULT CHALLENGES

Table 8 MEMS Difficult Challenges

Challenge	***Need***
Assembly and packaging	• Standardization for MEMS packaging to support integration. • Packages are needed that reduce or eliminate mechanical stress and enhance hermeticity. • Package data that can be used to accurately predict the effect of the package on device performance.
Device testing	• Move from testing at the device level towards more testing towards the wafer level. • Validated tools to predict device performance from wafer tests. • Methodologies to "Design for Test."
Reliability	• More knowledge of the physics of failure is required to develop accelerated life tests. • Need to share information. Individual solutions exist but are not being generalized across the industry.

EMERGING RESEARCH DEVICES

The ITRS Emerging Research Devices (ERD) ITWG, in collaboration with the Emerging Research Materials (ERM) ITWG and co-sponsored by the National Science Foundation, evaluated and updated their information in several key areas for beyond CMOS information processing, memory, and storage technologies. In particular, the ERD and ERM ITWGs thoroughly assessed memory select devices, storage class memory (SCM), emerging logic devices, and emerging architectures in four workshops co-sponsored by NSF.

Memory select devices and SCM are two new sub-sections added in the 2011 ERD chapter. Memory select devices are considered scaling bottleneck for some promising emerging memories, e.g., resistive RAM (RRAM). Select devices need to not only isolate memory devices in an array but also provide sufficient operation current and voltage. Two-terminal diode-like memory select devices that meet the performance requirements may become critical technology enablers for emerging memories.

A workshop on memory select devices was organized by ERD/ERM in April 2012 to evaluate a set of device options and their performance requirements, including transistors, diodes, complementary resistive switches, metal-insulator-transition switches, and mixed ionic electronic conduction (MIEC) devices.

Another ERD/ERM workshop was organized in July 2012 to assess SCM applications of emerging memory devices and architectures. SCM is an emerging memory category that seeks to combine the benefits of solid-state memory (e.g., high performance and robustness) with the data retention capabilities and low cost of conventional hard-disk drive (HDD). To be successful, SCM technologies have to provide non-volatility (from 1 week to 10 years), low read and write latencies (from hundreds of nanoseconds to tens of microseconds), physical durability, and ultra-low cost per bit. In addition, the potential of prototypical and emerging memory devices for SCM applications needs to be assessed in the context of memory architectures. It is likely that architectures and interfaces of these emerging memories will be significantly different from the existing commercialized storage technologies (e.g., HDD) and nonvolatile semiconductor flash memory. Among the emerging memories evaluated in the workshop, PCM and RRAM are considered promising candidates. The availability of functional select devices also impacts the suitability of these memories for SCM applications.

An ERD/ERM Logic Device workshop was conducted in September 2012 to evaluate the maturity of different categories of emerging devices surveyed in the 2011 ERD chapter. The scope of the assessment is expanded beyond digital electronics to include analog and reprogrammable applications of these devices. The workshop emphasized the importance of consistent benchmarking of emerging devices from device to circuit levels. Another ERD/ERM workshop scheduled in December 2012 is dedicated to emerging architectures. The objective is to develop a systematic taxonomy for emerging architectures and assess their potential in beyond-CMOS applications. Both the logic device workshop and emerging architecture workshop provide updated information and improved organization for the logic and architecture sections of 2013 ERD chapter.

EMERGING RESEARCH MATERIALS

The Emerging Research Materials (ERM) ITWG does not plan to make any updates or changes to the 2011 ERM chapter, but is focused on collecting input on changes in materials and technology status for the 2013 ITRS rewrite. The ERM has participated with the ERD in several workshops and we are holding e-workshops on materials for lithography, front end process, interconnects, and assembly and package. The goal is that these workshops will enhance the chapter with the latest industry materials and trends.

We have participated with the Emerging Research Devices ITWG in workshops on memory select devices, storage class memories, and logic devices in 2012 and will be identifying material requirements for the devices covered. For memory devices, the ERM is planning e-workshops on spin materials for out of plane STT, complex metal oxides for RRAM, and novel materials for memory select devices. For logic device alternate channel materials, the ERM is planning updates on carbon based device (graphene and carbon nanotubes) materials, semiconductor nanowires, p-channel III-V materials. For beyond CMOS logic, the ERM is planning updates on properties of spin materials, strongly correlated electron materials, semiconductor spin properties, and interface coupling between materials.

For lithography, the ERM will be holding a number of teleconferences in 2012 and early 2013 to update the status of photoresist and hard mask materials for 193 nm and EUV lithography. Nanocomposite resist with ~2 nm particles of HfO_2 or ZrO_2 have demonstrated improved sensitivity and resolution through the use of new ligands. Inorganic-organic hybrid (HfO_2-based) resist are also demonstrating improved resolution and sensitivity; however, resolution and sensitivity are a tradeoff as with conventional resists. These materials also can have dramatically higher etch resistance than SiO_2 and it is possible to use them as hard masks with patterned photoresist. Directed self assembly (DSA) continues to be evaluated as a potential lithography extension technology with block-copolymers and polymer blends continues to make progress. An informal survey identified that participants in industry have active plans to evaluate DSA for contact rectification and pattern density multiplication, but there was some interest in DSA for line edge roughness/line width reduction (LER/LWR) improvement. A second survey identified pre-competitive areas that needed consortia support to be: defects, materials specifications, simulation, metrology (2D and 3D), design tools, high χ (phase segregation energy) block co-polymers and prediction and modification of surface energy to control morphology.

In support of FEP, the ERM is evaluating conformal doping, ultra high κ gate dielectrics, and nano-contacts. The ability to produce conformal dopant deposition on 3D structures is important as multigate structures are introduced and scaled to high densities and a workshop is being planned on this in February, 2013. In addition, the ERM is planning an e-workshop on modeling high κ dielectrics to identify potential materials for second generation gate applications. As devices scale to sub 10 nm dimensions, contact resistivity may limit performance of devices, so the ERM is planning a workshop on contact resistivity in the spring of 2013.

For interconnects, the ERM had e-workshops on novel low κ dielectrics, ultrathin copper diffusion barrier layers, and carbon based interconnects.

A critical challenge for the assembly and packaging is to identify "zero residue" adhesives that could be used in a number of applications. A joint ERM and Assembly and Package e-workshop reviewed progress in for stimulus activated adhesive release included thermally or photon activated mechanisms. We are also planning e-workshops on low assembly temperature electrical interconnects and package polymers (< 200°C), electrical interconnect materials that have low electrical resistance and contact resistance, high electromigration resistance, and high resistance to fatigue.

The ERM is preparing to update the emerging materials earliest potential intercept table to help the ESH TWG identify when to assess potential issues and tradeoffs in their implementation, and to include sustainable and green chemistry principles in the ITRS.

FRONT END PROCESSES

Updates to the 2011 FEP content are minimal for the 2012 ITRS publication. Changes to the FEP tables in an update year such as 2012 are typically minor and often may occur as a result of adjustments in the ORTC scaling guidelines which impact the models associated with FEP calculated table values.

Efforts in 2012 have primarily focused on preparatory work for a broader 2013 revision of chapter content. Actions such as discussing requirements in the FeRAM sub-TWG of ferroelectric properties in the advent of scaling and low voltage, as well as cleaning methods in the Surface Preparation sub-TWG to address static friction-related pattern collapse in MEMS, were conducted. Tracking of 450 mm timing and associated impact of Starting Material sub-TWG table values remained an ongoing initiative and will again be addressed in 2013.

Additional activities were undertaken in conjunction with other ITWGs to address interconnected matter. Noteworthy examples include consideration of new metrology requirements for ultra-shallow junction (USJ), 3D devices and alternate channel materials with the Metrology ITWG, as well as the pull-in of MuGFETs into 2012 and FDSOI into 2013, aligning with the PIDS ITWG.

Attempts were also made with other ITWGs to reduce inconsistencies in content and values between interrelated tables, such as the case for FeRAM between PIDS and FEP.

FEP has been characterized in the past several years by continuing innovations. The expectation is that this will become even more prevalent in 2013 and beyond.

Table 9 Front End Processes Difficult Challenges

Difficult Challenges ≥ 11 nm	***Summary of Issues***
	Strain Engineering – continued improvement for increasing device performance – application to FDSOI and multi-gate technologies
	Achieving low parasitics (resistance and capacitance) and continued scaling of gate pitch
	Achieving DRAM cell capacitance with dimensional scaling – finding robust dielectric with dielectric constant of ~60 – finding electrode material with high work function
	Achieving clean surfaces free of killer defects – with no pattern damage – with low material loss (< 0.1 A)
	450 mm wafers—meeting production level quality and quantity
Difficult Challenges < 11 nm	***Summary of Issues***
	Continued scaling of HP multigate device in all aspects: EOT, junctions, mobility enhancement, new channel materials, parasitic series resistance, and contact silicidation.
	Introduction of high mobility channels (based on III-V and Ge) to replace strained Si
	Lowering required DRAM capacitance by $4F^2$ cell scheme or like, while continuing to address materials challenges
	Continued achievement of clean surfaces while eliminating material loss and surface damage and sub-critical dimension particle defects
	Continued equivalent oxide thickness (EOT) scaling below 0.7 nm with appropriate metal gates
	Continued charge rention with dimensional scaling and introduction of new non-charged based non-volatile memory (NVM) technologies

LITHOGRAPHY

Extending lithography to smaller dimensions has always been difficult and this year is no exception. The semiconductor industry needs to select a lithography method for 22 nm half pitch DRAM and 16 nm half pitch flash memory at the end of 2012, but no clear choice has emerged yet. ArF immersion lithography cannot be extended much below 40 nm half pitch and ArF immersion with double patterning will not meet these pitches. The possibilities for further progress are triple or quadruple patterning, EUV lithography, or some novel alternative patterning technique. The novel techniques that are currently possibilities in the ITRS roadmap are mask-less lithography (ML), nanoimprint lithography (NIL) or directed self assembly (DSA).

The industry has invested heavily in EUV, and it is clearly the front up approach for printing smaller features. But there have been major delays in scaling up EUV source power. These delays mean that wafer throughput on existing exposure tools is so limited that EUV materials, process and imaging learning have been constrained. It means that any actual EUV implementation for pilot use is likely to be more expensive per patterned wafer than originally predicted. And it may mean that the industry will choose another option for 22 nm half pitch DRAM and 16 nm half pitch Flash memory lithography or even that the industry will delay the schedule for introducing these products.

Alternative next generation patterning techniques are not ready for various reasons. Maskless involves direct writing of patterns in resist with e-beams. No mask is needed, which is very appealing, especially for low volume applications; but to get any reasonable throughput, massively parallel writing with a thousand or thousands of e-beams at once is needed. Such tools are under development, but no working prototypes exist today. Nanoimprint involves stamping out patterns in a photosensitive material using a 1× template and then curing the patterns in place. Tools are available for prototype work and they can print high resolution patterns. But defectivity after pattering multiple wafers is an issue that hasn't been solved. Directed self assembly shows great resolution and holds the promise for inexpensive pitch and/or CD reduction. It has shown large progress and activity evaluating DSA has increased tremendously. But it can only prepare simple repetitive patterns so designs for chips have to be modified if it is to be used. Also low full wafer DSA defectivity needs to be demonstrated. Both of these issues will take substantial time to resolve.

Since none of these techniques will be ready for selection as a patterning technology for pilot line and high volume use by the end of this year, this leaves multiple patterning, such as triple or quadruple patterning, as the only available technology that could be chosen instead of EUV at the end of this year. This would involve such complicated processing and such long process flows that the industry is faced with a true dilemma if it is to scale up new nodes on schedule—either start using EUV in 2013 despite likely slower throughput and much higher cost than planned for, or spend much development time and accept complicated process flows with high mask costs. Looking at the revised near-term challenges table from this year's roadmap shown below in Table 10, it is clear that the top five challenges are issues that need to be solved in order to make either EUV or multiple pattering work for the upcoming nodes. The first two challenges are issues with multiple patterning's difficulty and complexity. The next two challenges reflect the issues that are key for making EUV lithography a successful technology. The fifth challenge reflects the difficulty and already stretched performance of current lithography. This can also be seen in the 2012 Lithography tables, where many near-term needs are colored red, meaning "manufacturable solutions are not yet known."

Table 10 Lithography Near-term Challenges

Near Term Challenges (2011–2018) (16 nm Logic/DRAM @ HVM; Flash 11 nm @ optical narrowing with 16 nm in HVM)
Cost and cycle time of multiple patterning – especially for more than 2×
Optical mask complexity
EUV source power Defect “free EUV masks availability mask infrastructure availability
EUV Resist that meets sensitivity, resolution, LER requirements
Process control on key parameters such as overlay, CD control, LWR with multiple patterning
Retooling requirements for 450 mm transition (Economic & Technology Challenges)

LITHOGRAPHY—LONG TERM CHALLENGES

In the longer term, either a path for improving the resolution of EUV lithography or an alternative form of patterning that is manufacturable will be needed to maintain progress against the industry roadmap. Improving EUV resolution will require either increasing NA or reducing the wavelength to smaller EUV wavelength. Either option will require more source power and improved mirror technology for EUV optics and mirrors. A second EUV challenge will be to do EUV double patterning as device patterns get smaller. Even if single pattering will resolve the fundamental pitch of the pattern, two dimensional structures can require double patterning. Doing this with EUV will put pressure on throughput and cost and is another reason further source power increases will be needed.

Of the alternative technologies in the roadmap, DSA has had by far the most publication activity in the past year. It has the promise of high throughput and high resolution with low processing cost. But it has two major challenges to overcome. One is the challenge of defects. Some progress has been reported that shows potential for low defects, but no one has demonstrated such a process. The second challenge is design. DSA can make arrays of parallel 1:1 lines and spaces, using demonstrated processes. But turning these lines and spaces into actual device patterns will require cut levels and other secondary exposures and processing. It will also require special designs and design software to use the resulting patterns in real devices.

Metrology is another challenge. As features get smaller, specifications require higher resolution and more precise measurements. In some cases already, such as particles embedded in resist, suppliers measure the defect size they can measure rather than the actual defect size needed. Improved metrology is going to be a significant challenge for future nodes. A list of all the challenges is shown in the table below.

Table 11 Lithography Long-term Challenges

Long Term Challenges (2019–2025) (11 nm hp @ HVM)
Higher source power, increase in NA, chief ray angle change on EUV; Mask material and thickness optimization
EUV with multiple exposures for 2D patterns
Defect-free DSA processing
DSA compatible design rules
Selection of new EUV wavelength (taking resist, mask, source and tool technology into account)
Metrology tool availability to key parameters such as CDU, thickness control, overlay, defect

LITHOGRAPHY—CHANGES TO TABLES IN 2012

Changes made in the tables are listed below:

- The size of a contact in resist has been removed from the basic requirements and put separately into the optical and EUV tables. What remains in the basic requirements table is the size of an etched contact, which is the same no matter what technology is used to expose it. EUV has the capability to print a much smaller contact hole than ArF immersion lithography, so it is expected that EUV printed contacts in resist will be smaller than optical ones and also require less size bias during etching.
- The multiple patterning tables have been updated to reflect the predominant industry practice of intercalating different exposures rather than splicing them.

- The resist sensitivities table has been updated to reflect the expected impact of shot noise requirements on e-beam direct write resists.
- The color coding for EUV reticle reflectivity has been changed because most EUV reticles currently don't meet the desired 65% reflectivity number after processing, but this is adequate for current EUV reticle use. It is expected that further mask blank and mask processing improvements will enable masks with the desired 65% reflectivity in the future in time for volume manufacturing.
- A table was added called materials requirements. It specifies new or improved materials needed by lithography. It will serve to communicate lithographic needs to the ERM team.

INTERCONNECT

The Interconnect Technology Workgroup made changes to the 2011 chapter based on some errors in references and formatting. These changes will hopefully contribute to the reader's understanding of the main issues related to interconnect scaling. In preparation for the 2013 rewrite over the past year the team has done its best to recruit new ITWG members. We successfully recruited new members across the range of areas covered in the Interconnect chapter so that we will be prepared to provide the most relevant information regarding all aspects of the interconnect technology and provide insight from industry experts on the areas needing the most urgent attention.

In discussions during intra-group and cross ITWG meetings we have confirmed that the Interconnect ITWG's responsibilities include from via 0 through the final metal and ILD deposition and CMP as well as all steps in between these layers. The Assembly and Packaging ITWG is responsible for technology related to steps beyond. However, there is a significant gray area in the 3D-die stacking space. There is not a clear distinction for the end point for interconnect and the beginning for Assembly and Packaging. This lack of distinction arises from several preparation steps required in the 3D process flow including temporary bonding, wafer thinning, TSV expose, RDL introduction and microbumping followed by debonding. There can be a variation both in the order of some of these steps as well the location where the steps are completed. For example, the full process may be completed at an IDM or at some predetermined step the wafer may be shipped to outsourced assembly and test suppliers. It is important to delineate the responsibility for processing steps/area for each ITWG. However, it is possible that each IDM or foundry may take a different approach which make assignment of these areas to a specific ITWG ambiguous. In the near term the areas of contention will be reviewed jointly by the Interconnect and A&P ITWGs.

Also for 2012 the Interconnect TWG completed nearly a full review of the interconnect tables. Every attempt was made to update all the pertinent values. Further, for the first time a major effort was places on simplifying several of the tables. There were many rows in the tables that contained legacy information that at one time was probably useful but now many of the rows of values seemed more to detract rather than contribute to the reader's overall value and understanding in the interconnect chapter.

Finally, I would like to thank the efforts of the interconnect team and the other TWGs for their efforts in helping to improve this chapter.

Table 12 Interconnect Difficult Challenges

Five Most Critical Challenges ≥ 16 nm	***Summary of Issues***
Material *Introduction of new materials to meet conductivity requirements and reduce the dielectric permittivity*	*The rapid introductions of new materials/processes that are necessary to meet conductivity requirements and reduce the dielectric permittivity create integration and material characterization challenges.*
Manufacturable Integration *Engineering manufacturable interconnect structures, processes and new materials*	*Integration complexity, CMP damage, resist poisoning, dielectric constant degradation. Lack of interconnect/packaging architecture design optimization tool*
Reliability *Achieving necessary reliability*	*New materials, structures, and processes create new chip reliability (electrical, thermal, and mechanical) exposure. Detecting, testing, modeling, and control of failure mechanisms will be key.*
Metrology *Three-dimensional control of interconnect features (with its associated metrology) is required to achieve necessary circuit performance and reliability.*	*Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels combined with new materials, reduced feature size, and pattern dependent processes create this challenge.*
Cost and Yield for Manufacturability *Manufacturability and defect management that meet overall cost/performance requirements*	*As feature sizes shrink, interconnect processes must be compatible with device roadmaps and meet manufacturing targets at the specified wafer size. Plasma damage, contamination, thermal budgets, cleaning of high A/R features, defect tolerant processes, elimination/reduction of control wafers are key concerns. Where appropriate, global wiring and packaging concerns will be addressed in an integrated fashion.*

Five Most Critical Challenges < 16 nm	***Summary of Issues***
Material *Mitigate impact of size effects in interconnect structures*	*Line and via sidewall roughness, intersection of porous low-κ voids with sidewall, barrier roughness, and copper surface roughness will all adversely affect electron scattering in copper lines and cause increases in resistivity.*
Metrology *Three-dimensional control of interconnect features (with its associated metrology) is required*	*Line edge roughness, trench depth and profile, via shape, etch bias, thinning due to cleaning, CMP effects. The multiplicity of levels, combined with new materials, reduced feature size and pattern dependent processes, use of alternative memories, optical and RF interconnect, continues to challenge.*
Process *Patterning, cleaning, and filling at nano dimensions*	*As features shrink, etching, cleaning, and filling high aspect ratio structures will be challenging, especially for low-κ dual damascene metal structures and DRAM at nano-dimensions.*
Complexity in Integration *Integration of new processes and structures, including interconnects for emerging devices*	*Combinations of materials and processes used to fabricate new structures create integration complexity. The increased number of levels exacerbate thermomechanical effects. Novel/active devices may be incorporated into the interconnect.*
Practical Approach for 3D *Identify solutions which address 3D structures and other packaging issues*	*3-dimensional chip stacking circumvents the deficiencies of traditional interconnect scaling by providing enhanced functional diversity. Engineering manufacturable solutions that meet cost targets for this technology is a key interconnect challenge.*

FACTORY INTEGRATION

- No major changes to Factory Integration tables/potential solutions
  - Potential changes being logged and will be updated at one time
- Data discussion with key ITWGs
  - Lithography: EUV/E-beam data volumes
  - Metrology: FI agreed to do AEC/APC write up edits in the Metrology chapter
  - ESH: Joint teams set up to do common table/write up edits
    - Agreed to provide inputs to G450C requirements documents
  - Yield: Joint effort on developing predictive yield models
- Revising Factory Integration Vision/scope to better align to the changing manufacturing environment and challenges
  - Manufacturing technology is key to profitability

Table 13 Factory Integration Difficult Challenges

Difficult Challenges through 2019	***Summary of Issues***
1. Responding to rapidly changing, complex business requirements	• Increased expectations by customers for faster delivery of new and volume products (design → prototype and pilot → volume production) • Rapid and frequent factory plan changes driven by changing business needs • Ability to load the fab within manageable range under changeable market demand, e.g., predicting planning and scheduling in real-time • Enhancement in customer visibility for quality assurance of high reliability products; tie-in of supply chain and customer to FICS operations
2. Managing ever increasing factory complexity	• Quickly and effectively integrating rapid changes in process technologies • Increased requirements for high mix factories. Examples are 1) significantly short life cycle time of products that calls frequent product changes, 2) the complex process control as frequent recipe creations and changes for process tools and frequent quality control criteria due to small lot sizes • Manufacturing knowledge and control information need to be shared as required among factory operation steps and disparate factories • Need to concurrently manage new and legacy FICS software and systems with increasingly high interdependencies • Ability to model factory performance to optimize output and improve cycle time for high mix factories • Need to manage clean room environment for more environment susceptible processes, materials, and, process and metrology tools • Addressing need to minimize energy resource usage and waste; e.g., need to integrate fab management and control with facilities management and control • Comprehending increased purity requirements for process and materials Providing a capability for more rapid adaptation, re-use and reconfiguration of the factory to support capabilities such as rapid new process introduction and ramp-up. This includes a challenge of supporting evolution of a FI communication infrastructure to support emerging capabilities beyond interface A. • Supporting adoption and migration of equipment communication protocol standards to meet ITRS challenges and be in sync with emerging technologies in systems communication and management such as XML and cloud computing. • Meeting equipment design challenges in maintaining yield and improving maintenance practices resulting from movement to new process materials that may be corrosive, caustic, environmentally impacting, molecularly incompatible etc. • Addressing factory integration challenges to assess and integrate EUV systems into the factory infrastructure • Addressing AMC challenges through possibly changing factory operation approach (e.g., maintaining vacuum in specific areas), as well as providing necessary interfaces, information and technologies (e.g., virtual metrology and APC).

Table 13 Factory Integration Difficult Challenges

Difficult Challenges through 2019	***Summary of Issues***
	• Maintaining equipment availability and productivity while managing increase in sensors and systems within and outside the equipment, coordinated to support new paradigms (e.g., management of energy expended by the equipment and the fab in general, movement from reactive to fully predictive) • Linking yield and throughput prediction into factory operation optimization • Real-time simulation in lock-step with production for operations prediction
3. Achieving growth targets while margins are declining	• Ability to visualize cost and cycle time for systematic waste reduction from all aspects. • Reducing complexity and waste across the supply chain; reducing white space in cycle times • Minimize the cost of new product ramp up against the high cost of mask sets and product piloting
4. Meeting factory and equipment reliability, capability and productivity requirements per the Roadmap	• Increased impacts that single points of failure have on a highly integrated and complex factory • More equipment reliability, capability and productivity visualization that can be used bidirectionally between equipment suppliers and users for more efficient task sharing • Design-in of equipment capability visualization in production equipment; design-in of APC (R2R control, FD, FC and SPC) to meet quality requirements • Equipment supplier roadmap for equipment quality visualization and improvement, and, reduction of Equipment Output Waste. • Reduction of equipment driven NPW (non-product wafers) operations that compete for resources with production wafers and Dandori operations[1] • Meeting wait-time waste factory level management targets; developing wait-time waste reporting for tools; supporting standardized fab-wide equipment state information management. • Moving from reactive to predictive paradigm for scheduling, maintenance and yield management
5. Emerging factory paradigm and next wafer size change	• Addressing issues in movement from lot-based to single-wafer processing and control • Uncertainty about 450 mm conversion timing and ability of 300 mm wafer factories to meet historic 30% cost effectiveness. • 450 mm era: Effecting architectural and other changes as necessary at an affordable cost to maintain or improve wafer-throughput-to-footprint levels in migration to 450 mm
Difficult Challenges Beyond 2019	***Summary of Issues***
1. Meeting the flexibility, extendibility, and scalability needs of a cost-effective, leading-edge factory	• Ability to utilize task sharing opportunities to keep the manufacturing profitable such as manufacturing outsourcing • Enhanced customer visibility for quality assurance of high reliability products including manufacturing outsourcing business models • Scalability implications to meet large 450 mm factory needs • Cost and task sharing scheme on industry standardization activity for industry infrastructure development
2. Managing ever increasing factory complexity	• Higher resolution and more complications in process control due to smaller process windows and tighter process targets in many modules • Complexity of integrating next generation lithography equipment into the factory • More comprehensive traceability of individual wafers to identify problems to specific process areas • Comprehensive management that allows for automated sharing and re-usages of complex engineering knowledge and contents such as process recipes, APC algorithms, FD and C criteria, equipment engineering best known methods
3. Increasing global restrictions on environmental issues	• Need to meet regulations in different geographical areas • Need to meet technology restrictions in some countries while still meeting business needs • Comprehending tighter ESH/Code requirements • Lead free and other chemical and materials restrictions • New material introduction
4. Post-conventional CMOS manufacturing uncertainty	• Uncertainty of novel device types replacing conventional CMOS and the impact of their manufacturing requirements on factory design • Timing uncertainty to identify new devices, create process technologies, and design factories in time for a low risk industry transition • Potential difficulty in maintaining an equivalent 0.7× transistor shrink per year for given die size and cost efficiency

Notes for Table 13

[1] Dandori operations: Peripheral equipment related operations that are in parallel or in-line and prior to or following to the main thread PE operations. So-called in-situ chamber cleaning is another good example than NPW operations.

ASSEMBLY AND PACKAGING

While Moore's Law continues to move forward scaling in feature size to deep submicron nodes, the performance, power, bandwidth, and cost are no longer scaling at the same rate. New materials and new device types will be necessary to address this shortfall. Advances in assembly and packaging technology have helped take up the slack with new package types with improved functional density enabled by new packaging materials and processes. The packaging community has introduced wafer-level packaging, new generations of flip chip "chip-size" packages (CSPs), various forms of system-in-package (SiP) including 3D stacked die and stacked packages, fine pitch surface mount, silicon and glass interposers (2.5D) and 3D IC. SiP architecture is the enabling technology for "More than Moore" equivalent scaling through functional diversification and heterogeneous integration. This allows many different types of electronic, optical and electro-mechanical components to be integrated into a single package. New package architectures such as package-on-package (PoP) and package-in-package (PiP), already in volume production, are examples of early SiP technology.
Despite these innovations, packaging has not scaled at the same pace as integrated circuits. As a result, packaging is currently a gating issue in the drive for expanded functionality at higher performance that is lower cost and in a smaller and thinner form factor.

DIFFICULT CHALLENGES

There are many difficult challenges associated with continued cost reduction, size reduction, improved performance, and improved power efficiency for all types of packages. In addition, the number of device types is expanding with heterogeneous integration, photonics, photovoltaics, and MEMS devices. New package architectures such as advanced wafer-level packaging, complex SiP and 3D-TSV based SiP integration are emerging to address rapidly evolving market needs. These challenges have spawned an increasing number of consortia where the cost of research is shared. The result has been an acceleration of progress in an environment where individual participants in the industry have less resource allocated to research. The annual list of difficult challenges for assembly and packaging provides some focus to cooperative efforts to meet these challenges before they become roadblocks to continued progress. This list for 2012 is presented below.

Table 14 Assembly and Packaging Difficult Challenges

Difficult Challenges ≥16 nm	***Summary of Issues***
Impact of BEOL including Cu/low κ on packaging	Direct wire bond and bump to Cu for very fine pitch due to thin wire limits
	Dicing for ultra low κ dielectric (Includes κ < 2.5eff and air gaps)
	Improved fracture toughness of dielectrics
	Interfacial adhesion
	Mechanical reliability for chip-package interconnect (requires co-design due to chip-package interaction)
	Methodologies for measurement of critical properties needed.
	Probe damage for copper/ultra low κ
Wafer-level packaging	I/O pitch for small die with high pin count
	Solder joint reliability for tight pitch-low stand-off interconnect
	Compact ESD structures
	CTE mismatch compensation for large die and fan-out die

Table 14 Assembly and Packaging Difficult Challenges

Difficult Challenges ≥16 nm	***Summary of Issues***
Coordinated design tools and simulators to address chip, package, and substrate co-design	Mix signal co-design and simulation environment
	Rapid turnaround modeling and simulation
	Integrated analysis tools for transient thermal analysis and integrated thermal mechanical analysis
	Electrical (power disturbs, EMI, signal and power integrity associated with higher frequency/current and lower voltage switching)
	System level co-design is needed now
	EDA for "native" area array is required to meet the Roadmap projections
	Models for reliability prediction
Interposers and embedded components	CTE mismatch and warpage for large interposers
	Defect density at very thin interfaces
	Low cost embedded passives: R, L, C
	Embedded active devices
	Quality levels required not attainable on chip
	Electrical and optical interface integration
	Wafer level embedded components
Thinned die packaging	Handling technologies for thinned die and wafers (particularly for bumped wafers)
	Impact of different carrier materials (organics, silicon, ceramics, glass, laminate core)
	Establish new process flows
	Reliability
	Testability
Difficult Challenges ≤16 nm	***Summary of Issues***
Package cost does not follow the die cost reduction curve	Margin in packaging is inadequate to support investment required to reduce cost
	Wafer level packaging and 3D equipment cost is not scaling with product cost
	Increased device complexity requires higher cost packaging solutions
Small die with high pad count and/or high power density	Electromigration at high current density for interconnect (die, package)
	Thermal dissipation
	Improved current density capabilities
	Higher operating temperature
High frequency die	Substrate wiring density to support >20 lines/mm
	Lower loss dielectrics
	"Hot spot" thermal management
	Package substrates with lines and spaces below 10 microns
System-level design capability to integrate chips, passives, substrates, and 3D Structures	Partitioning of system designs and manufacturing across numerous companies will make required optimization for performance, reliability, and cost of complex systems very difficult.
	Complex standards for information types and management of information quality along with a structure for moving this information will be required.
Emerging device types (organic, nanostructures, biological) that require new packaging technologies	Organic device packaging requirements not yet defined (will chips grow their own packages)
	Biological interfaces will require new interface types
Power integrity	Power supply quality
	Power delivery in stacked die
	Reducing power supply voltage with high device switching currents

ENVIRONMENT, SAFETY, AND HEALTH

The 2012 ESH section of the overall roadmap reflects the major changes that were begun in the 2011 roadmap, where many of the tactical short term requirement elements previously present were de-emphasized, with a renewed focus on the overall long range strategic direction for the semiconductor industry. Recognizing the significant directional change that 2011 represented, the current roadmap bears a close resemblance to its predecessor being a minor edit year, and is essentially transitional as we prepare for the major re-write of the roadmap in 2013. Looking forward then, we will be emphasizing the critical importance of leveraging the roadmap to drive proactive, integratives and technical solutions to address many future ESH challenges.

Nevertheless, the core principles of successful ESH program execution remain largely independent of the specific technology thrust advances to which they are applied. This also means that many of the ESH roadmap elements, such as the difficult challenges and the technology requirements, are very similar to those in previous roadmap editions. Therefore, the fundamental ESH roadmap strategies we have historically employed to guide our approach in developing our long range vision has not changed:

- Understand (characterize) processes and materials during the development phase
- Use materials that are less hazardous or whose byproducts are less hazardous
- Design products and systems (equipment and facilities) that consume less raw material and resources
- Continue to ensure that factories are safe for employees and the surrounding communities

In 2011, to better address our key challenges of defining research needs, determine technology requirements, and to mitigate future regulatory and compliance restrictions, we added a new strategic element to our core strategies listed above. This new strategy included integration of the principles of "Green Chemistry" into the overall ITRS Roadmap. The objective of this approach was to create a framework and process for the industry, aligning with a concept that has been gaining acceptance in government, academia and other industries (such as pharmaceutical and chemical). In fact, adoption of green/sustainable chemistry concepts naturally builds on the well-established business processes for ESH developed in the semiconductor industry over many decades, enabling us to drive consistency and alignment and to proactively address the growing complexity of regulations, restriction and global compliance requirements. For the roadmap, this means that EHS materials issues are addressed at the outset of the technology life cycle (in the chemical and process design phase).

By applying and building on these strategies as essential elements to success, the industry continues to be an ESH as well as a technology leader. For many years, the semiconductor industry has adopted a business approach, where key ESH principles are integrated into research and development, manufacturing technologies, products, and services.

However, the unique challenge that we have faced since the early days of the Roadmap in the ESH section, namely how to comprehend and address various policy and regulatory issues, has not changed. As previously stated, any failure to do so could jeopardize the implementation of successfully developed technologies. Our first step towards addressing this was in the 2009 Roadmap, by the introduction of ESH categories and domains. This concept was extended in 2011, by the introduction of two new subcategories ("requirements have data", or "no data available") to reflect the availability of roadmap quality goals and metrics to address the ESH goals presented. Now moving forward, we are using the concept of the aforementioned green/sustainable chemistry to establish a consistent and forward looking framework to address ESH issues.

This does not diminish our foundational activity of comprehending the state of the global regulatory environment, but going forward, this characterization of the current landscape serves as a basis for projecting out key trends as we identify future ESH challenges for the roadmap.

The ESH Roadmap will continue to identify challenges when new wafer processing and assembly technologies move through research and development phases, and towards manufacturing insertion. Following the presentation of ESH Domains and Categories (including the Subcategories) in Table ESH2, ESH technology requirements are listed in Tables ESH3–7. Potential technology and management solutions to meet these challenges are proposed in Figures ESH1–3, and are essentially unchanged, from 2011. As we have stated previously, effective resolution of these future challenges will only be fully realized when ESH concerns are integral to the technology design process, where we have the most impact and lower cost to effect change; hence our focus on green/sustainable chemistry (and engineering). That said, we have expanded our ESH ITWG membership to include all key stakeholders (process, equipment, and facilities engineers; chemical/material and tool suppliers; and academic and consortia researchers), in the road mapping process. This will enable ESH improvements to contribute to (or at minimum, not conflict with) enhanced cost, technical performance, and

product timing. Roadmap requirements must inherently minimize risk, public and employee health and safety effects, and environmental impact. Successful global ESH initiatives must be timely, yet far reaching, to ensure long-term success over the Roadmap's life, improving efficient use of industry resources and ensuring effective decision making.

The ESH Roadmap domains remain essentially the same as they were in 2011 (shown in the table below: Table 15), which serve to unify ESH elements for the full requirement set. However, the tables themselves remain in their simplified state relative to previous years due to the radical changes made in 2011. Even as we move toward a major re-write of the tables in 2013, we will continue employing these domain categories:

- *Restricted Chemicals:* By nature, this domain highlights chemicals which fall into the critical category
- *New Chemicals:* There are a variety of emerging chemicals and materials, the exact specifications and ESH properties of which are not always fully established when they enter into new process consideration.
- *Nanotechnology:* While formally only a subset of new chemicals, there can be unique ESH considerations for nanometer-scale chemicals and materials, which merit their separation into their own domain.
- *Utilization/Waste Reduction*: The fundamental ESH strategies noted in the opening paragraph all have a prominent role in this domain.
- *Energy:* Given the increasing attention to greenhouse gas control, carbon footprint, and related energy-control metrics, this area stands out as one deserving deeper attention at the domain level.
- *Green Fab:* This is a broad—and at present not-well-defined or universally agreed-upon—term meant to represent fab operations conducted with minimal ESH impact (and the process and economic benefits which may derive from such practices). This domain includes sustainability issues, as well as the full life-cycle considerations for chemicals/materials, tools and processes, the full fab infrastructure, and the products derived from them. The lessons we learn, from developing integrated solutions at the fab level, will be crucial to proactively address ESH challenges, that may be not be soluble at the operational, case by case basis.

We will continue to emphasize the critical importance of defining research needs that ensure alignment of public/government policy expectations with future technology needs, where critical materials are needed or new materials required to assure future technology. Emphasizing the distinction between green and sustainable chemistries will be a key role for the roadmap. So while the long term ideal goal will be to strive for completely "green" materials, we will nonetheless address ESH issues at the earliest possible time, to develop sustainable materials and highlight the technical advantages that these new materials provide. Determining how to specify technology requirements for non-quantifiable or non-data supported requirements (i.e., where no meaningful information exists) are not representative of the overall industry or there is insufficient data for defining a technical objective, is nonetheless important for ESH, to at least provide a path toward obtaining data. This is where our role of defining the key characteristics of alternative assessment tools will be critical in developing predictive tools for materials selections.

Looking ahead to 2013 and beyond, the ESH ITWG Team recognizes that the roadmap will undergo significant changes going forward, as we strive to focus on a more strategic, long term focus that emphasizes the critical importance of employing novel technology solutions to ESH challenges, to support and enable the advancement of future industry technology developments. This certainly applies to the 450 mm transition, which represents a clear opportunity for driving ESH technology improvements. As this transition will touch many parts of the overall roadmap, we did not deem it appropriate to create a separate domain for this.

DIFFICULT CHALLENGES

Table 15 Environment, Safety, and Health Difficult Challenges

Difficult Challenges ≥ 16 nm	***Summary of Issues***
Overall challenge	There is a need for Roadmap quality goals and metrics to be defined for a substantial number of ESH technology requirements.
Chemicals and materials management	• *Chemical Assessment:* There is a need for robust and rapid assessment methodologies to ensure that new chemicals/materials achieve timely insertion in manufacturing, while protecting human health, safety, and the environment. Given the global options for R&D, pre-manufacturing, and full commercialization, these methodologies must recognize regional regulatory/policy differences, and the overall trends towards lower exposure limits and increased monitoring. • *Chemical Data Availability:* Comprehensive ESH data for many new, proprietary chemicals/materials are incomplete, hampering industry response to the increasing regulatory/policy requirements on their use. In addition, methods for anticipating and forecasting such future regulatory requirements are not well developed. • *Chemical Exposure Management:* There is incomplete information on how chemicals/materials are used and how process by-products are formed. Also, while methods used to obtain such information are becoming more standardized, their availability varies depending on the specific issue being addressed.
Process and equipment management	• *Process Chemical Optimization:* There is a need to develop processes and equipment which meet technology requirements, while at the same time reduce their impact on human health, safety and the environment (e.g., use more benign materials, reduce chemical quantity requirements by more efficient and cost-effective process management). • *Environment Management:* There is a need to understand ESH characteristics, and to develop effective management systems, for process emissions and by-products. In this way, the appropriate mitigations (including the capability for component isolation in waste streams) for such hazardous and non-hazardous emissions and by-products can be properly addressed. • *Global Warming Emissions Reduction:* There is a need to limit emissions of high GWP chemicals from processes which use them, and/or produce them as by-products. • *Water and Energy Conservation:* There is a need for innovative energy- and water-efficient processes and equipment. • *Consumables Optimization:* There is a need for more efficient chemical/material utilization, with improved reuse/recycling/reclaiming of process emissions and by-products. • *By-products Management:* There is a need for improved metrology for by-product speciation. • *Chemical Exposure Management:* There is a need to design-out chemical exposure potentials and the requirements for personal protective equipment (PPE). • *Design for Maintenance:* There is a need to design equipment so that commonly serviced components and consumable items can be easily and safely accessed; with maintenance and servicing safely performed by a single person with minimal health and safety risks. • *Equipment End-of-Life:* There is a need to develop effective management systems to address issues related to equipment end-of-life reuse/recycle/reclaim.
Facilities technology requirements	• *Conservation:* There is a need to reduce energy, water and other utilities consumption and for more efficient thermal management of cleanrooms and facilities systems. • *Global Warming Emissions Reduction:* There is a need to design energy efficient manufacturing facilities, to reduce total CO_2 equivalent emissions.
Sustainability and product stewardship	• *Sustainability Metrics:* There is a need for methodologies to define and measure a technology generation's sustainability. • *Design for ESH:* There is a need to make ESH a design-stage parameter for new facilities, equipment, processes and products. • *End-of-Life Reuse/Recycle/Reclaim:* There is a need to design facilities, equipment and products to facilitate these end-of-life issues.

Table 15 Environment, Safety, and Health Difficult Challenges

Difficult Challenges < 16 nm	***Summary of Issues***
Chemicals and materials management	• *Chemical Assessment:* There is a need for robust and rapid assessment methodologies to ensure that new chemicals/materials achieve timely insertion in manufacturing, while protecting human health, safety, and the environment. • *Chemical Data Availability:* There is incomplete comprehensive ESH data for many new, proprietary chemicals/materials, to be able to respond to the increasing regulatory/policy requirements on their use.
Process and equipment management	• *Chemical Reduction:* There is a need to develop processes and equipment meeting technology requirements, while also reducing their impact on human health, safety and the environment (e.g., using more benign materials, reducing chemical quantity requirements by more efficient and cost-effective process management). There is a need to limit emissions of high GWP chemicals from processes which use them, and/or produce them as by-products. • *Environment Management:* There is a need to understand ESH characteristics, and to develop effective management systems, for process emissions and by-products. In this way, the appropriate mitigations for such hazardous and non-hazardous emissions and by-products can be addressed. • *Water and Energy Conservation:* There is a need to reduce water and energy consumption, and for innovative energy- and water-efficient processes and equipment. • *Consumables Optimization:* There is a need for more efficient chemical/material utilization, including their increased reuse/recycle/reclaim of process emissions and by-products. • *Chemical Exposure Management:* There is a need to design-out chemical exposure potentials and personal protective equipment (PPE) requirements. • *Design for Maintenance:* There is a need to design equipment so that commonly serviced components and consumable items can be easily and safely accessed; with maintenance and servicing safely performed by a single person with minimal health and safety risks. • *Equipment End-of-Life:* There is a need to develop effective management systems to address issues related to equipment reuse/recycle/reclaim.
Facilities technology requirements	• *Conservation:* There is a need to reduce energy, water and other utilities use, and for more efficient thermal management of cleanrooms and facilities systems. • *Global Warming Emissions Reduction:* There is a need to design energy efficient manufacturing facilities, to enable reducing total CO_2 equivalent emissions.
Sustainability and product stewardship	• *Sustainability Metrics:* There is a need for methodologies to define and measure sustainability by technology generation, as well as at the factory infrastructure level. • *Design for ESH:* There is a need to make ESH a design-stage parameter for new facilities, equipment, processes and products, with methodologies to holistically evaluate and quantify the ESH impacts of facilities operations, processes, chemicals/materials, consumables, and process equipment for the total manufacturing flow. • *End-of-Life Reuse/Recycle/Reclaim:* There is a need to design facilities, equipment and products to facilitate these end-of-life issues.

YIELD ENHANCEMENT

According to the reorientation of the scope of the chapter that was introduced by the 2011 roadmap edition, the Yield Enhancement Chapter currently consists of the two subchapters "Wafer Environment and Contamination Control" (WECC) and "Characterization, Inspection and Analysis" (CIA). Activities in Yield Enhancement thus were focused on these two aspects.

The key challenges, according to table YE2, in principle remain unchanged. However, there is an adaption of wording in some cases in order to improve clarity. The most important key challenge on near term scale for dimensions above 16 nm is estimated to be the detection of small yield limiting defects and their identification from nuisance. It is a challenge to detect multiple killer defect types and to differentiate them simultaneously at high capture rates, low cost of ownership and high throughput. Furthermore, it is a dare to identify yield relevant defects under a vast amount of nuisance and false defects. A challenge with second priority still is process stability versus absolute contamination level. This includes the correlation to yield test structures, methods, and data that are needed for correlating defects caused by wafer environment and handling to yield. This requires determination of control limits for gases, chemicals, air, precursors, ultrapure water and substrate surface cleanliness. The challenge of detection of organic contamination on surfaces, which was added as key challenge with lower priority in 2011, persists further on. The detection and speciation of nonvolatile organics on surfaces is currently not possible in the fab. There is no laboratory scale instrumentation available.

Next generation inspection still is assessed to be the first key challenge in the long term, i.e., for dimensions below 16 nm. As bright field detection in the far-field loses its ability to discriminate defects of interest, it has become necessary to explore new alternative technologies that can meet inspection requirements beyond 13 nm node. Several techniques should be given consideration as potential candidates for inspection: high speed scanning probe microscopy, near-field scanning optical microscopy, interferometry, scanning capacitance microscopy and e-beam inspection. This assessment should include each technique's ultimate resolution, throughput and potential interactions with samples (contamination, or degree of mechanical damage) as key success criteria. In addition, in-line defect characterization and analysis as well as next generation lithography remain key challenges on long term scale.

As recently, major attention of the community has been rivet on activities in WECC, which continues providing contamination control limits for media as ultra pure water (UPW), pure gases and air in clean rooms and clean compartments. Control limits have been reviewed with respect to their known yield impact in critical process steps (cf. table YE3).

WECC activities were specifically focused on "Airborne Molecular Contamination" (AMC) in enclosed wafer environments as FOUPs. The description and assessment of solutions improving the contamination situation in FOUPs has been fostered, thus resulting in the introduction of the new tables YE4 'AMC Monitoring methods' and YE4a 'Supporting table for on-line methods.' In particular YE4 reveals relevant analytical procedures, which are capable of monitoring the adherence of the technology requirements listed by table YE3. By doing so, a comparison of online versus offline analytical methods is given as well as method limitations and respective detection limits. The table moreover newly incorporates FOUP environment sampling. In accordance with the high degree of attention, which is drawn at the AMC activities, review for an "AMC definition" is one scope of future work. Activities will moreover focus on review of "potential solutions" and adjustment of AMC limits. However, since means of production as reticles and new manufacturing technologies and the respective effects of contamination gain increasing importance within WECC, activities moreover will concentrate on the introduction of extreme ultraviolet (EUV) related contamination and of moisture as a new chemical contamination for the description of the reticle environment. In this context critical steps for moisture control in FOUP environment will be identified as well. Further aspect of future work will be the definition and standardization of "organics." Moreover, discussions about adding bare wafer suppliers requirements will be continued.

Regarding UPW, ions and metals still are considered as critical with the result that there is no change in the roadmap in this respect. Taken as a whole, electrically active particles are reckoned as more critical than electrically inactive particles. However, since on-line metrology for particles in liquid currently does not address killer particle size, increase of knowledge of filtration efficiency for killer particles is targeted at present. A standard for the filter performance validation therefore is going to be developed in collaboration with SEMI. Particles' control as a whole is supposed to gain even more importance with relation to next generation lithography (NGL) technologies, which have stricter requirements concerning particles' control, e.g., for EUV mask cleaning and nano-imprint. Evaluation of respective contamination effects and recommendation of limit values is within the scope of the period 2012/2013. Review of the definition of critical organics based on front-end processing (FEP) input is also aimed at. A new and better definition of critical organics at this is aspired to make use of failure mode and effects analysis (FMEA).

Facing the demands of broad applications as, e.g., More Moore (MM) and More than Moore (MtM) technologies was defined as the scope of CIA in 2011. In this respect also power electronics, mechatronics and MEMS applications as well as characterization, inspection and analysis demands and requirements of packaging and assembly have been taken into account. This, in comparison to previous years, major change of the scope was decided and confirmed in the meetings of 2010/2011/2012. Accordant tables and potential solutions covering this scope will be prepared for the revision in 2013. In addition, a further extension of the mentioned scope towards a better balance of defect/contamination detection and fault diagnostics/control of electrical defects is still under discussion. That means, it is a current subject for debate, whether referring to not only physical and process defects but also to device defects and abnormal electrical characteristics of a device provides some benefit for yield enhancement with respect to proceeding shrinking of devices and a lack of accordant measurement capacity. Acquisitions of electrical characteristics of devices and determination of pass or fail characteristics of chips probably involve advantages in time and in measuring possibility. Extending the CIA activities in this regard also seems to be a corollary of the advent of MtM and 450 mm technology and the inclusion of back end yield into the CIA focus. Including a statistical/systematic approach into yield enhancement activities is one major point of discussion in this respect. Another one is the introduction of tables and requirements concerning yield enhancement on device, chip and system level into the ITRS 2013 edition.

In conclusion, improvement of the Yield Enhancement chapter prospectively focuses on the adjustment of the outline and the content of the chapter in order to correctly reflect the current status and the future requirements especially with respect to yield enhancement for manufacturing of MM, MtM, larger diameter substrates and masks. Keeping tables for front end processing updated, adding back end yield enhancement specifications, and considering assembly and packaging yield enhancement will be done in practice.

The specific revisions to the subchapter were:

- Wafer Environment and Contamination Control
  - Line item 19 (Refractory compounds in lithography zone; POE) of table YE3 was revised.
  - Two new tables YE4 “AMC Monitoring Methods” and YE4a “Supporting table for on-line methods” are introduced within the subchapter wafer environmental control and airborne molecular contamination. In this regard, the text was also revised by including some explanation for the introduction of the tables and some corrections.
- Characterization, Inspection and Analysis (CIA)
  - A review was performed for the tables YE4, YE5 and YE6, which are now named as YE5, YE6 and YE7, with regard to current technology specific critical dimensions. This review did not reveal any changes compared to the 2011 edition of the ITRS roadmap.

WAFER ENVIRONMENTAL CONTAMINATION CONTROL

Wafer environmental contamination control requirements are categorized by manufacturing materials or environment, as shown in Table YE3.

WAFER ENVIRONMENT CONTROL

The wafer environment control considers the ambient space around the wafer at all times, whether the wafers are open to the cleanroom air or stored in PODs/FOUPs. As the list of ambient contaminants to be controlled broadens, measurement capabilities have to adapt. Affordable, accurate, repeatable, real time sensors for non-particulate contamination are becoming increasingly desirable. The use of inert environments to transport and store wafers is expected to increase with process sensitivities. Pre-gate, pre-contact clean, salicidation, exposed copper, and reticle exposure are cited as processes that first require this capability. In addition, using inert environments offers the opportunity to reduce the introduction of moisture into vacuum load-lock tools, thereby decreasing contamination and load-lock pump-down times. While closed carrier purging systems exist and are evolving, tool environments that may need to become inert, such as wet sink end-stations, present a challenge. As wafer isolation technologies evolve, design and material selection of carriers and enclosures will be critical for performance in isolating the wafers from the ambient and in not contributing contaminants themselves. In addition, the materials and designs must not promote cross-contamination between processes. Seal technology, low-outgassing, and non-absorbing materials development are key to effective wafer and reticle isolation deployment.

AIRBORNE MOLECULAR CONTAMINATION

Outgassing from materials of construction in the cleanroom, wafer processing equipment, post processed wafers, and wafer environmental enclosures as well as inadequate exhaust and fugitive emissions from chemicals used in wafer processing are the main sources of AMC. Makeup air can also be a significant source for AMC, depending on outside ambient air conditions. Oxygen and water vapor as well as other atmospheric contaminants (e.g., CO, O_3, NO_X, organics) can also be considered as part of the AMC burden. Acid vapors in the air have been linked to corrosion, as well as with the release of boron (a dopant) from HEPA filters. The impact of amines on deep ultraviolet (DUV) photoresists are well known examples of AMC affecting wafer processing, recently also spreading to acids for negative resists. Hydrocarbon films of only a few mono layers may lead to loss of process control, especially for front-end processes and also may cause deposits on optical systems.

The impact of AMC on wafer processing can only be expected to become more important. This is not only driven by device dimensions but also by the introduction of new chemistry and recipes for future technology nodes with yet unknown defect schemes. Besides AMC creating defects on wafer surfaces or bulk materials, the Yield Enhancement group engages on defects or shortfalls in productivity that originate from the impact of AMC to production tools such as reticles, metrology or exposure tools. AMC is in many cases a highly dynamic phenomenon. AMC control deals mainly with prevention of AMC release for which a tight source control is mandatory. There is clearly a need for better AMC monitoring instrumentation in the clean room and other wafer environments to measure AMC at the part per trillion level (by volume) in real time.

INTRODUCTION OF NEW TABLE: YE4 "AMC MONITORING METHODS"

In 2012 WECC workgroup assessed the AMC monitoring methods and instruments to give a state-of-the art update and near future perspective on that subject. The results are consolidated in Table YE4 with a supporting table YE4a for on-line methods. The information on AMC monitoring methods has been aligned to the structure of YE3 Technological Requirements for Wafer Environmental Control. With this alignment a direct link from contamination control limits (YE3) to suitable technologies to monitor to the limits (YE4) is given. WECC workgroup will revisit the information on every two years and update to state-of-the art.

Numerous studies related to AMC outgassing from the materials of construction of environmental enclosures and FOUPs have been performed to guide material selection for these enclosures. Beyond proper material choice the need for pumping and nitrogen purging of wafer environment enclosures is further investigated for critical process steps to diminish cross-over of contamination from different process steps by FOUPs. The potential for AMC to impact new processes should be considered in all process integration studies.

This is specifically true where disruptive, revolutionary techniques are introduced into the manufacturing chain. For example, future lithography systems require vacuum processing and are not expected to impose new AMC control requirements in the clean room environment. However new challenge compounds are identified for the tool interior that may require novel air and purge gas treatments.

A detailed definition of critical impurities is provided in *AMC definitions*.

Temperature and humidity specifications have been added to Table YE3 this year for the most critical applications, e.g., lithography for several reasons:

1) The strictest requirements are driven by the lithography process, which is protected by an environmental chamber. The specifications in the Table YE3 reflect the inlet condition to each individual environmental chamber. Here especially, the maximum variation over time is important, which the environmental chamber must be able to compensate. At the POP lower specifications down to ± 0.03˚K are maintained.

2) But also in the coater/developer track temperature and humidity specifications must be guaranteed to maintain stable conditions for the resist.

3) The temperature variation is also important for the stepper itself, since minor temperature variations can result due to different thermal extension coefficients in misalignments between the stepper foundation/wafer stage and the lens column. Steppers need up to a week to stabilize after a temperature change.

4) Another critical requirement is driven by metrology equipment which depend either on laser beams (the air density depend on temperature and humidity) and by measurements where misalignments are important.

The temperature and humidity stability over different locations within critical areas is less important. Also in other areas temperature and humidity variations shall be controlled to less strict limits since it may have an impact on the surface (native oxide formation) or alignments. Some companies choose not to have different specifications for critical and non-critical areas to allow flexibility in the cleanroom use as well as simplify the temperature and humidity control and the associated segregation.

These specifications are variational specifications and set points can be chosen in a wide range. A recent benchmarking study between fabs has shown values between 19.5 and 24°C for temperature and values between 35% and 48% for the relative humidity. There are different drivers for that. The temperature set point is normally chosen based on comfort level and climatic conditions and the resulting energy consumption. The set point for relative humidity takes into consideration higher electrostatic charges at lower humidity and higher corrosion/native oxide formation at higher relative humidity. Capacity of AMC filters also depends on the humidity.

Another process area with temperature/humidity control as well as AMC control requirements is the location of the lithography excimer lasers, if they are installed in the subfab and not in the main cleanroom.

TABLE YE3

Table YE3 is taking into account the immediate wafer and masks environment and enclosures (FOUPs, reticle Pods). The revision aligns the table structure and content with actual manufacturing concepts involving clean room control, high purity storage environments as (bare) wafer and mask stockers and enclosures. Each process segment listed is split into information that is referring to the clean room ambient conditions and limits that are referring to the interior environment and atmosphere of FOUPs, reticle Pods or bare material storage environment. Clean room ambient conditions are regarded as POE conditions to critical process steps that may involve further tool related measures of AMC protection and reduction, yet require controlled entry conditions to achieve proper process control. FOUP and reticle Pods interior limits are not only influenced by clean room environmental contamination but are depending heavily on remaining active material outgassing or re-evaporation of AMC attached to the containment walls.

New Text: In 2012 WECC workgroup checked the limits and contents of table YE3 yet without the need for revisions.

The revision of line 19 (Refractory compounds in lithography zone, POE) could be closed. Footnote [44] relates the limit value of 100 pptv to boundary conditions of preventive tool maintenance.

Table 16 Yield Enhancement Difficult Challenges

Difficult Challenges ≥ 16 nm	***Summary of Issues***
It is a challenge to detect multiple killer defect types and to differentiate them simultaneously at high capture rates, low cost of ownership and high throughput. Furthermore, it is a dare to identify yield relevant defects under a vast amount of nuisance and false defects.	• Existing techniques trade-off throughput for sensitivity, but at expected defect levels, both throughput and sensitivity are necessary for statistical validity. • Reduction of inspection costs and increase of throughput is crucial in view of CoO. • Detection of line roughness due to process variation. • Electrical and physical failure analysis for killer defects at high capture rate, high throughput and high precision. • Reduction of background noise from detection units and samples to improve the sensitivity of systems. • Improvement of signal to noise ratio to delineate defect from process variation. • Where does process variation stop and defect start?

Table 16 Yield Enhancement Difficult Challenges

Difficult Challenges ≥ 16 nm	***Summary of Issues***
Process Stability vs. Absolute Contamination Level – This includes the correlation to yield test structures, methods and data that are needed for correlating defects caused by wafer environment and handling to yield. This requires determination of control limits for gases, chemicals, air, precursors, ultrapure water and substrate surface cleanliness.	• Systematic Mechanisms Limited Yield (SMLY), resulting from unrecognized models hidden in the chip, should be efficiently identified and tackled through logic diagnosis capability designed into products and systematically incorporated in the test flow. It is required to manage the above models at both the design and the manufacturing stage. Potential issues can arise due to: a) Accommodation of different Automatic Test Pattern Generation (ATPG) flows. b) Automatic Test Equipment (ATE) architecture which might lead to significant test time increase when logging the numbers of vectors necessary for the logic diagnosis to converge. c) Logic diagnosis runs time per die. d) Statistical methodology to analyze results of logic diagnosis for denoising influence of random defects and building a layout-dependent systematic yield model. • Test pattern generation has to take into account process versus layout marginalities (hotspots) which might cause systematic loss, and has to improve their coverage. • Methodology for employment and correlation of fluid/gas types to yield of a standard test structure/product. • Relative importance of different contaminants to wafer yield. • Define a standard test for yield/parametric effect. • A possible work around is the use of NEXAF at a synchrotron radiation facility.
Difficult Challenges < 16 nm	***Summary of Issues***
Next Generation Inspection – As bright field detection in the far-field loses its ability to discriminate defects of interest, it has become necessary to explore new alternative technologies that can meet inspection requirements beyond 13 nm node. Several techniques should be given consideration as potential candidates for inspection: high speed scanning probe microscopy, near-field scanning optical microscopy, interferometry, scanning capacitance microscopy and e-beam. This assessment should include each technique's ultimate resolution, throughput and potential interactions with samples (contamination, or degree of mechanical damage) as key success criteria.	• Several techniques should be given consideration as potential candidates for inspection: high speed scanning probe microscopy, near-field scanning optical microscopy, interferometry, scanning capacitance microscopy and e-beam. This path finding exercise needs to assess each technique's ultimate resolution, throughput and potential interactions with samples (contamination, or degree of mechanical damage) as key success criteria.
In-line Defect Characterization and Analysis – Based on the need to work on smaller defect sizes and feature characterization, alternatives to optical systems and Energy Dispersive X-ray Spectroscopy systems are required for high throughput in-line characterization and analysis for defects smaller than feature sizes. The data volume to be analyzed is drastically increasing, therefore demanding for new methods for data interpretation and to ensure quality. [1]	• Data volume + quality: strong increase of data volume due to miniaturization • The probe for sampling should show minimum impact as surface damage or destruction from SEM image resolution. • It will be recommended to supply information on chemical state and bonding especially of organics. • Small volume technique adapted to the scales of technology generations. • Capability to distinguish between the particle and the substrate signal.
Next generation lithography – Manufacturing faces several choices of lithography technologies in the long term, which all pose different challenges with regard to yield enhancement, defect and contamination control.	

Note for table

[1] Cross-link to metrology chapter

METROLOGY

Metrology requirements continue to be driven by advanced lithography processes, new materials, and beyond CMOS materials, structures, and devices. The push for EUV Lithography is driving the development of new metrology equipment for masks. Existing Critical Dimension metrology is approaching its limits and requires significant advances to keep pace with the needs of patterning.

There is a new emphasis on directed self assembly which utilized block co-polymer materials which require CD metrology. Another key challenge to critical dimension metrology is tool matching. Near term precision (measurement uncertainty) requirements for the next few years can be met using single tools. Overlay metrology capability lags behind the need for improved overlay control. Front end processes continue to drive metrology to provide measurements for new channel materials including III-V film stacks, higher dielectric constant materials, dual work function metal gates, and new ultra shallow junction doping processes. 3D device structures such as FinFETs place significantly more difficult requirements on dimensional and doping metrology. The need for porosity control for low k materials has driven a renewed interest in porosity measurements. 3D interconnect metrology requirements are largely driven by the activity in through silicon vias (TSV) R&D. Bonded wafer overlay control for next generation. Potential solutions for bonded wafer overlay are now available. For Beyond CMOS R&D, many areas of graphene metrology have advanced but putting them into volume manufacturing will require challenging R&D.

A key metrology challenge is electrical measurements for nanoscale structures and devices especially junction characterization. In addition, metrology R&D is working with other Beyond CMOS materials.

DIFFICULT CHALLENGES

Many short-term metrology challenges listed below will continue beyond the 16 nm ½ pitch Metrology needs after 2019 will be affected by unknown new materials and processes. Thus, it is difficult to identify all future metrology needs. Shrinking feature sizes, tighter control of device electrical parameters, such as threshold voltage and leakage current, and new interconnect technology such as 3D interconnect will provide the main challenges for physical metrology methods. To achieve desired device scaling, metrology tools must be capable of measurement of properties on atomic distances. Table 17 presents the ten major challenges for metrology.

Table 17 Metrology Difficult Challenges

Difficult Challenges ≥ 16 nm	***Summary of Issues***
Factory level and companywide metrology integration for real-time *in situ*, integrated, and inline metrology tools; continued development of robust sensors and process controllers; and data management that allows integration of add-on sensors.	Standards for process controllers and data management must be agreed upon. Conversion of massive quantities of raw data to information useful for enhancing the yield of a semiconductor manufacturing process. Better sensors must be developed for trench etch end point, and ion species/energy/dosage (current).
Starting materials metrology and manufacturing metrology are impacted by the introduction of new substrates such as SOI. Impurity detection (especially particles) at levels of interest for starting materials and reduced edge exclusion for metrology tools. CD, film thickness, and defect detection are impacted by thin SOI optical properties and charging by electron and ion beams.	Existing capabilities will not meet Roadmap specifications. Very small particles must be detected and properly sized. Capability for SOI wafers needs enhancement. Challenges come from the extra optical reflection in SOI and the surface quality.
Control of new process technology such as Directed Self Assembly Lithography, complicated 3D structures such as FinFET and MuGFET transistors, capacitors and contacts for memory, and 3D Interconnect are not ready for their rapid introduction.	Although there have been significant advances in off-line characterization of FinFET structures, the recent announcement that a FinFET transistor will be used in manufacturing at the 16 nm 1/2 pitch has placed renewed emphasis on the near term need for in-line metrology for dimensional, compositional, and doping measurements. The materials properties of block co-polymers result in new challenges for lithography metrology. 3D Interconnect comprises a number of different approaches. New process control needs are not yet established. For example, 3D (CD and depth) measurements will be required for trench structures including capacitors, devices, and contacts.

Table 17 Metrology Difficult Challenges

Difficult Challenges ≥ 16 nm	***Summary of Issues***
Measurement of complex material stacks and interfacial properties including physical and electrical properties.	Reference materials and standard measurement methodology for new high-κ gate and capacitor dielectrics with engineered thin films and interface layers as well as interconnect barrier and low-κ dielectric layers, and other process needs. Optical measurement of gate and capacitor dielectric averages over too large an area and needs to characterize interfacial layers. Carrier mobility characterization will be needed for stacks with strained silicon and SOI substrates, or for measurement of barrier layers. Metal gate work function characterization is another pressing need.
Measurement test structures and reference materials.	The area available for test structures is being reduced especially in the scribe lines. Measurements on test structures located in scribe lines may not correlate with in-die performance. Overlay and other test structures are sensitive to process variation, and test structure design must be improved to ensure correlation between measurements in the scribe line and on chip properties. Standards institutions need rapid access to state of the art development and manufacturing capability to fabricate relevant reference materials.
Difficult Challenges < 16 nm	***Summary of Issues***
Nondestructive, production worthy wafer and mask-level microscopy for critical dimension measurement for 3D structures, overlay, defect detection, and analysis	Surface charging and contamination interfere with electron beam imaging. CD measurements must account for sidewall shape. CD for damascene process may require measurement of trench structures. Process control such as focus exposure and etch bias will require greater precision and 3D capability.
New strategy for in-die metrology must reflect across chip and across wafer variation.	Correlation of test structure variations with in-die properties is becoming more difficult as device shrinks. Sampling plan optimization is key to solve these issues.
Statistical limits of sub-16 nm process control	Controlling processes where the natural stochastic variation limits metrology will be difficult. Examples are low-dose implant, thin-gate dielectrics, and edge roughness of very small structures.
Structural and elemental analysis at device dimensions and measurements for *beyond CMOS.*	Materials characterization and metrology methods are needed for control of interfacial layers, dopant positions, defects, and atomic concentrations relative to device dimensions. One example is 3D dopant profiling. Measurements for self-assembling processes are also required.
Determination of manufacturing metrology when device and interconnect technology remain undefined.	The replacement devices for the transistor and structure and materials replacement for copper interconnect are being researched.

MODELING AND SIMULATION

Modeling and simulation software tools span the entire semiconductor world. These tools are being used daily with increasing efficiency. The Modeling and Simulation (M&S) chapter of the ITRS presents specific needs to increase this effectiveness and to provide impact on the semiconductor industry in the future. Similar to the other chapters of the ITRS, in the Modeling and Simulation chapter only the tables have been revised in the 2012 Update. Besides this the preparations for the next full version of the ITRS, the 2013 issue, have been started. Generally, the ITRS is extending its scope which has in the past focused on aggressively scaled devices ("More Moore") to also include functional diversification ("More than Moore"). Whereas for Modeling and Simulation this wider scope will be addressed in more detail in the texts of the 2013 roadmap, a direct impact on the 2012 update has been the broadening of a short-term challenge to now read "Nanoscale/advanced MtM device simulation capability; Methods, models and algorithms". Except for this, the titles of the M&S challenges have been kept unchanged, whereas their content has again evolved: Some new processes, materials and devices have been addressed as well as some additional physical effects.

A key change made in all three "Technology Requirements" tables is that the feature size definitions, such as half pitch and gate length, have been skipped in the table headers. The reason is that modelling and simulation tools should be available before the technology which should be supported by these tools goes into production. Therefore, the time specified does not refer to the manufacturing of a device with certain feature sizes but to the requested availability of simulation.

The table *"Modeling and Simulation Technology Requirements: Capabilities—Near-term Years"* again summarizes the needs in the areas of process, device, circuit and package simulation, and besides this also premier general requirements on tools. The most important changes are as follows: For EUV lithography, high numerical apertures have come into play. The need for data bases for all relevant processes and equipment has been highlighted. Various details of the requirements have been changed, including an update of the timelines, the sequences and the state-of-the-art of several requirements. At this level of detail, also some aspects have been dropped because they were identified as solved.

Compared to this the M&S table on "*Modeling and Simulation Technology Requirements: Capabilities—Long-term Years*" is far less detailed, because long-term technology options are so far only partly defined or prioritized in the other parts of the ITRS. Generally, this long-term requirements table contains in majority "*red" items* for which so far no solutions are known. Partly this is due to the fact that the technological options are not yet known or prioritized, and in turn also simulation approaches cannot yet be developed or selected. Another problem is of course the inherent difficulty to develop models and tools to meet the ambitious requirements—in turn, the success of the development work required from M&S cannot be predicted ten or more years in advance. In the 2012 Update, the long-term requirements for circuit component modelling have been extended to include new memory devices.

The table on *"Modeling and Simulation Technology Requirements: Accuracy—Near-term Years"* is quite similar to the other requirement tables grouped into lithography modeling, front end process modeling, topography modeling, numerical device modeling, circuit element modeling/ECAD, and package modeling. Here, the estimate of about one third, given for the cost and time reduction from use of TCAD in best practice cases reported by industry, is based on an industrial survey already discussed in the 2008 ITRS. In this table, accuracy refers to models and tools calibrated to a certain technology (at a company), not to a certain experiment. Most accuracy specifications are given as percent of the respective nominal value or of some top-level parameter of the respective technology node, e.g., the physical gate length. A key issue in the preparation of this table has been how to define the accuracy of simulation when comparing with experiment which themselves have a significant inaccuracy or uncertainty. Detailed definitions made are listed in the footnotes of the table, e.g., "compared with median value of statistically meaningful samples." Furthermore, the table does not only specify the required accuracy in the simulation of nominal values like a junction depth, but also the accuracy of the sensitivity of such values with respect to changes in process conditions. This is important for tracing the impact of process variations through a simulation sequence, as requested in M&S subchapter on "Modeling for Design Robustness, Manufacturing and Yield" of the 2011 ITRS. In the 2012 Update, the specifications for the simulation of leakage currents have been consolidated, and some time lines have been updated.

Table 18 Modeling and Simulation Difficult Challenges

Difficult Challenges ≥ 14 nm	***Summary of Issues***
Lithography simulation including EUV	Complementary lithography
	Simulation of defect inspection and characterization, influences/defect printing. Mask optimization including defect repair or compensation based on defect signature available from characterization. Multilayer defect propagation.
	Simulation of resolution enhancement techniques including combined mask/source optimization (OPC, PSM) and including EMF and resist effects, and extensions for inverse lithography
	Models that bridge requirements of OPC (speed) and process development (predictive) including EMF effects, including high NA effects for EUV
	Predictive and separable resist models (e.g., mesoscale models) including line-edge roughness, accurate profiles, topcoat and substrate (underlayer) interactions, etch resistance, adhesion, mechanical stability, leaching, swelling or slimming, and time-dependent effects in in single and multiple exposure
	Resist model parameter calibration methodology (including kinetic transport and stochastic parameters)
	Fast, predictive simulation of ebeam mask making (single-beam and multibeam) including short and long range proximity corrections
	Simulation of directed self-assembly of sublithography patterns, esp. guiding pattern optimization and defect formation.
	Modeling lifetime effects of equipment and masks, including lens and mirror heating effects
	Predictive coupled deposition-lithography-etch simulation (incl. double patterning, self-aligned patterning)
	Modeling metrology equipment and data extraction for enhancing model calibration accuracy
	Modeling of pellicle effects and pellicle defects simulation (incl. double patterning, self-aligned patterning)
Front-end process modeling for nanometer structures	Coupled diffusion/(de)activation/damage/stress models and parameters including low-temperature, SPER, millisecond and microwave processes in Si-based substrate, that is, Si, SiGe, Ge-on-Si, III/V-on-Si (esp. InGaAs-on-Ge-on-Si), SOI, epilayers, and ultra-thin body devices, taking into account possible anisotropy in thin layers. Accurate models for stressors and Stress-Induced Defects
	Implantation models (parameters) for ions needed for new materials
	Models for alternative implantation methods: Plasma doping (e.g. conformal doping for FinFETs), cluster implantation, cyro or hot implants (incl. self-annealing)
	Diffusion in advanced gate stacks
	Predictive segregation and dose loss models
	Modeling of interface and dopant passivation by hydrogen or halogens
	Modeling of epitaxially grown layers: Morphology, stress, defects, doping, diffusion, activation
	Modeling hierarchy from atomistic to continuum for dopants and defects in bulk and at interfaces
	Modeling the impact of front-end processing-induced damage to devices on their leakage, noise and reliability behavior during operation
	Efficient and robust 3D meshing for moving boundaries

Table 18 Modeling and Simulation Difficult Challenges

Difficult Challenges ≥ 14 nm	***Summary of Issues***
Integrated modeling of equipment, materials, feature scale processes and influences on device and circuit performance and reliability, including random and systematic variability	Fundamental physical data (e.g., rate constants, cross sections, surface chemistry for ULK, photoresists and high-κ metal gate); reaction mechanisms (reaction paths and (by-) products, rates ...), and simplified but physical models for complex chemistry and plasma reaction
	Linked equipment/feature scale models (including high-κ metal gate integration, flows for RIE processes, damage prediction)
	Deposition processes: MOCVD, PECVD, ALD, electroplating and electroless deposition modeling
	Spin-on-dielectrics (stress, poriosity, dishing, viscosity, …) for high aspect ratio fills, evolution during transformation and densification
	Removal processes: CMP, etch, electrochemical polishing (ECP) (full wafer and chip level, pattern dependent effects)
	Pattern/microloading effects in radiative annealing or plasma processing
	Propagation of process variations into circuit block simulation
	Simulation of wafer polishing, grinding and thinning
	Efficient extraction of impact of equipment – and/or process induced variations on devices and circuits, using simulations
	Modeling of impact of consumables (e.g. resists, slurries, gas quality ….) on process results
Nanoscale/advanced MtM device simulation capability: Methods, models and algorithms	General, accurate, computationally efficient and robust quantum based simulators including fundamental parameters linked to electronic band structure and phonon spectra
	Efficient models and tools for analysis to enable design and evaluation of devices and architectures beyond traditional planar CMOS
	Models (incl. material models) to investigate new memory devices like redox resistive memories, PCM/PRAM, etc.
	Models for gate stacks with ultra-thin/high-κ dielectrics for all channel materials addressed above with respect to electrical permittivity, built-in charges, influence on work function by interface interaction with metals, reliability, tunneling currents and carrier transport
	Modeling of salicide/silicon contact resistance and engineering (e.g., Fermi-level depinning to reduce Schottky barrier height)
	Advanced numerical device simulation models and their efficient usage for predicting and reproducing statistical fluctuations of structure, dopant and material variations in order to assess the impact of variations on statistics of device performance
	Physical models for novel channel materials, e.g., p-type Ge and compound III/V (esp. n-type InGaAs-on-Ge-on-Si) channels …: Band structure, defects/traps …
	Accurate, robust and computational efficient modeling of wide bandgap devices
	Treatment of individual dopant atoms and traps in (commercial) continuum and MC device simulation. Coupling between atomistic process and continuum or atomistic device simulation
	Reliability modeling for ultimate CMOS new memory and HV MOS devices
	Orientation-dependent mobility for non-standard directions
	Commercial device simulators (software) for STT and redox resistive memories
	Physical models for (mechanical) stress induced device performance for advanced architectures (esp. FinFET) and/or novel materials

Table 18 Modeling and Simulation Difficult Challenges

Difficult Challenges ≥ 14 nm	***Summary of Issues***
Electrical-thermal-mechanical-modeling for interconnect and packaging	Model thermal-mechanical, thermodynamic and electrical properties of low κ, high κ, and conductors for efficient on-chip and off-chip incl. SIP and wafer level packages, including power management, and the impact of processing on these properties especially for interfaces and films under 1 micron dimension
	Thermal modeling for 3D ICs and assessment of modeling and CAD tools capable of supporting 3D designs. Thermo-mechanical modeling of Through Silicon Vias and thin stacked dies (incl. adhesive/interposers), and their impact on active device properties (stress, expansion, keep out regions …). Size effects (microstructure, surfaces, ...) and variability of thinned wafers
	Combined EM and drift diffusion simulation to include inductance effects in substrate caused by interconnects and bond wires
	Signal integrity modeling for 3D ICs
	Identify effects and apply/extend models which influence reliability of interconnects/packages incl. 3D integration (e.g., stress voiding, electromigration, fracture initiation, dielectric breakdown, piezoelectric effects)
	Physical models and simulation tools to predict adhesion and fracture toughness on interconnect-relevant interfaces (homogeneous and heterogeneous), packages and die interfaces
	Dynamic simulation of mechanical problems of flexible substrates and packages
	Models for electron transport in ultra fine patterned interconnects
	Simulation tools for die, package and board that allow for coherent co-design
Circuit element and system modeling for high frequency (up to 300 GHz) applications [1]	Supporting heterogeneous integration (SoC+SiP) by enhancing CAD-tools to simulate mutual interactions of building blocks, interconnect, dies on wafer level and in 3D and package: – possibly consisting of different technologies, – covering and combining different modeling and simulation levels as well as different simulation domains – including manufacturability
	Introduction of new model features including non-quasi-static effects, substrate noise and coupling, RT noise, and asymmetric channels in multigate devices
	Computer-efficient inclusion of aging, reliability and variability at device level including their statistics (including correlations) before process freeze into circuit modeling, treating local and global variations consistently
	Scalable active component models for circuit simulation of new multigate MOSFET like double gate FDSOI
	Scalable passive component models [2] for compact circuit simulation, including interconnect, transmission lines, …
	Scalable circuit models [2] for More-than-Moore devices including switches, filters, accelerometers, oscillators …
	Compact models for new memory devices, such as PCM, and standardization of models for III/V (esp. InGaAs-on-Ge-on-SI) devices
	Computer-efficient assessment of building block/circuit-level using process/device/circuit simulation, including process variations
Difficult Challenges < 14 nm	***Summary of Issues***
Modeling of chemical, thermomechanical and electrical properties of new materials	Computational materials science tools to predict materials synthesis, structure, properties, process options, and operating behavior for new materials applied in devices and interconnects, including especially for the following: 1) Layer stacks for gates, junctions and channels: Predictive modeling of dielectric constant, bulk polarization charge, ferroelectric/-magnetic properties, surface states, phase change, thermomechanical (including stress effects on mobility), optical properties, transport properties, reliability, breakdown, and leakage currents including band structure, phonon coupling, tunneling from process/materials and structure conditions 2) Models for novel integrations in (3D) interconnects including data for ultrathin material properties. Models for new ULK materials that are also able to predict process impact on their inherent properties and stability of physical parameters (e.g. keff) 3) Modeling-assisted metrology: Linkage between first principle computation, reduced models (classical MD or thermodynamic computation) and metrology including ERD and ERM applications 4) Use of such tools for accumulation of databases for semi-empirical computation

Table 18 Modeling and Simulation Difficult Challenges

Difficult Challenges ≥ 14 nm	***Summary of Issues***
Nano-scale modeling for Emerging Research Devices and interconnects including Emerging Research Materials	Ab-initio modeling tools for the development of novel nanostructure materials, processes and devices (nanowires, carbon nanotubes (including doping), nano-ribbons (graphene), deterministic doping and doping by chemical functionalization, quantum dots, atomic electronics, multiferroic materials and structures, materials for non-charge-based Beyond-CMOS devices)
	Device modeling tools for analysis of nanoscale device operation (quantum transport, tunneling phenomena, contact effects, spin transport …). Modeling impact of geometry (esp. edge effects / edge roughness), interfaces and bias on transport for carbon-based nanoelectronics (carbon nanotubes and monolayer/bilayer graphene structures)
	Compact models for maturing emerging devices
Optoelectronics modeling	Materials and process models for on-chip/off-chip optoelectronic elements (transmitters and receivers, optical couplers). Coupling between electrical and optical systems, fast and efficient optical interconnect models of larger domains
	Physical design tools for integrated electrical/optical systems
NGL simulation	Simulation of mask less lithography by e-beam direct write (shaped beam / multi beam), including advanced resist modeling (low activation energy effects for low-keV writers (shot noise effects and impact on LER); heating and charging effects), including impact on device characteristics (e.g., due to local crystal damage by electron scattering or charging effects)
	Simulation of nano imprint technology (pattern transfer to polymer = resist modeling, etch process)

Notes for table:
[1] 3 times frequency of envisioned applications (100 Ghz) because of harmonics/linearity

GLOSSARY

KEY ROADMAP TECHNOLOGY CHARACTERISTICS TERMINOLOGY (ALSO WITH OBSERVATIONS AND ANALYSIS)

Moore's Law—An historical observation by Gordon Moore, that the market demand (and semiconductor industry response) for functionality per chip (bits, transistors) doubles every 1.5 to 2 years. He also observed that device affordability must be taken into account and also performance. Although viewed by some as a "self-fulfilling" prophecy, "Moore's Law" has been recently acknowledged and celebrated as a consistent macro trend and key indicator of successful leading-edge semiconductor products and companies for the past 40 years.

Scaling ("More Moore")—

- *Geometrical (constant field) Scaling* refers to the continued shrinking of horizontal and vertical physical feature sizes of the on-chip logic and memory storage functions in order to improve density (cost per function reduction) and performance (speed, power) and reliability values to the applications and end customers.
- *Equivalent Scaling (occurs in conjunction with, and also enables, continued geometrical scaling)* refers to 3-dimensional device structure ("Design Factor") improvements plus other non-geometrical process techniques and new materials that affect the electrical performance of the chip.
- *Design Equivalent Scaling (occurs in conjunction with equivalent scaling and continued geometric scaling)* refers to design technologies that enable high performance, low power, high reliability, low cost, and high design productivity.
  - "Examples (not exhaustive) are: Design for variability; low power design (sleep modes, hibernation, clock gating, multi-Vdd, etc.); and homogeneous and heterogeneous multicore SOC architectures."
  - Addresses the need for quantifiable, specific Design Technologies that address the power and performance tradeoffs associated with meeting "More Moore" functionality needs, and may also drive "More Moore" architectural functionality as part of the solution to power and performance needs.

Functional Diversification ("More than Moore")—The incorporation into devices of functionalities that do not necessarily scale according to "Moore's Law," but provides additional value to the end customer in different ways. The "More-than-Moore" approach typically allows for the non-digital functionalities (e.g., RF communication, power control, passive components, sensors, actuators) to migrate from the system board-level into a particular package-level (SiP) or chip-level (SoC) potential solution.

- Design technologies enable new functionality that takes advantage of More than Moore technologies.
- "Examples (not exhaustive) are: Heterogeneous system partitioning and simulation; software; analog and mixed signal design technologies for sensors and actuators; and new methods and tools for co-design and co-simulation of SIP, MEMS, and biotechnology."
- Addresses the need for design technologies which enable functional diversification.

Beyond CMOS—emerging research devices, focused on a "new switch" used to process information, typically exploiting a new state variable to provide functional scaling substantially beyond that attainable by ultimately scaled CMOS. Substantial scaling beyond CMOS is defined in terms of functional density, increased performance, dramatically reduced power, etc. The "new switch" refers to an "information processing element or technology," which is associated with compatible storage or memory and interconnect functions.

- Examples of Beyond CMOS include: carbon-based nano-electronics, spin-based devices, ferromagnetic logic, atomic switch, NEMS switches, etc.

CHARACTERISTICS OF MAJOR MARKETS

Technology Cycle Time Period—The timing to deliver 0.71× reduction per period or 0.50 reduction per two periods of a product-scaling feature. The minimum half-pitch Metal 1 scaling feature of custom-layout (i.e., with staggered contacts/vias) metal interconnect is most representative of the process capability enabling high-density (low cost/function) integrated DRAM and MPU/ASIC circuits, and is selected to define an ITRS Technology Cycle. The Flash product technology cycle timing is defined by the uncontacted dense line half-pitch. For each product-specific technology cycle timing, the defining metal or polysilicon half-pitch is taken from whatever product has the minimum value. Historically, DRAMs have had leadership on metal pitch, but this could potentially shift to another product in the future.

Other scaling feature parameters are also important for characterizing IC technology. The half-pitch of first-level stagger-contacted interconnect dense lines is most representative of the DRAM technology level required for the smallest economical chip size. However, for logic, such as microprocessors (MPUs), the physical bottom gate length isolated feature is most representative of the leading-edge technology level required for maximum performance, and includes additional etch process steps beyond lithography printing to achieve the smallest feature targets.

MPU and ASIC logic interconnect half-pitch processing requirement typically refers to the first stagger-contacted metal layer (M1) and presently lags slightly behind DRAM stagger-contacted M1 half-pitch. The smallest half-pitch is typically found in the memory cell area of the chip. Each technology cycle time (0.71× reduction per cycle period, 0.50× reduction per two cycle periods) step represents the creation of significant technology equipment and materials progress in the stagger contacted metal half-pitch (DRAM, MPU/ASIC) or the uncontacted polysilicon (Flash product).

As defined above, additional "Equivalent Scaling" process technologies can be combined with transistor gate dimensional scaling technology advancement to further advance the performance and power-management characteristics of a device. The "Equivalent Scaling" technologies can also be "mix-and-matched" by companies within their specific product fabs. In some cases the most recent ITRS TWG surveys have indicated that dimensional scaling (both gate length and gate material thickness) reduction can be slowed and still meet power management and performance requirements, when traded off with "equivalent scaling" process insertion.

Some (not comprehensive or complete) examples of "equivalent scaling" process and transistor design technology are: copper interconnect; low-κ interconnect materials; strained silicon; high-κ/metal gate; fully depleted silicon-on-insulator (FDSOI); multiple-gate 3-D transistors, III-V gate material; etc.

It should be noted that the timing of availability and implementation of "equivalent scaling" process insertion may not be as regular as dimensional cycles. See the Interconnect and process integration and device structures (PIDS) chapters for additional technology description and timing details.

Cost-per-Function Manufacturing Productivity Improvement Driver—In addition to the "Moore's Law" driver of functions/chip doubling every two years , there has been a historically-based "corollary" to the "law," which suggests that, to be affordable and competitive, manufacturing productivity improvements must also enable the cost-per-function (micro-cents per bit or transistor) to decrease by -29% per year. Historically, when functionality doubled every 2 years, cost per function must also reduce by half every 2 years (-29%/year average). On average then cost-per-chip (packaged unit), for affordability, could remain approximately constant (requires both flat chip cost targets and flat back-end packaging targets to remain constant), If functionality doubles only every three years, then the manufacturing cost per chip (packaged unit) can remain flat if the cost per function reduction rate slows to one-half every 3 years (-21%/year average). It should be noted that this simplistic manufacturing cost affordability model, used as a first-order driver for the ITRS, does not take into account the economic supply and demand market complexity of actual external market environments.

Affordable Packaged Unit Cost/Function—Final cost in microcents of the cost of a tested and packaged chip divided by Functions/Chip. Affordable costs are calculated from historical trends of affordable average selling prices [gross annual revenues of a specific product generation divided by the annual unit shipments] less an estimated gross profit margin of approximately 35% for DRAMs and 60% for MPUs. The affordability per function is a guideline of future market "tops-down" needs, and as such, was generated independently from the chip size and function density. Affordability requirements are expected to be achieved through combinations of—1) increased density and smaller chip sizes from technology and design improvements; 2) increasing wafer diameters; 3) decreasing equipment cost-of-ownership; 4) increasing equipment overall equipment effectiveness; 5) reduced package and test costs; 6) improved design tool productivity; and 7) enhanced product architecture and integration.

DRAM and Flash Generation at (product generation life-cycle level)—The anticipated bits/chip of the DRAM or Flash product generation introduced in a given year, manufacturing technology capability, and life-cycle maturity (Demonstration-level, Introduction-level, Production-level, Ramp-level, Peak).

Flash Single-Level Cell (SLC)—A Flash non-volatile memory cell with only one physical bit of storage in the cell area.

Flash Multi-Level Cell (MLC)—The ability to electrically store and access two to four bits of data in the same physical area.

MPU Generation at (product generation life-cycle level)—The generic processor generation identifier for the anticipated MPU product generation functionality (logic plus SRAM transistors per chip) introduced in a given year, manufacturing technology capability, and life-cycle maturity (Introduction-level, Production-level, Ramp-level, Peak).

Cost-Performance MPU—MPU product optimized for maximum performance and the lowest cost by limiting the amount of on-chip SRAM level-two and level-three (L2 and L3) cache. Logic functionality and L2 cache typically double every two to three-year technology cycle (0.71×/cycle period) generation.

High-performance MPU[9]—MPU product optimized for maximum system performance by combining a single or multiple CPU cores with large level-2 and level-3 (L2 and L3) SRAM. Logic functionality and L2 cache typically double every two to three-year technology cycle (0.71×/cycle period) generation by doubling the number of on-chip CPU cores and associated memory. Recently the typical pattern among MPU products is to keep the number of cores constant within a generation and double the number of transistors within each core, and the latest ITRS ORTC modeling reflects this trend in the table targets.

Product inTER-generation—Product generation-to-generation targets for periodically doubling the on-chip functionality at an affordable chip size. The targets are set to maintain Moore's Law (2×/two years) while preserving economical manufacturability (flat chip size and constant manufacturing cost per unit). This doubling every two years at a constant cost assures that the cost/function reduction rate (inverse productivity improvement) is -29% per year (the target historical rate of reduction). In order to double the on-chip functionality every two years, when technology cycle scaling (.7× linear, .5× area) is every three years, the chip size must increase.

The 2005 ITRS consensus target for the time between a doubling of DRAM bits/chip had increased from 2× bits/chip every two years to 2×/chip every three years average. Historically, DRAM cell designers achieved the required cell-area-factor improvements, however, the slower bits/chip growth is still maintained, although the latest consensus ITRS forecast of cell-area-factor improvement to 4 by 2011, but flat thereafter... Presently, the MPU transistor area is shrinking only at lithography-based rate. Therefore, the latest ITRS MPU inTER-generation functionality model target is 2× transistors/chip every technology cycle time, in order maintain a flat maximum introductory and affordable production chip size growth throughout the roadmap period.

Product inTRA-generation—Chip size shrink trend within a given constant functions-per-chip product generation. The latest ITRS consensus-based model targets reduce chip size (by shrinks and "cut-downs") utilizing the latest available manufacturing and design technology at every point through the roadmap. The ITRS targets for both DRAM and MPU reduce chip size within a generation by minus 50% per 0.71× technology cycle timing.

Year of Demonstration—Year in which the leading chip manufacturer supplies an operational sample of a product as a demonstration of design and/or technology generation processing feasibility and prowess. A typical venue for the demonstration is a major semiconductor industry conference, such as the International Solid State Circuits Conference (ISSCC) held by the Institute of Electrical and Electronic Engineers (IEEE). Demonstration samples are typically manufactured with early development or demonstration- level manufacturing tools and processes. Historically, DRAM products have been demonstrated at 4× bits-per-chip every three to four years at the leading-edge process technology generation, typically two–three years in advance of actual market introduction. DRAM demonstration chip sizes have doubled every six to eight years, requiring an increasing number of shrinks and delay before market introduction is economically feasible. Frequently, chip sizes are larger than the field sizes available from lithography equipment, and must be "stitched" together via multiple-exposure techniques that are feasible only for very small quantities of laboratory samples.

Example: 1997/ISSCC/1Gb DRAM, versus ITRS 1Gb 1999 Introduction-level, 2005 Production-level targets.

Year of INTRODUCTION—Year in which the leading chip manufacturer supplies small quantities of engineering samples (typically <1K). These are provided to key customers for early evaluation, and are manufactured with qualified production tooling and processes. To balance market timeliness and economical manufacturing, products will be introduced at 2× functionality per chip every technology cycle reduction (0.71×/cycle period), unless additional design-factor improvement occurs, which allows additional chip shrinking or additional functionality per chip. In addition, manufacturers will delay production until a chip-size shrink or "cut-down" level is achieved which limits the inTER-generation chip-size growth to be flat.

Year of PRODUCTION—Year in which at least one leading chip manufacturers begins shipping volume quantities (initially, 10K/month or higher, depending upon die size and wafer generation size) of product manufactured with customer product qualified* production tooling and processes and is followed within three months by a second

[9] *Note: The 2007 MPU model was revised by the Design TWG to introduce the doubling of logic cores every other technology cycle, but function size and density was kept unchanged by doubling the transistor/core targets. The Design TWG believed this approach to the MPU Model was more representative of current design trends.*

manufacturer. (**Note: Start of actual volume production ramp may vary between one to twelve months depending upon the length of the customer product qualification*). As demand increases for the leading-edge performance and shrink products, the tooling and processes are being quickly "copied" into multiple modules of manufacturing capacity.

For high-demand products, volume production typically continues to ramp to fab design capacity within twelve months. Alpha-level manufacturing tools and research technology papers are typically delivered 24–36 months prior to volume production ramp. Beta-level tools are typically delivered 12–24 months prior to ramp, along with papers at industry conferences. The beta-level tools are made production-level in pilot-line fabs, which must be ready up to 12–24 months prior to Production Ramp "Time Zero" [see Figure 2a in the Executive Summary] to allow for full customer product qualification. The production-level pilot line fabs may also run low volumes of product that is often used for customer sampling and early qualification prior to volume production ramp. Medium-volume production-level DRAMs will be in production concurrently with low-volume introduction-level DRAMs, and also concurrently with very-high-volume, shrunken, previous-generation DRAMs (example: 2003: .5 Gb/production, 4 G/introduction, plus 256 Mb/128 Mb/64 Mb high-volume). Similarly, high-volume cost-performance MPUs are in production concurrently with their lower-volume, large-chip, high-performance MPU counterparts, and also with very-high volume shrinks of previous generations.

Functions/Chip—The number of bits (DRAMs) or logic transistors (MPUs/ASICs) that can be cost-effectively manufactured on a single monolithic chip at the available technology level. Logic functionality (transistors per chip) include both SRAM and gate-function logic transistors. DRAM functionality (bits per chip) is based only on the bits (after repair) on a single monolithic chip.

Chip Size (mm^2)—The typical area of the monolithic memory and logic chip that can be affordably manufactured in a given year based upon the best available leading-edge design and manufacturing process. (Estimates are projected based upon historical data trends and the ITRS consensus models).

Functions/cm^2—The density of functions in a given square centimeter = Functions/Chip on a single monolithic chip divided by the Chip Size. This is an average of the density of all of the functionality on the chip, including pad area and wafer scribe area. In the case of DRAM, it includes the average of the high-density cell array and the less-dense peripheral drive circuitry. In the case of the MPU products, it includes the average of the high-density SRAM and the less-dense random logic. In the case of ASIC, it will include high-density embedded memory arrays, averaged with less dense array logic gates and functional cores. In the 2009 ITRS, the typical high-performance ASIC (hpASIC) design is assumed to have the same average density as the high-performance MPUs, which are mostly SRAM transistors.

DRAM Cell Array Area Percentage—The maximum practical percentage of the total DRAM chip area that the cell array can occupy at the various stages of the generation life cycle. At the introduction chip size targets, this percentage must be typically less than 74% to allow space for the peripheral circuitry, pads, and wafer scribe area. Since the pads and scribe area do not scale with lithography, the maximum cell array percentage is reduced in other inTRA-generation shrink levels (typically less than 56% at the production level, and also for shrunk die at the high-volume ramp level).

DRAM Cell Area (μm^2)—The area (C) occupied by the DRAM memory bit cell, expressed as multiplication of a specified ITRS-consensus cell area factor target (A) times the square of the minimum half-pitch feature (f) size, that is: $C = Af^2$. To calculate the chip size, the cell area must be divided by the array efficiency, a factor (E) that is statistically derived from historical DRAM chip analysis data. Thus an average cell area (C_{AVE}) can be calculated, which is burdened by the overhead of the drivers, I/O, bus lines, and pad area. The formula is: $C_{AVE} = C/E$.

The total chip area can then be calculated by multiplying the total number of bits/chip times the C_{AVE}.

Example: 2000: A=8; square of the half-pitch, $f^2 = (180\ nm)^2 = .032\ \mu m^2$; cell area, $C=Af^2=0.26\ \mu m^2$; for 1 Gb introduction-level DRAM with a cell efficiency of E=74% of total chip area, the $C_{AVE} = C/E = 0.35\ \mu m^2$; therefore, the 1 Gb Chip Size Area=2^{30} bits * 0.35e-6 mm^2/bit = 376 mm^2.

DRAM Cell Area Factor—A number (A) that expresses the DRAM cell area (C) as a multiple of equivalent square half-pitch (f) units. Typically, the cell factor is expressed by equivalent aspect ratios of the half-pitch units (2×4=8, 2×3=6, 2×2=4, etc.).

Flash Cell Area Factor—Similar to DRAM area factor for a single-level cell (SLC) size. However, the Flash technology has the ability to store and electrically access two to four bits in the same cell area, creating a multi-level-cell (MLC) "virtual" per-bit size that is one-half to one-fourth the size of an SLC product cell size and will also have a "virtual area factor" that is half to one-fourth of the SLC Flash Product.

SRAM Cell Area Factor—Similar to the DRAM area factor, only applied to a 6-transistor (6t) logic-technology latch-type memory cell. The number expresses the SRAM 6t cell area as a multiple of equivalent square technology-generation half-

pitch (f) units. Typically, the cell factor of the SRAM 6t cell is 10–15 times greater than a DRAM memory cell area factor.

Logic Gate Cell Area Factor—Similar to the DRAM and SRAM cell area factors, only applied to a typical 4-transistor (4t) logic gate. The number expresses the logic 4t gate area as a multiple of equivalent square technology-generation half-pitch (f) units. Typically, the cell factor of the logic 4t gate is 2–3 times greater than an SRAM 6t cell area factor, and 30–40 times greater than a DRAM memory cell area factor.

Usable Transistors/cm^2 (High-performance ASIC, Auto Layout)—Number of transistors per cm^2 designed by automated layout tools for highly differentiated applications produced in low volumes. High-performance, leading-edge, embedded-array ASICs include both on-chip array logic cells, as well as dense functional cells (MPU, I/O, SRAM, etc.). Density calculations include the connected (useable) transistors of the array logic cells, in addition to all of the transistors in the dense functional cells. The largest high-performance ASIC designs will fill the available production lithography field.

CHIP AND PACKAGE—PHYSICAL AND ELECTRICAL ATTRIBUTES

Number of Chip I/Os–Total (Array) Pads—The maximum number of chip signal I/O pads plus power and ground pads permanently connected to package plane for functional or test purposes, or to provide power/ground contacts (including signal conditioning). These include any direct chip-to-chip interconnections or direct chip attach connections to the board (Package plane is defined as any interconnect plane, leadframe, or other wiring technology inside a package, i.e., any wiring that is not on the chip or on the board). MPUs typically have a ratio of signal I/O pads to power/ground pads of 1:2, whereas the high-performance ASIC ratio is typically 1:1.

Number of Chip I/Os–Total (Peripheral) Pads—The maximum number of chip signal I/O plus power and ground pads for products with contacts only around the edge of a chip.

Pad Pitch—The distance, center-to-center, between pads, whether on the peripheral edge of a chip, or in an array of pads across the chip.

Number of Package Pins/Balls—The number of pins or solder balls presented by the package for connection to the board (may be fewer than the number of chip-to-package pads because of internal power and ground planes on the package plane or multiple chips per package).

Package Cost (Cost-performance)—Cost of package envelope and external I/O connections (pins/balls) in cents/pin.

CHIP FREQUENCY (MHZ)

On-Chip, Local Clock, High-performance—On-chip clock frequency of high-performance, lower volume microprocessors in localized portions of the chip.

Chip-To-Board (Off-chip) Speed (High-performance, Peripheral Buses)—Maximum signal I/O frequency to board peripheral buses of high and low volume logic devices.

OTHER ATTRIBUTES

Lithographic Field Size (mm^2)—Maximum single step or step-and-scan exposure area of a lithographic tool at the given technology generation. The specification represents the minimum specification that a semiconductor manufacturer might specify for a given technology generation. The maximum field size may be specified higher than the ORTC target values, and the final exposure area may be achieved by various combinations of exposure width and scan length.

Maximum Number of Wiring Levels—On-chip interconnect levels including local interconnect, local and global routing, power and ground connections, and clock distribution.

FABRICATION ATTRIBUTES AND METHODS

Electrical D_0 Defect Density (d/m^{-2})—Number of electrically significant defects per square meter at the given technology generation, production life-cycle year, and target probe yield.

Minimum Mask Count—Number of masking levels for mature production process flow with maximum wiring level (Logic).

MAXIMUM SUBSTRATE DIAMETER (MM)

Bulk or Epitaxial or Silicon-on-Insulator Wafer—Silicon wafer diameter used in volume quantities by mainstream IC suppliers. The ITRS timing targets, contributed by the Factory Integration ITWG, are based on the first production-qualified development manufacturing facilities. Additional clarification was added by the IRC in 2009 to differentiate the

new 450 mm wafer generation early consortia pilot line equipment readiness from the timing of anticipated production readiness and ramp.

ELECTRICAL DESIGN AND TEST METRICS

POWER SUPPLY VOLTAGE (V)

Minimum Logic V_{dd}—Nominal operating voltage of chips from power source for operation at design requirements.

Maximum Power High-performance with Heat Sink (W)—Maximum total power dissipated in high-performance chips with an external heat sink.

Battery (W)—Maximum total power/chip dissipated in battery operated chips.

DESIGN AND TEST

Volume Tester Cost/Pin ($K/pin)—Cost of functional (chip sort) test in high volume applications divided by number of package pins.