EuroNanoForum 2013
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IRELAND'S PRESIDENCY OF THE COUNCIL OF THE EU

CMOS and Beyond: Future Device Technology.

Kelin J. Kuhn

Intel Fellow

Intel Corporation

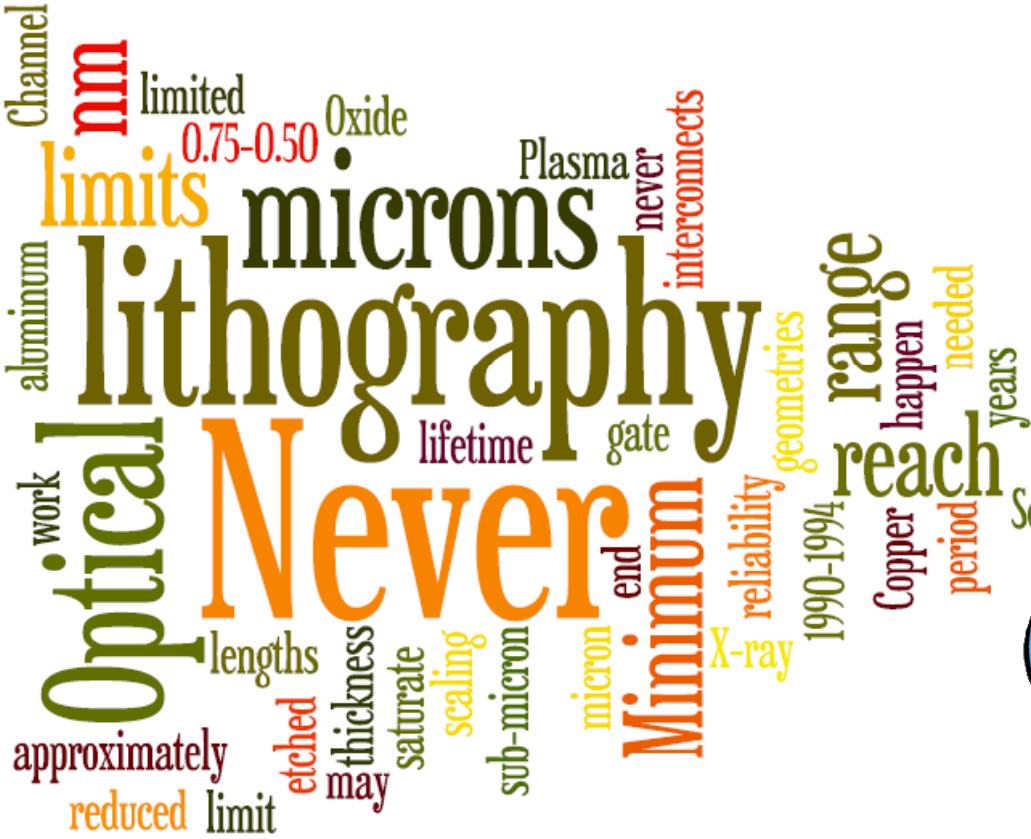
ENTERPRISE IRELAND
where innovation means business
SPINVERSE
Capital & Consulting
European Commission
SEVENTH FRAMEWORK PROGRAMME

Messages

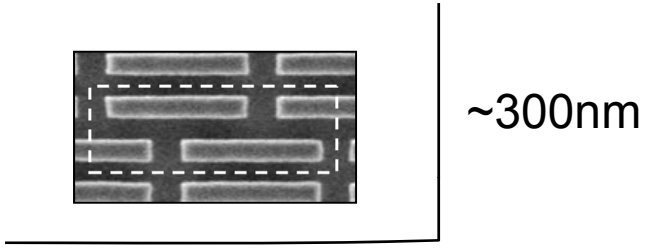
- It's NOT the End of the World
- Plenty of Room at the Bottom
- Many Creative New Options

It's NOT the End of the World

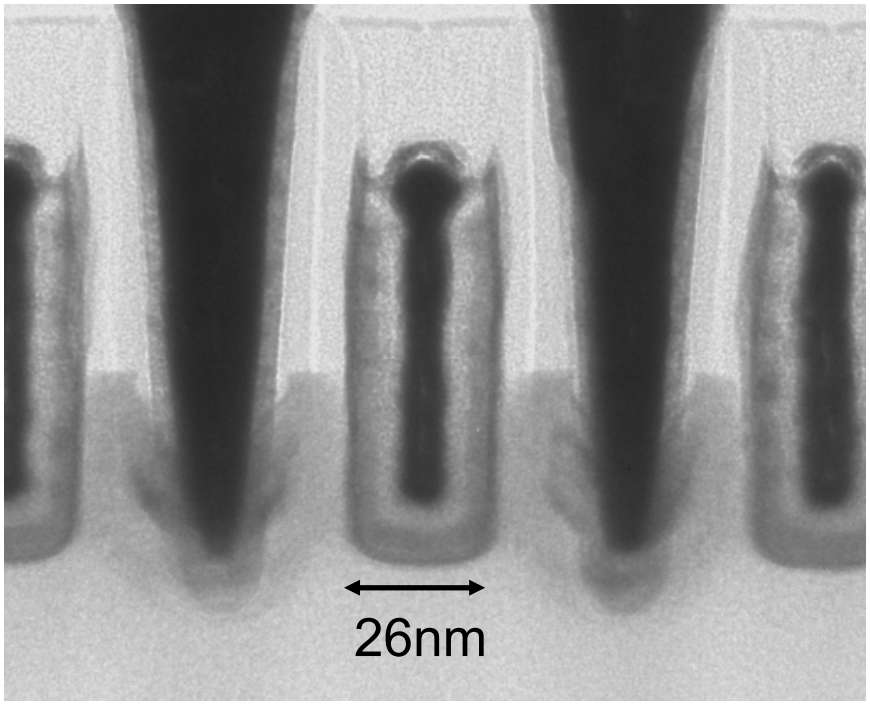
The End of Scaling is Near?



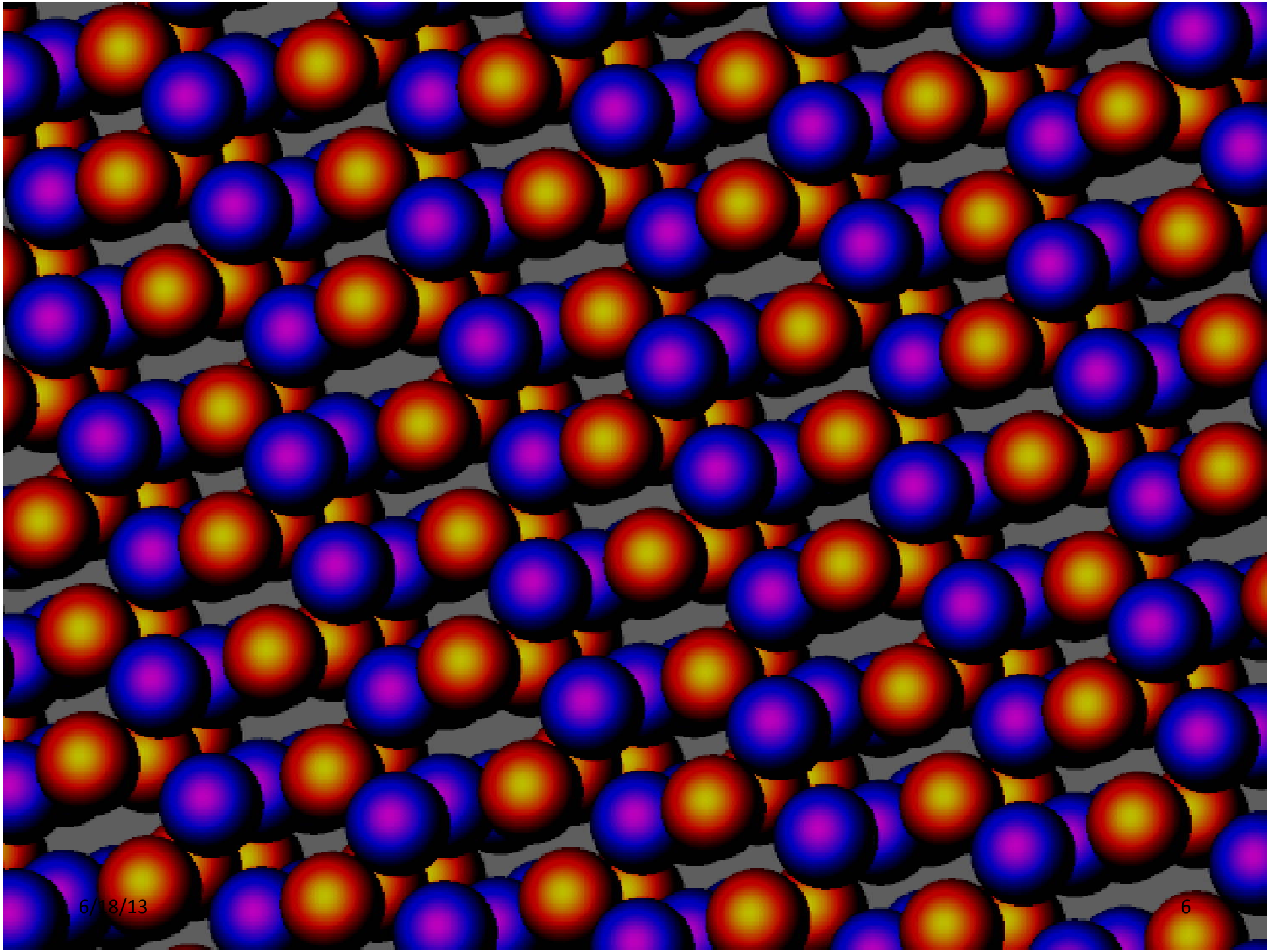
So? Where are we today?

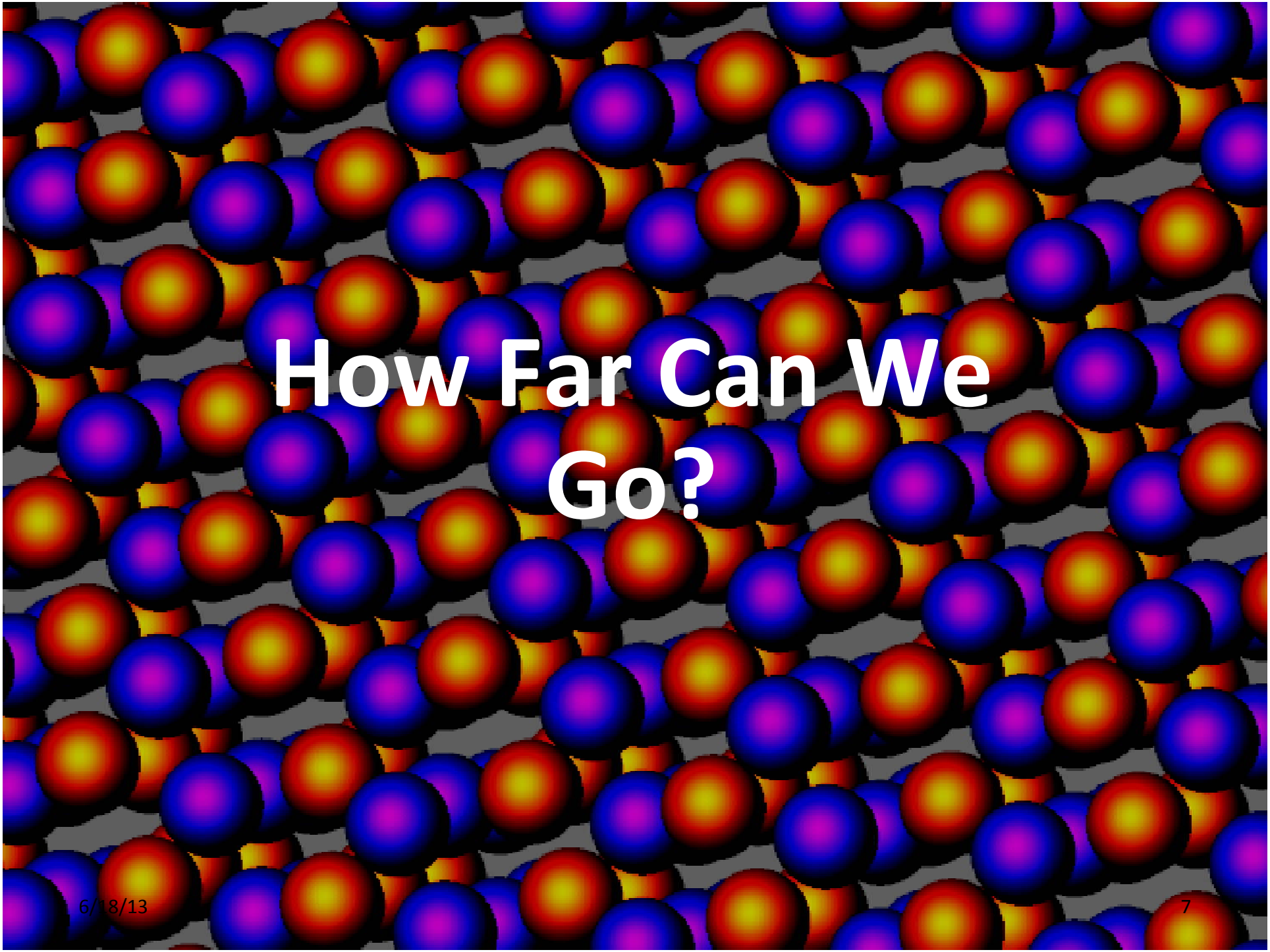


The ENTIRE 22nm SRAM cell
is SMALLER
than was speculated
in mid-1980s
for the limit of the size
of the GATE alone!

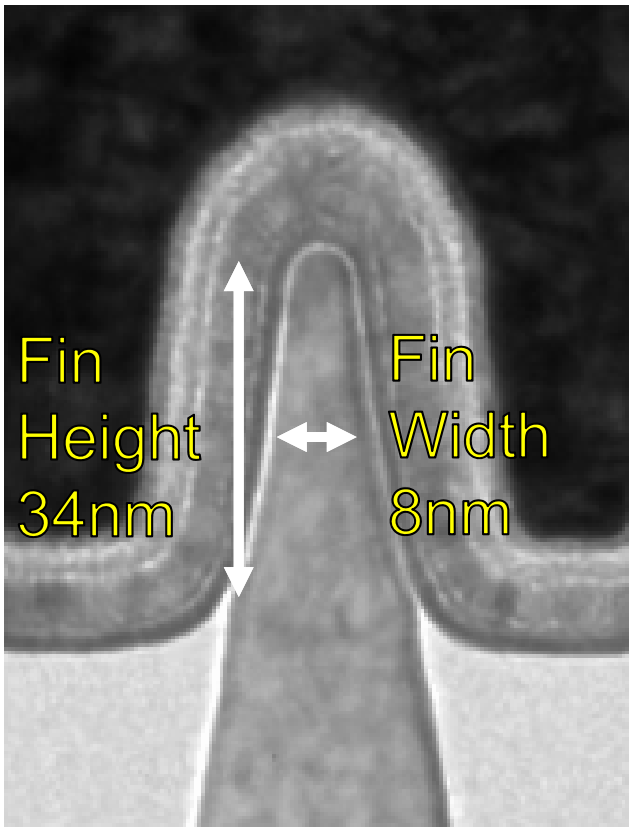


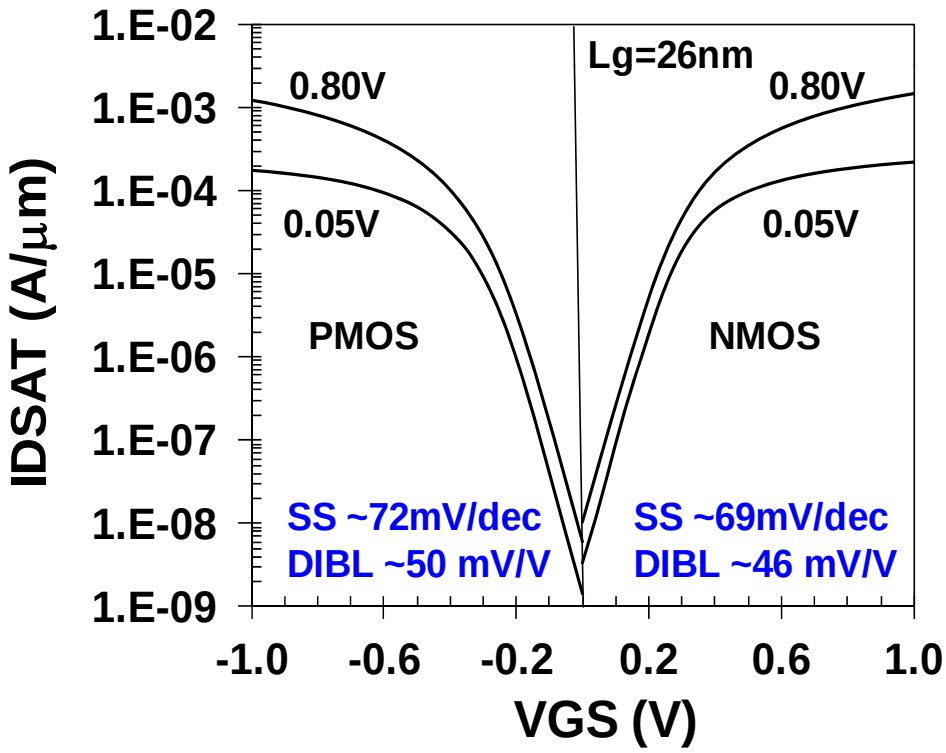
WRONG
By ~10X even!




How Far Can We Go?

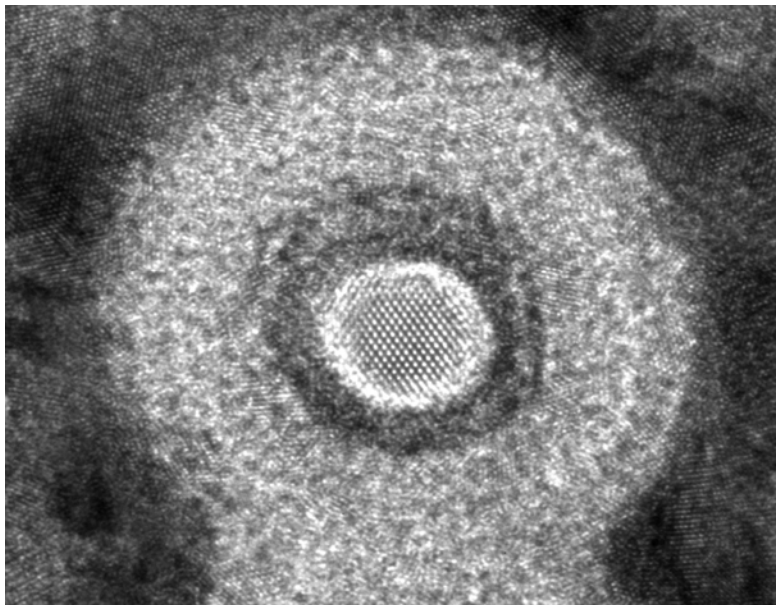
Production 22nm Tri-Gate Transistors ~400,000 atoms

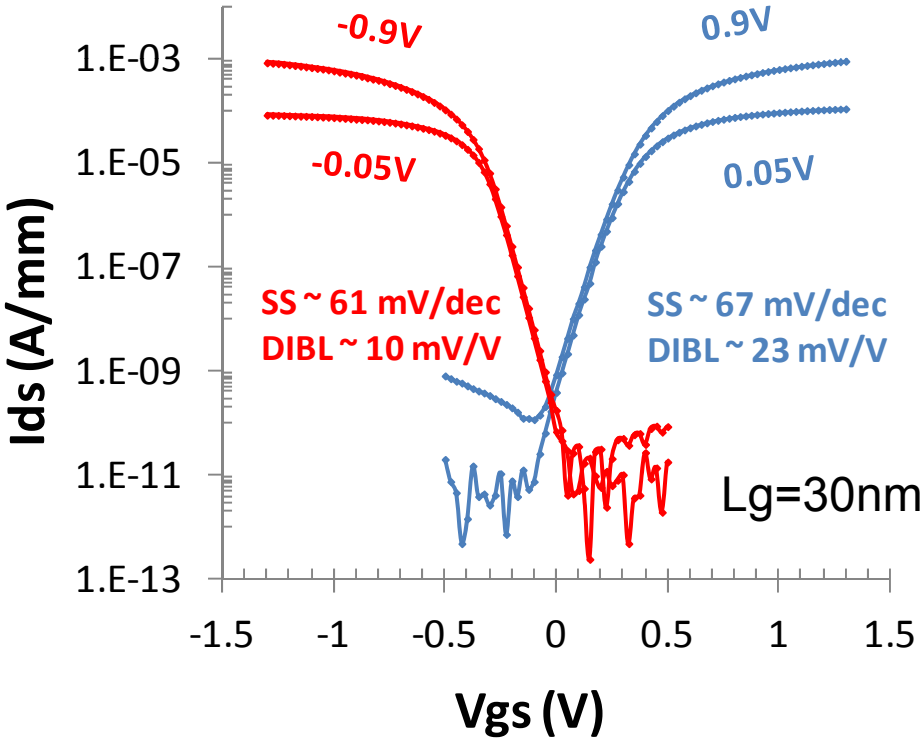




C. Auth, VLSI 2012

Research Nanowire Transistors ~40,000 atoms





K. Kuhn, IEDM 2012

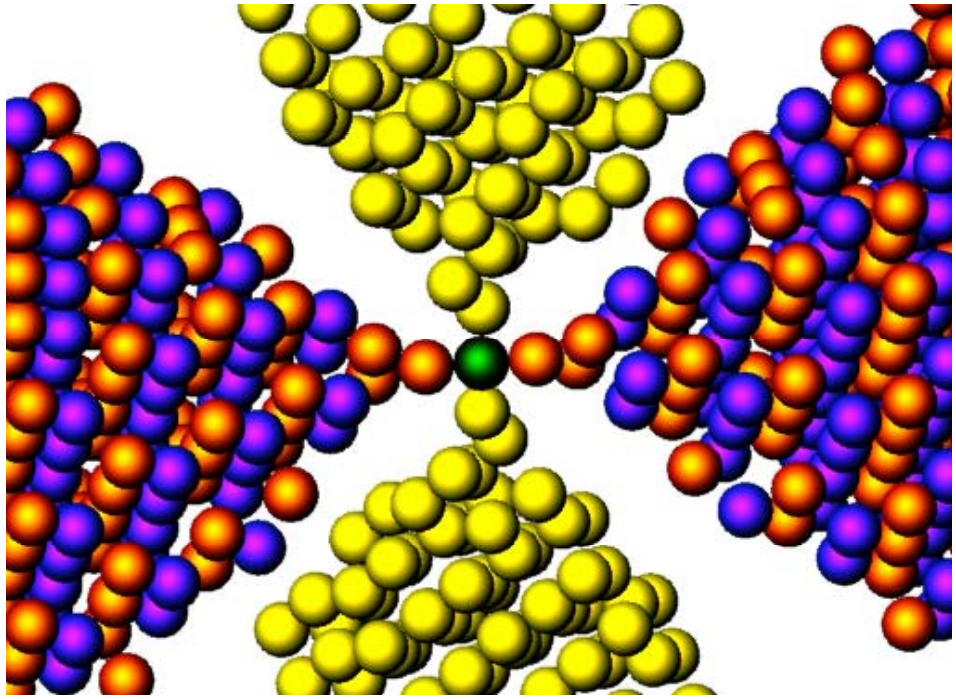
Research Physics: One Atom Transistors

"A single-atom transistor"

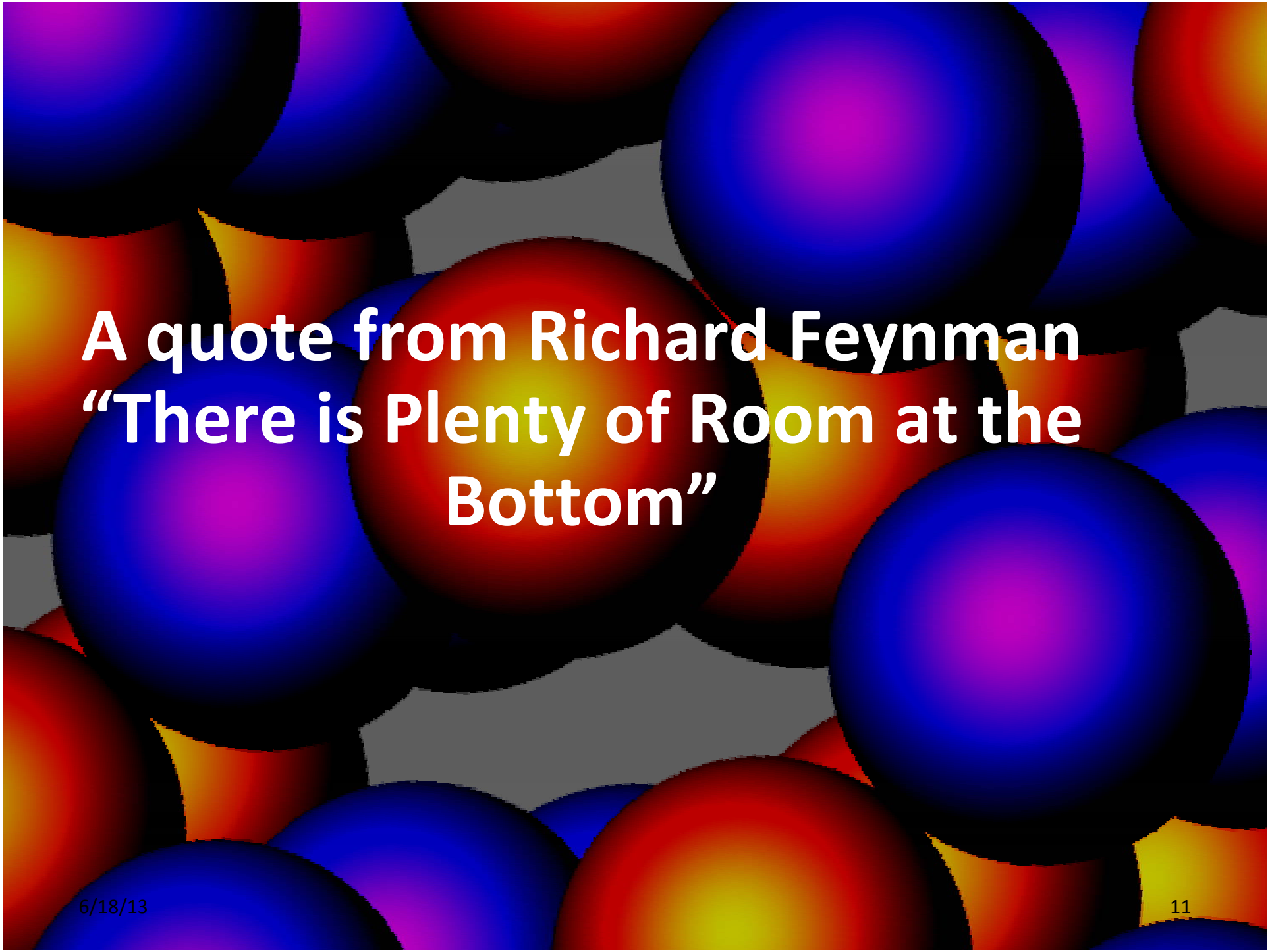
Nature Nanotechnology, Feb. 19, 2012
Martin Fuechsle, Jill A. Miwa, Suddhasatta Mahapatra, Hoon Ryu, Sunhee Lee, Oliver Warschkow, Lloyd C. L. Hollenberg, Gerhard Klimeck and Michelle Y. Simmons

"Gate-induced quantum-confinement transition of a single dopant atom in a silicon FinFET"

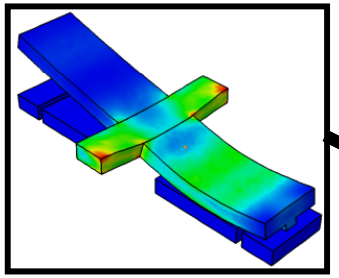
Nature Physics, June 15 2008
G. P. Lansbergen, R. Rahman, C. J. Wellard, I. Woo, J. Caro, N. Collaert, S. Biesemans, G. Klimeck, L. C. L. Hollenberg and S. Rogge



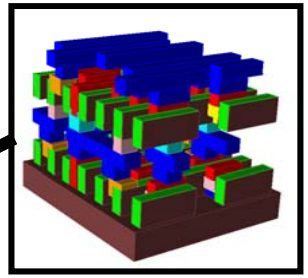
400000 * (0.5)^N ~ 1
N= 18


A quote from Richard Feynman
“There is Plenty of Room at the Bottom”

MANY
Creative New Options

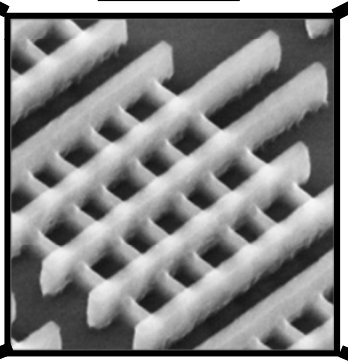


Nano-mechanical



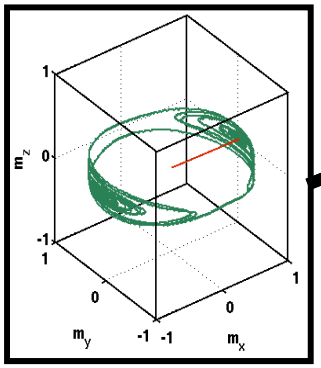
Vertical

22nm



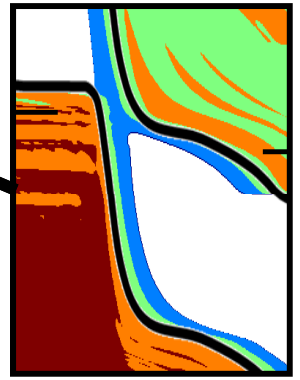
FUNCTION

DENSITY

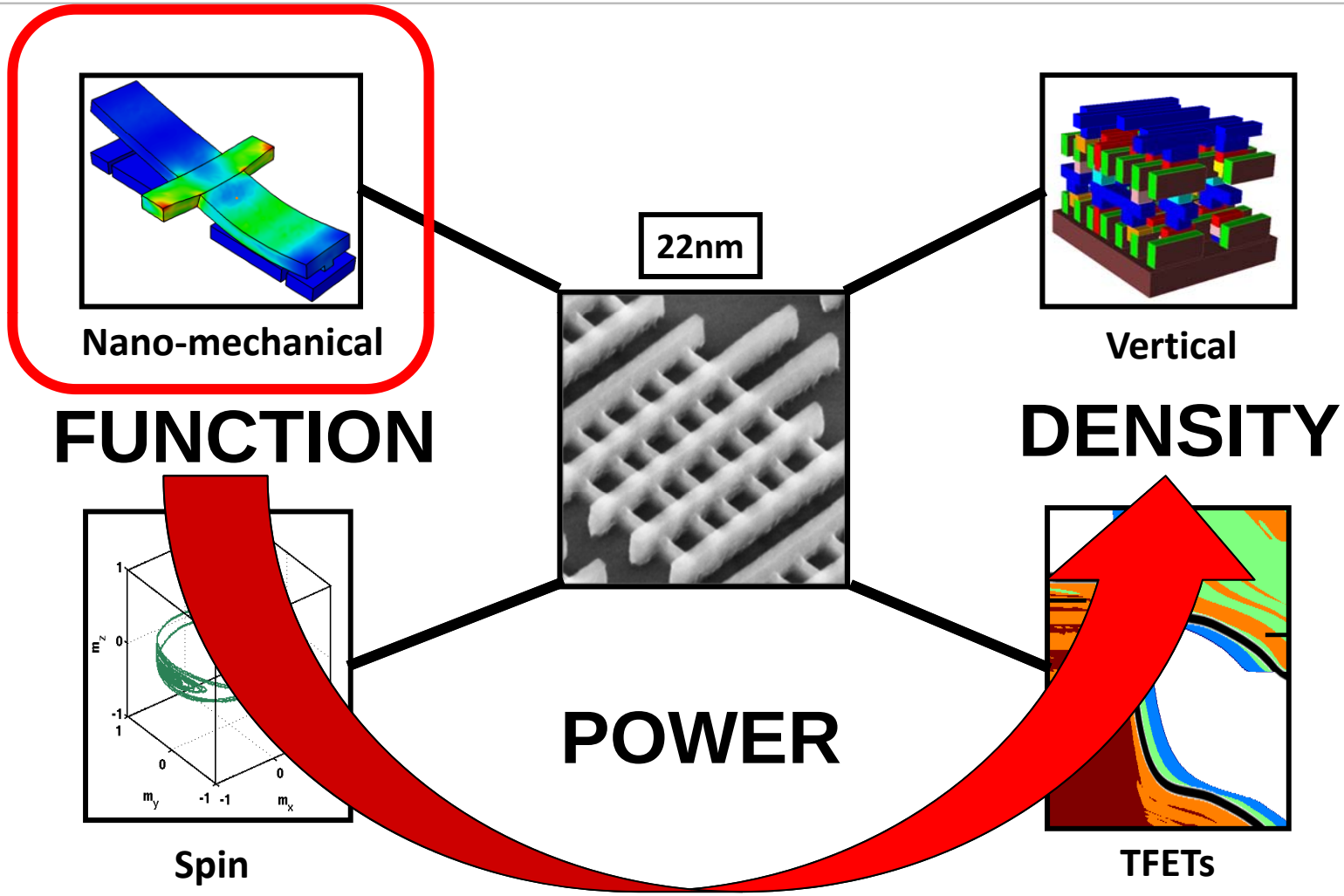


Spin

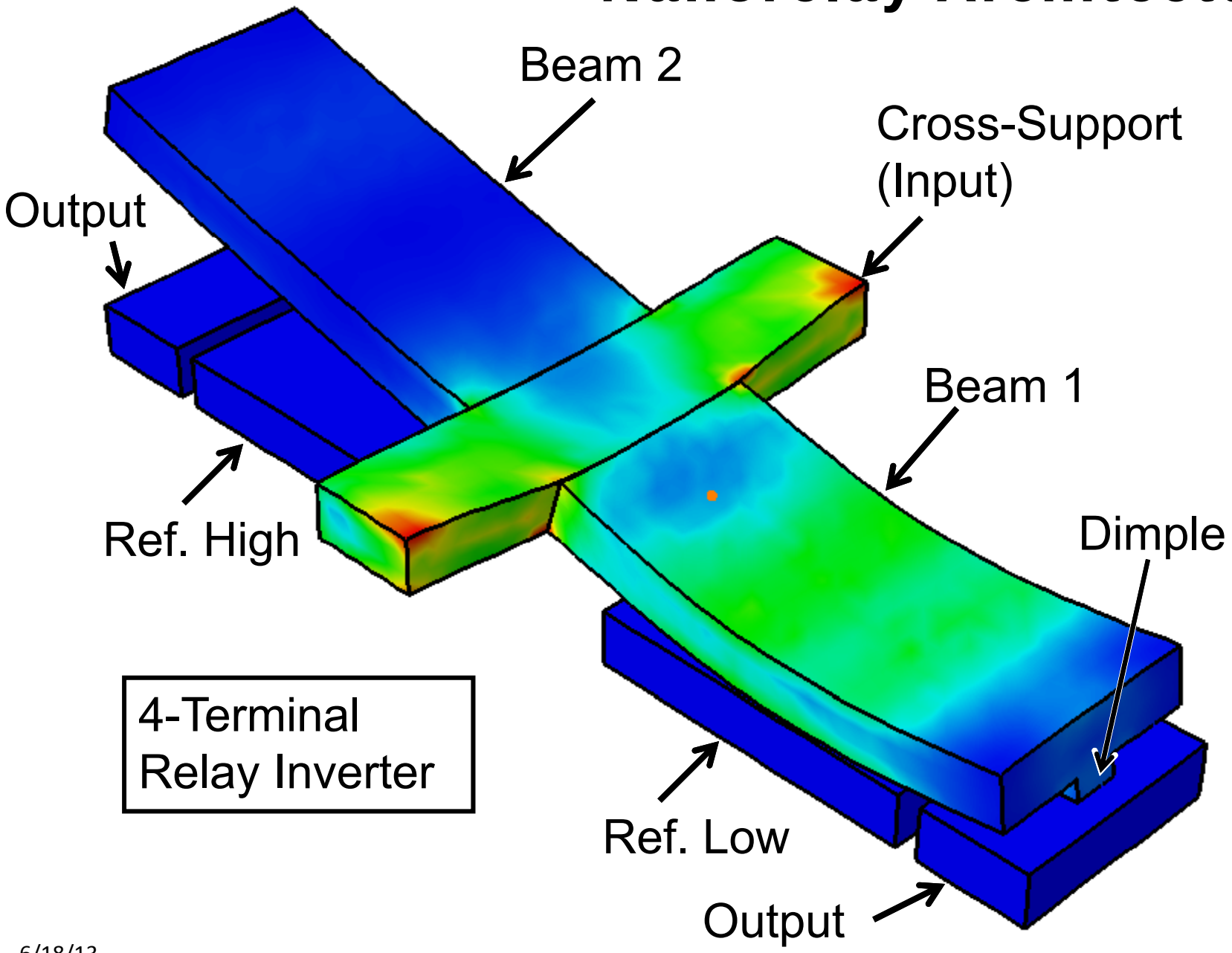
POWER



TFETs


Nano-mechanical
22nm
Vertical
FUNCTION
DENSITY
POWER
Spin
TFETs

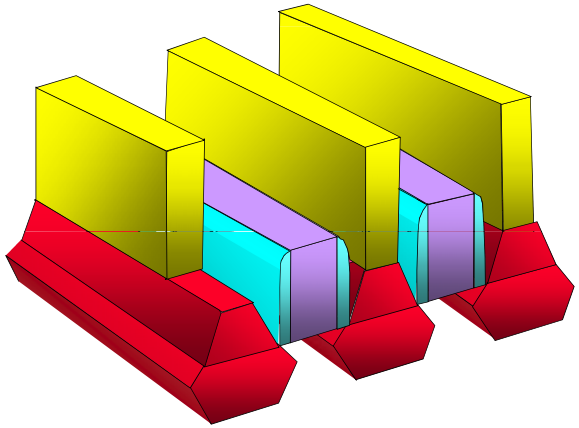
Nanorelay Architecture



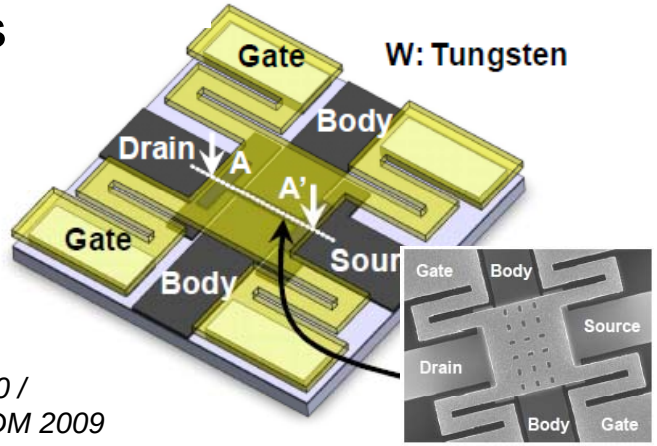
Courtesy: Chytra Pawashe

CMOS Switch vs Relay Switch

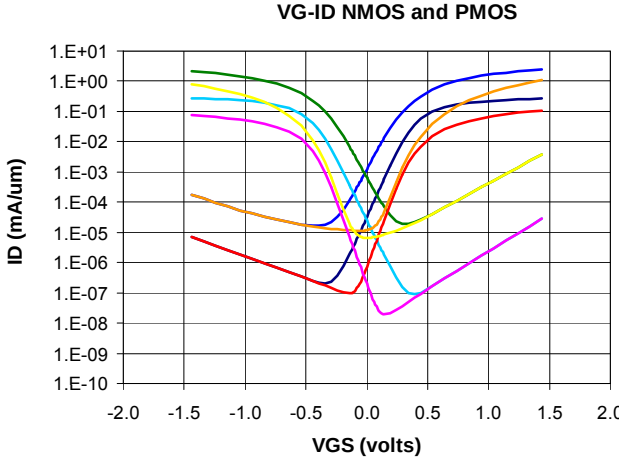
CMOS

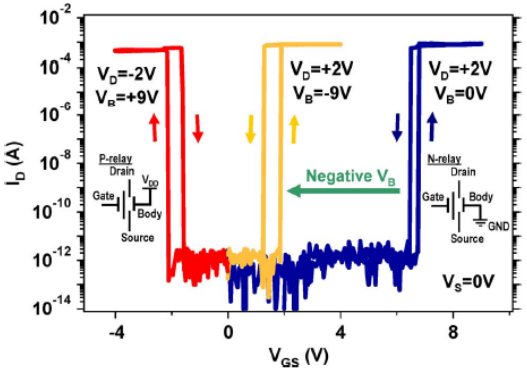


NEMs



Liu IEDM 2010 /
Nathanael IEDM 2009

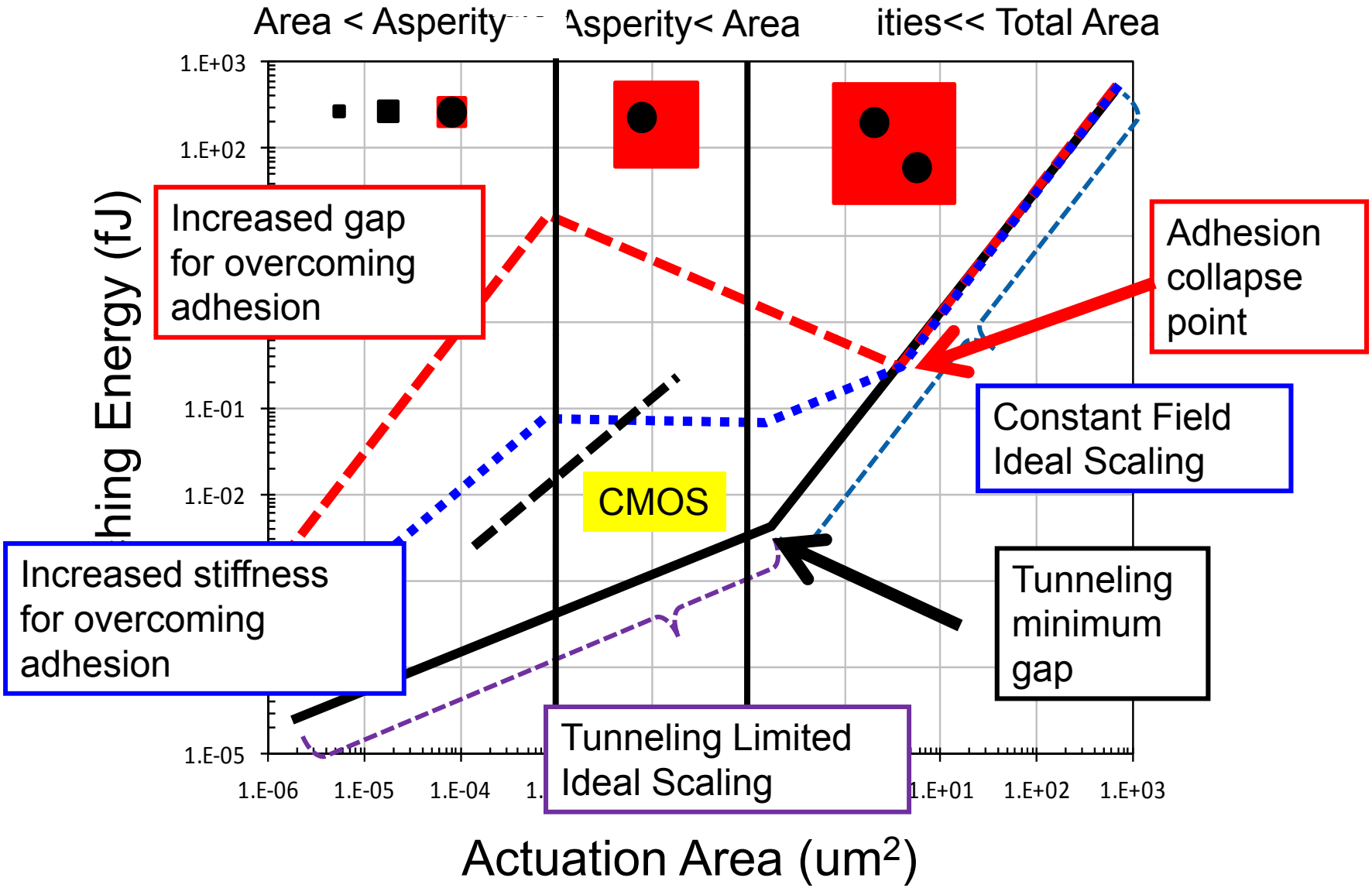




Infinite SS
700 uA/um @1V
Note Hysteresis

The attraction is infinite sub-threshold slope and zero Ioff

NEMS: Scaling Relationships:

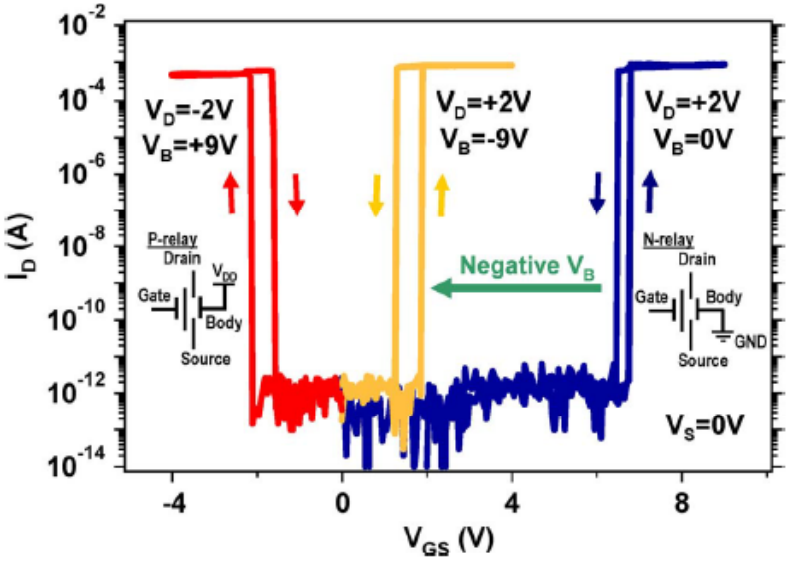


Courtesy Chytra Pawashe / Kevin Lin

NEMS

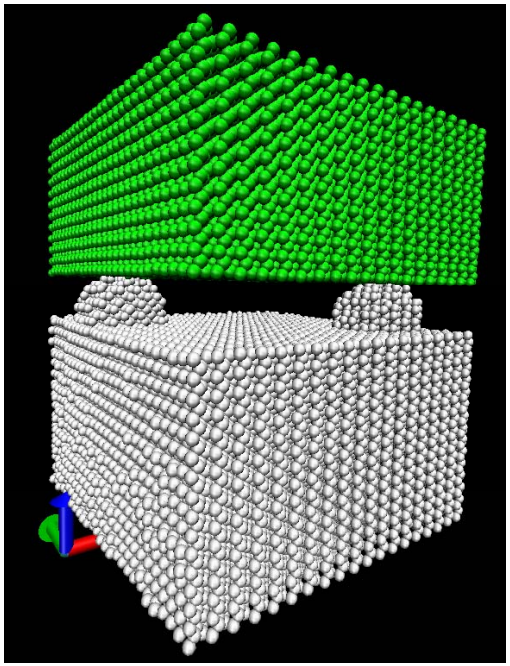
BENEFITS

Nathanael, IEDM 2009

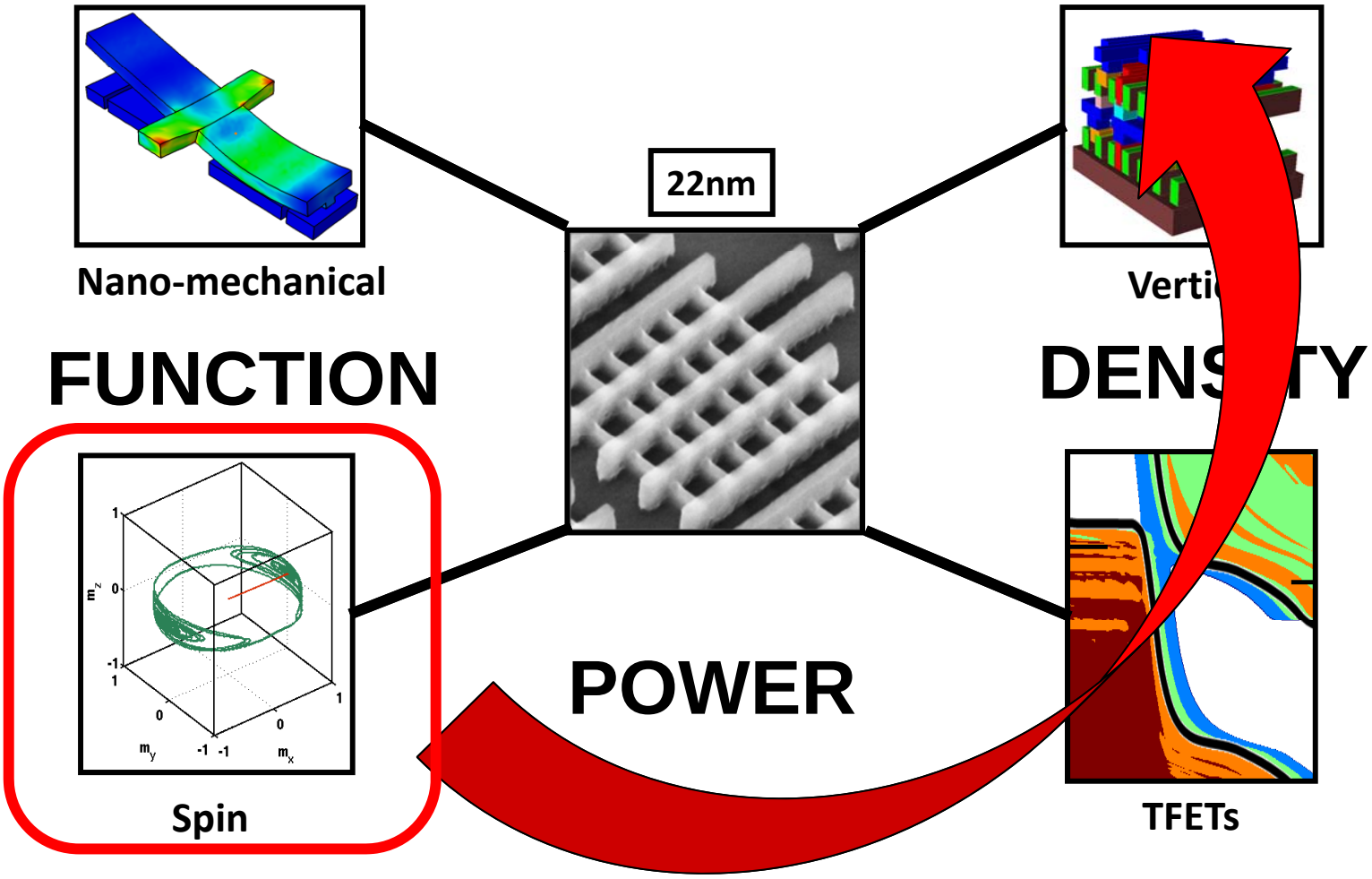


Ideal sub-threshold slope:
Very low Ioff

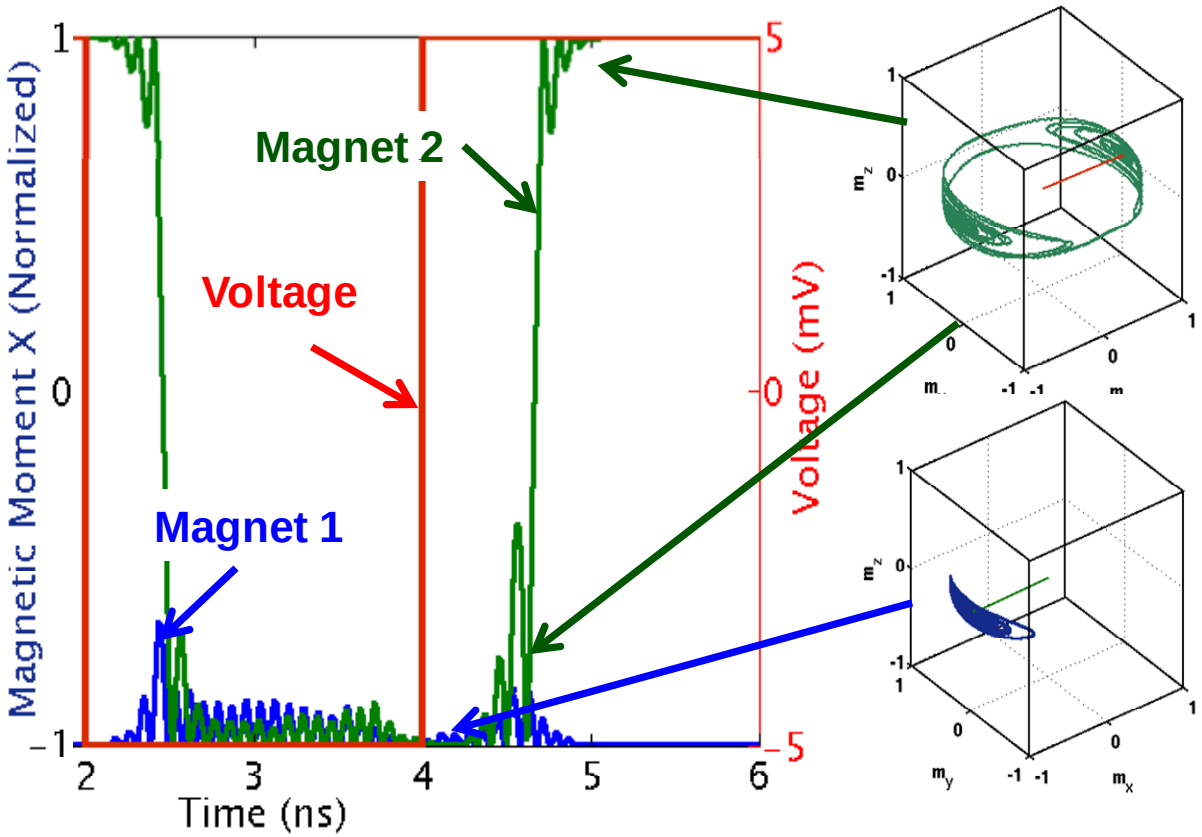
CHALLENGES



Adhesion issues:
For nano-geometries


22nm
Nano-mechanical
FUNCTION
DENSITY
POWER
Spin
TFETs

Spin-Torque Architecture

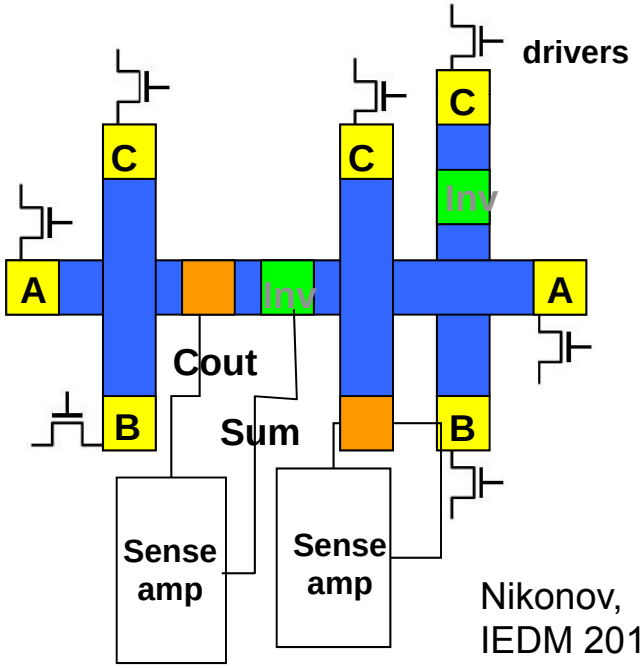


Spin-torque devices use the orientation of the spin of the electron to carry information

Courtesy: Sasikanth Manipatruni / Dmitri Nikonov

Spin Torque Architectures

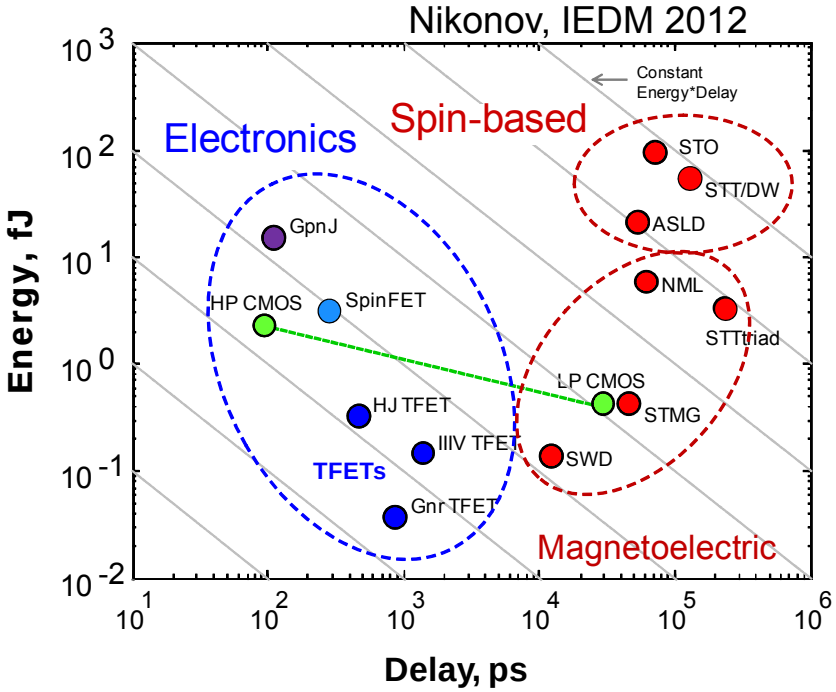
BENEFITS



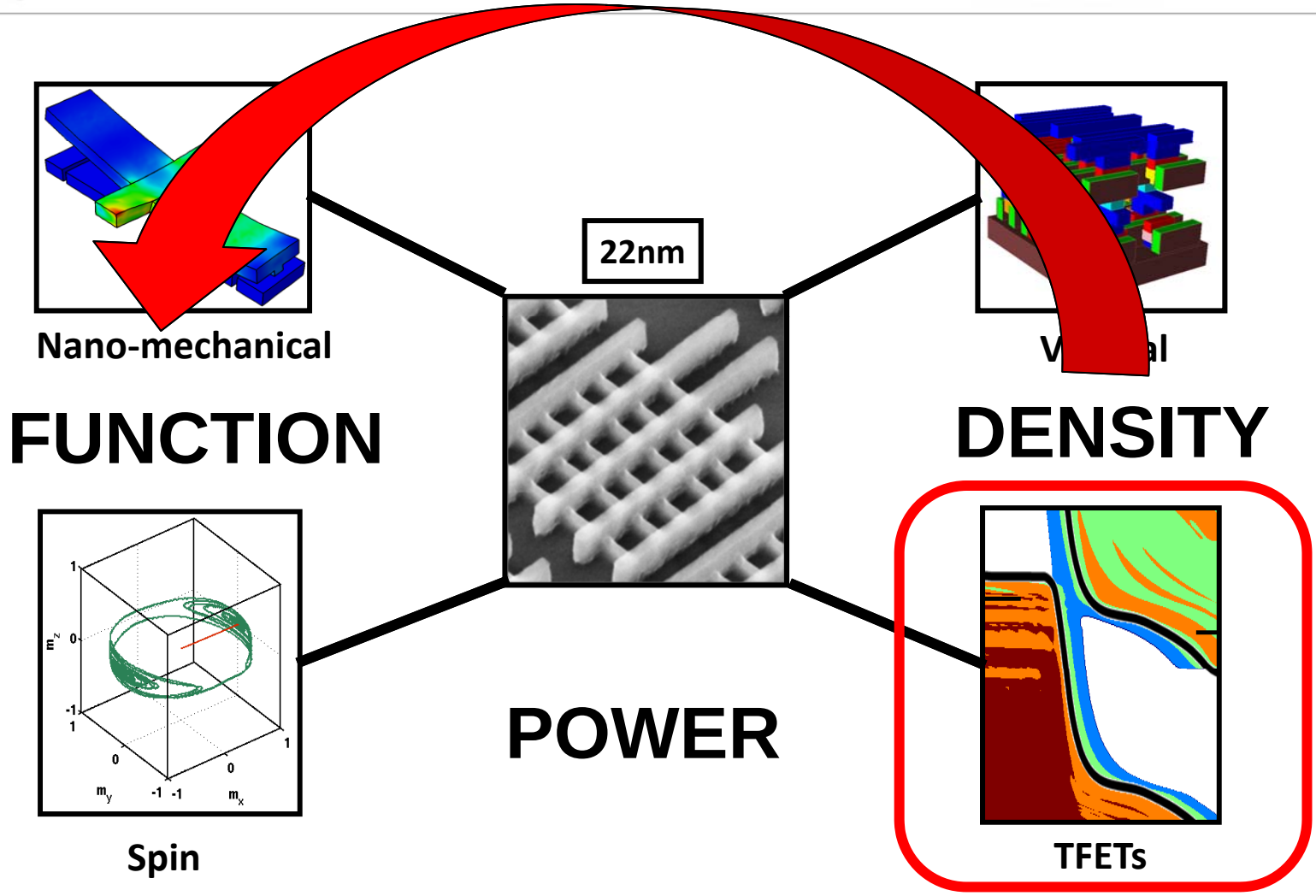
Nikonov, IEDM 2012

Improved area/gate and power vs CMOS

CHALLENGES



Degraded switching time and throughput vs CMOS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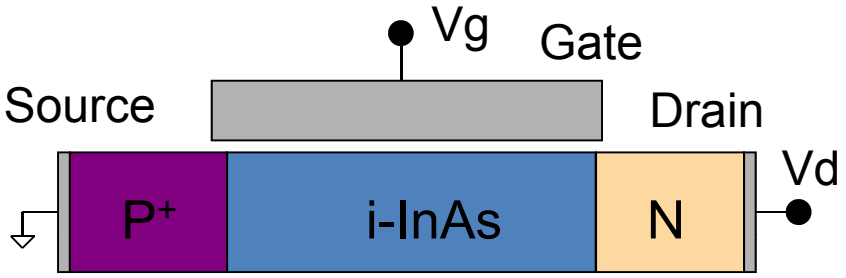
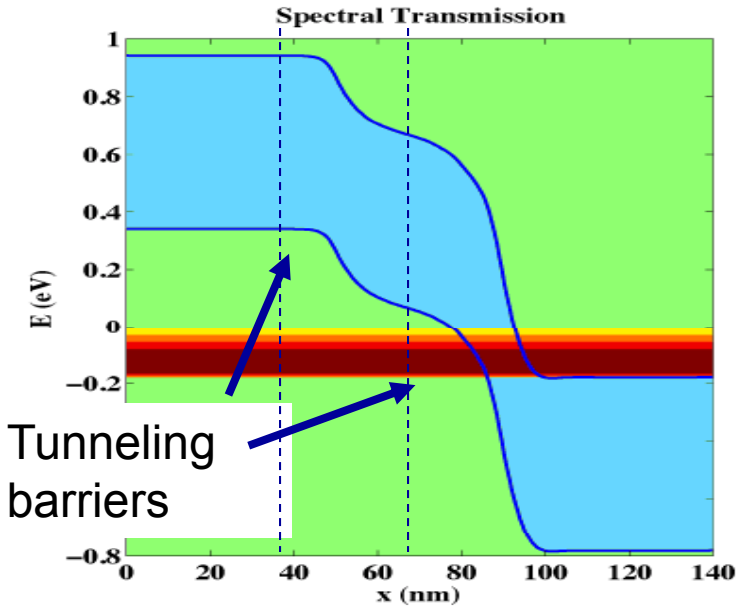
TFET (Tunneling Field-Effect Transistor)





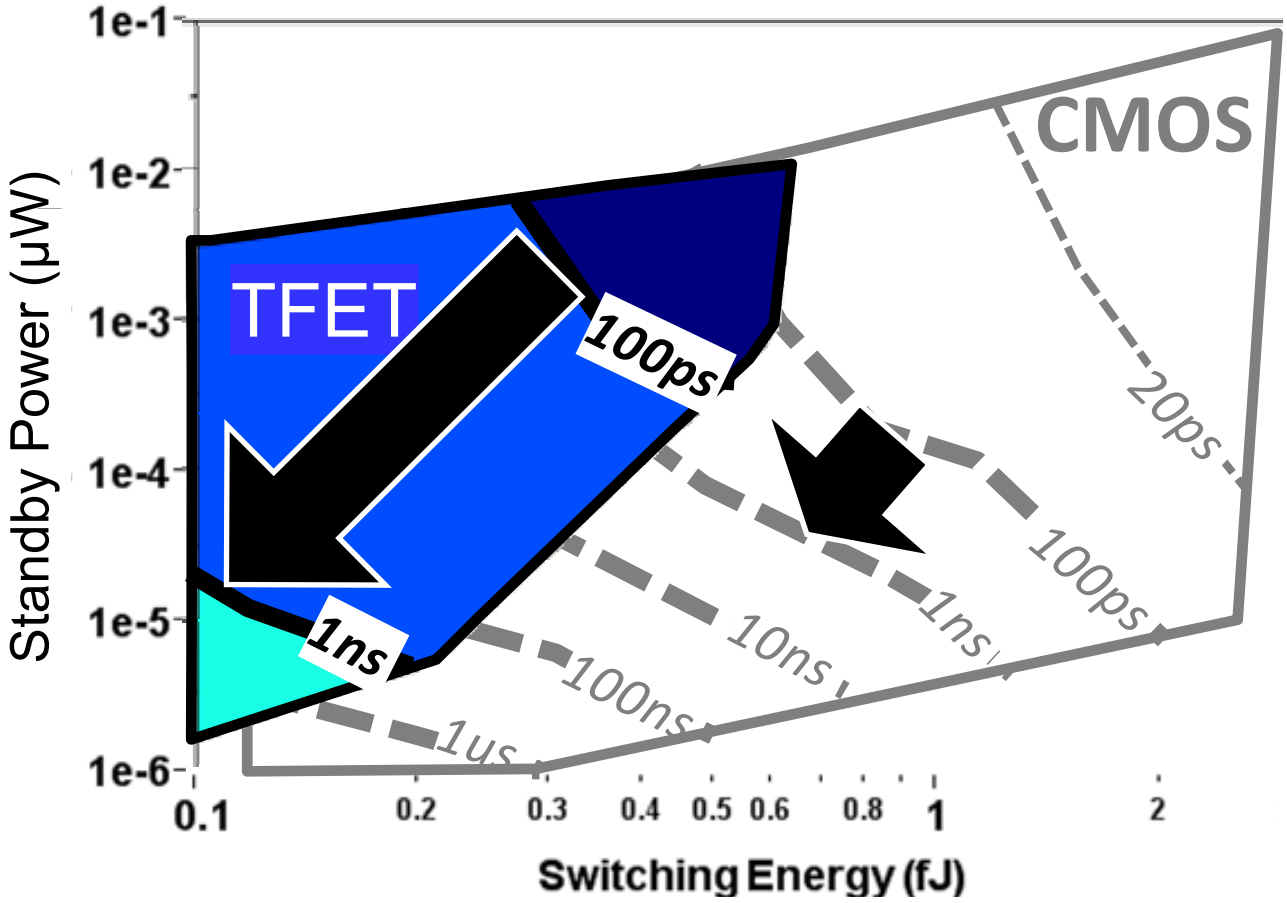
Tunnel FETs operate by tunneling through the S/D barrier rather than diffusion over the barrier

Two required conditions:

- Thin enough barrier over a large enough area for effective (high current) tunneling.
- Sufficient density of states on both the transmission and receiving sides to provide energetic locations for the carriers.

Courtesy: M. Luisier (Purdue), M. Luisier and G. Klimeck, EDL 2009, Uygar Avci, VLSI 2011

TFET vs. MOSFET

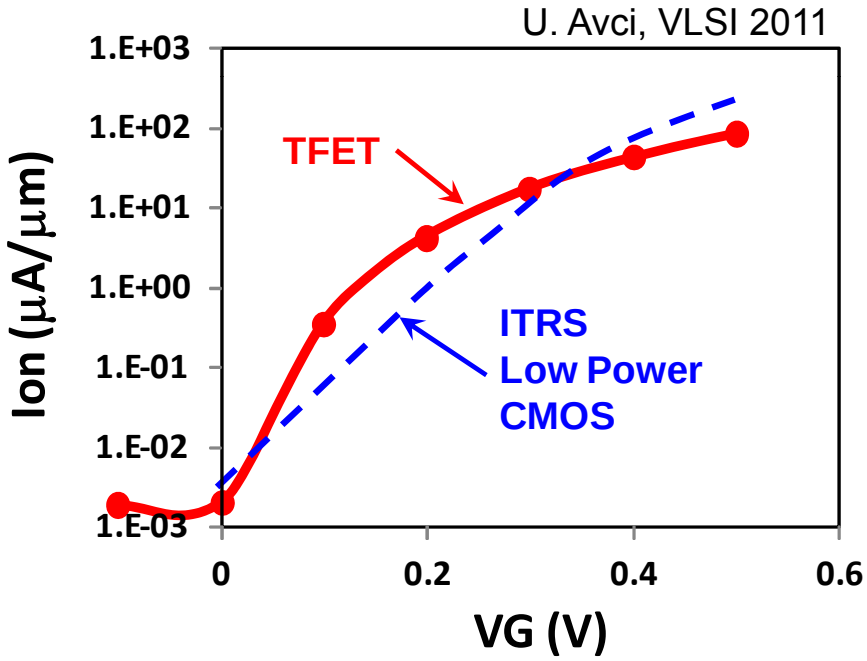


At low switching energy, an InAs TFET is theoretically capable of providing more than 8x performance advantage over MOSFET

U. Avci, VLSI 2011

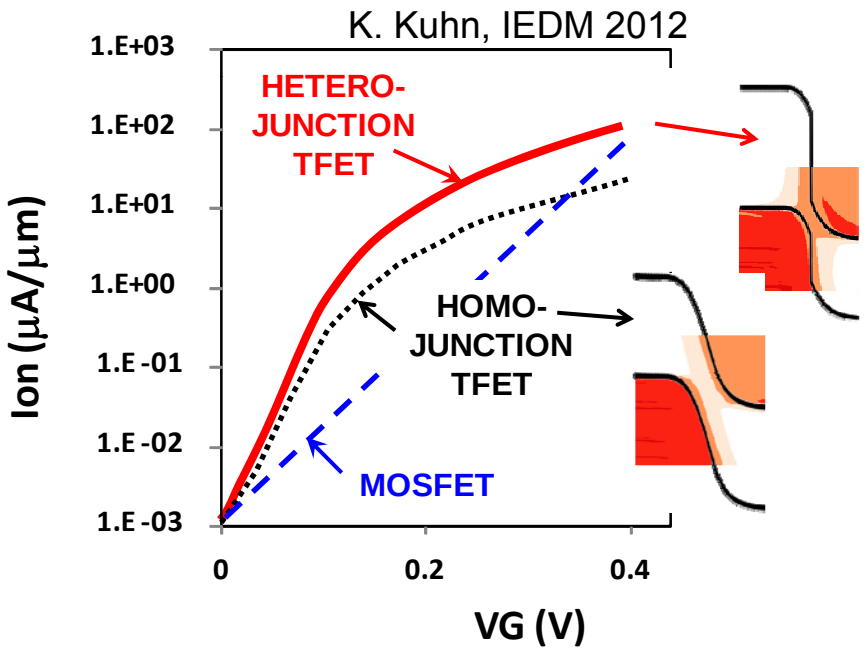
TFET

BENEFITS

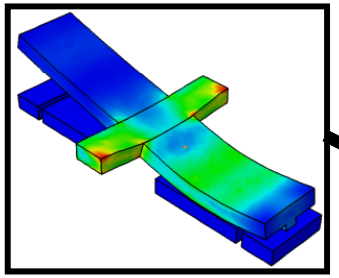


Better sub-threshold slope:
Tunneling through the barrier

CHALLENGES

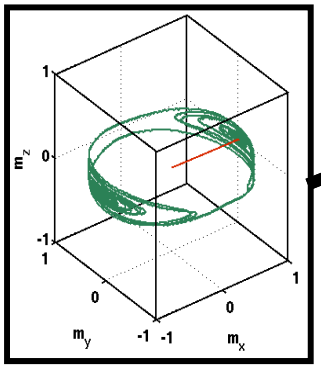


Requires offset bandedges:
Exotic heterostructures



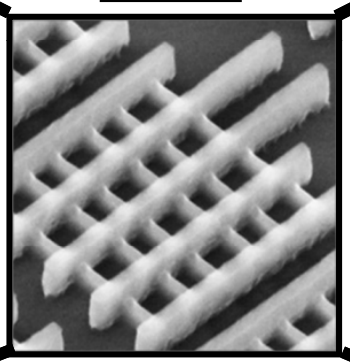
Nano-mechanical

FUNCTION

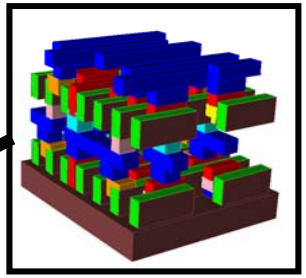


Spin

22nm

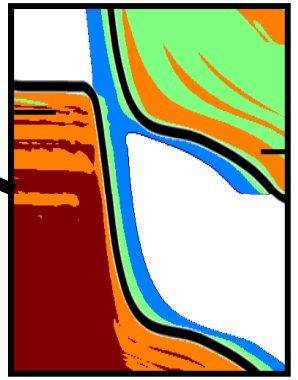


POWER



Vertical

DENSITY

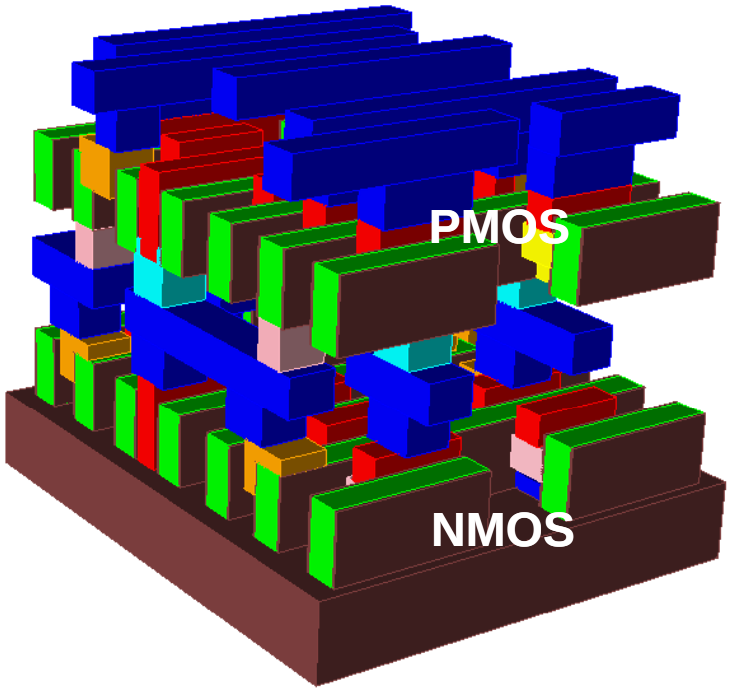


TFETs

Benefits

- **50% reduction in "plan view" density**
- **Vertical orientation may enable new circuit concepts**
- **Possibility for different N/P materials/orientations**

Vertical Device Architectures



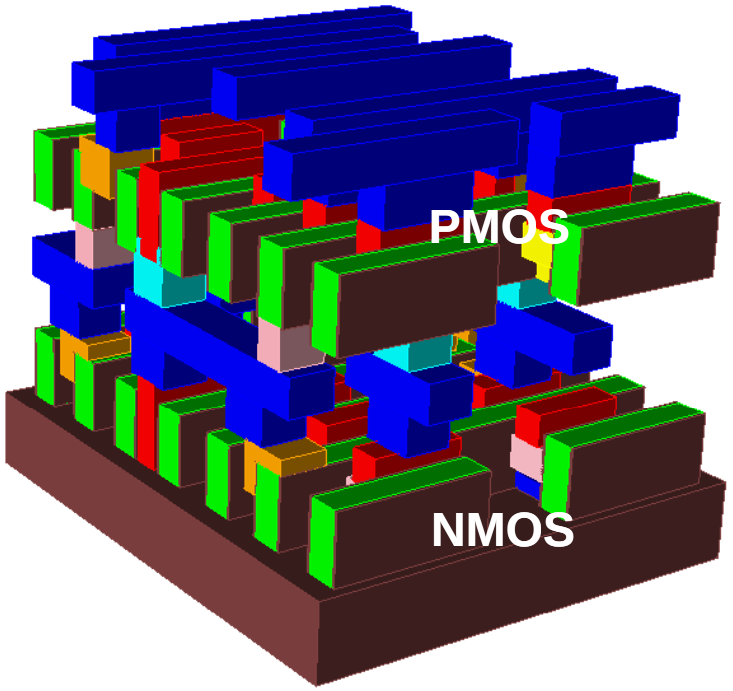
Benefits

- 50% reduction in "plan view" density
- Vertical orientation may enable new circuit concepts
- Possibility for different N/P materials/orientations

Challenges

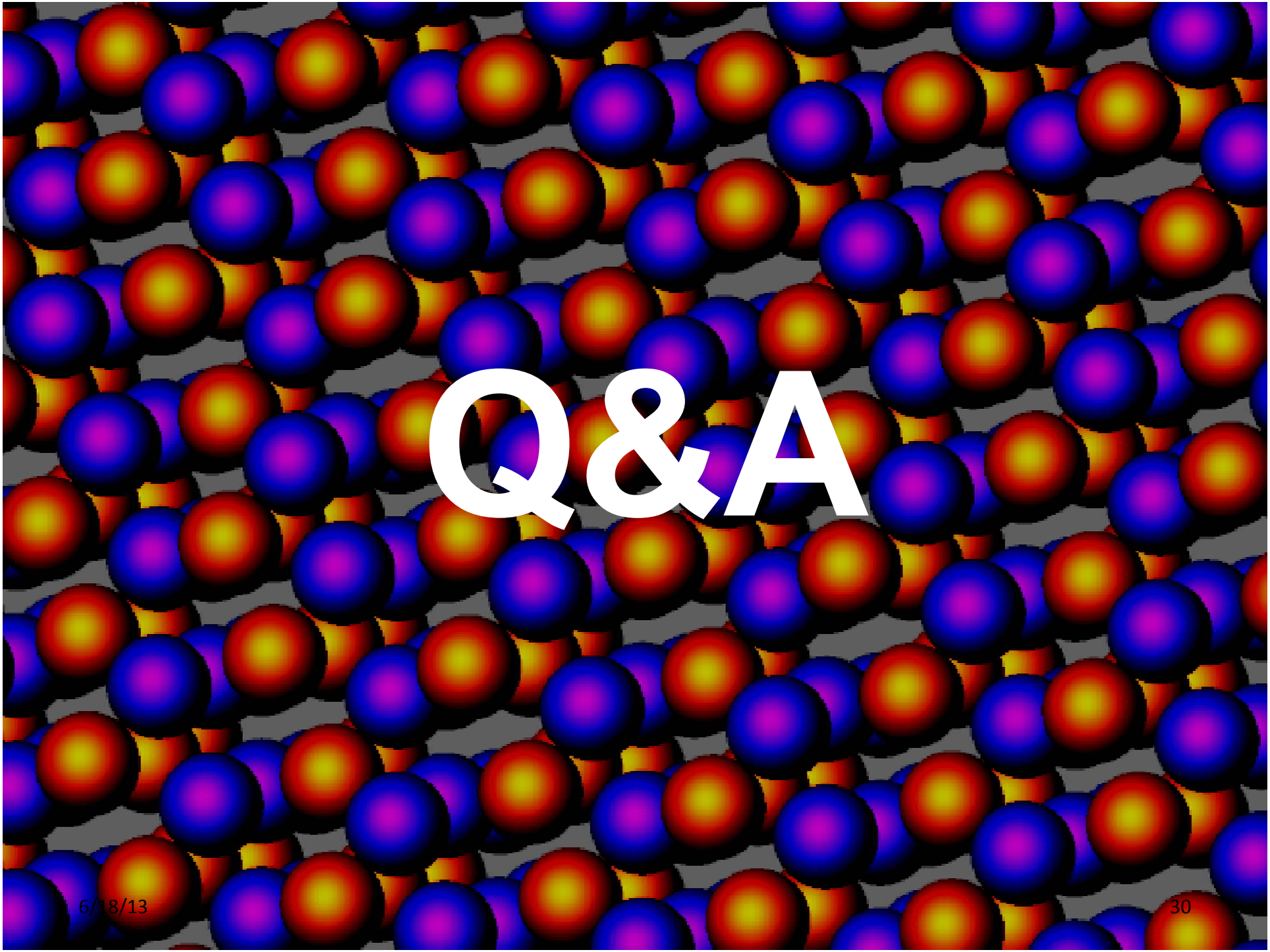
- Lithography (may double the number of FE critical layers)
- Interlayer Contacts (diffusion-diffusion, gate-gate contacts)
- Thermal processing (top layer may need to be processed over existing bottom layer)
- Strain engineering (more challenging than single layer)

Vertical Device Architectures



Messages

- **It's NOT the End of the World**
- **Plenty of Room at the Bottom**
- **Many Creative New Options**


Q&A