Published in *Proc. IEEE,* vol. 87, pp. 606-632, April 1999

Single-Electron Devices and Their Applications

Konstantin K. Likharev
Department of Physics, State University of New York at Stony Brook
Stony Brook, NY 11794-3800
klikharev@ccmail.sunysb.edu

Abstract

The goal of this paper is to review in brief the basic physics of single-electron devices, as well as their current and prospective applications. These devices, based on the controllable transfer of single electrons between small conducting "islands", have already enabled several important scientific experiments. Several other applications of analog single-electron devices in unique scientific instrumentation and metrology seem quite feasible. On the other hand, the prospect of silicon transistors being replaced by single-electron devices in integrated digital circuits faces tough challenges and remains uncertain. Nevertheless, even if this replacement does not happen, single-electronics will continue to play an important role by shedding light on the fundamental size limitations of new electronic devices. Moreover, recent research in this field has generated some exciting by-product ideas which may revolutionize random-access-memory and digital-data-storage technologies.

Keywords *- Single-electron tunneling, Fowler-Nordheim tunneling, single-electron devices, Coulomb blockade, supersensitive electrometry, single-electron spectroscopy, dc current standards, temperature standards, random access memories, floating-gate memories, logic circuits, data storage.*

I. INTRODUCTION: BASIC PHYSICS AND SCALING

The manipulation of single electrons was demonstrated in the seminal experiments by Millikan at the very beginning of the century, but in solid state circuits it was not implemented until the late 1980s, despite some important earlier background work [1-5]. The main reason for this delay is that the manipulation requires the reproducible fabrication of very small conducting particles, and their accurate positioning against external electrodes. The necessary nanofabrication techniques have become available during the past two decades, and have made possible a new field of solid state physics, *single-electronics* (see Refs. 6-8 for its general reviews).

Figure 1 illustrates the basic concept of single-electronics. Let a small conductor (traditionally called an *island*) be initially electroneutral, i.e. have exactly as many (m) electrons as it has protons in its crystal lattice. In this state the island does not generate any appreciable electric field beyond its borders, and a weak external force $\boldsymbol{F}$ may bring in an additional electron from outside. (In most single-electron devices, this injection is carried out by tunneling through an energy barrier created by a thin insulating layer). Now the net charge Q of the island is ($-e$), and the resulting electric field $\boldsymbol{E}$ repulses the following electrons which might be added. Though the fundamental charge $e \approx 1.6\times10^{-19}$ Coulomb is very small on the human scale of things, the field $\boldsymbol{E}$ is inversely proportional to the square of the island size, and may become rather strong for nanoscale

structures. For example, the field is as large as ~140 kV/cm on the surface of a 10-nm sphere in vacuum.

The theory of single-electron phenomena (see the next section) shows that a more adequate measure of the strength of these effects is not the electric field, but the *charging energy*

$$E_c = e^2/C, \qquad (1)$$

where C is the capacitance of the island[1]. When the island size becomes comparable with the de Broglie wavelength of the electrons inside the island, their energy quantization becomes substantial (see, e.g., reviews [10-13]). In this case the energy scale of the charging effects is given by a more general notion, the *electron addition energy* E_a. In most cases of interest, E_a may be well approximated by the following simple formula:

$$E_a = E_c + E_k. \qquad (2)$$

Here E_k is the quantum kinetic energy of the added electron; for a degenerate electron gas $E_k = 1/g(\varepsilon_F)V$, where V is the island volume and $g(\varepsilon_F)$ is the density of states on the Fermi surface.

Figure 2 shows the total electron addition energy as a function of the island diameter, as calculated using Eq. (2) for a simple but representative model. For 100-nm-scale devices which were typical for the initial stages of experimental single-electronics, E_a is dominated by the charging energy E_c and is of the order of 1 meV, i.e. ~ 10 K in temperature units. Since thermal fluctuations suppress most single-electron effects unless

$$E_a \geq 10\, k_B T, \qquad (3)$$

these experiments have to be carried out in the sub-1-K range (typically, using helium dilution refrigerators).

On the other hand, if the island size is reduced below ~10 nm, E_a approaches 100 meV, and some single-electron effects become visible at room temperature. However, most suggested digital single-electron devices require even higher values of E_a (~ 100 $k_B T$) in order to avoid thermally-induced random tunneling events, so that for room temperature operation the electron addition energy E_a has to be as large as a few electron-volts, and the minimum feature size of single-electron devices has to be smaller than ~1 nm (Fig. 2). In this size range the electron quantization energy E_k becomes comparable with or larger than the charging energy E_c for most materials; this is why islands this small are frequently called *quantum dots*. Their use involves not only extremely difficult nanofabrication technology (especially challenging for large scale integration), but also some major physics problems including the high sensitivity of transport properties to small variations of the quantum dot size and shape. This is why it is very important to develop single-electron devices capable of operating with the lowest possible ratio $E_a/k_B T$. As we will see below, some devices may work in the size range where $E_c > E_k$ even at room temperature, thus avoiding complications stemming from the energy quantization effects.

[1] For a *two-electrode* capacitor, the elementary charging energy is of course $e^2/2C = E_c/2$, rather than E_c. However, if a *single* small conductor is charged with electrons from a source kept at a fixed electrochemical potential μ, this is E_c which gives the electrostatic contribution to the energy necessary for the transfer of one additional electron to the conductor: $e\Delta\mu \equiv E_a \approx E_c$ + kinetic energy - see Eq. (2).

The objective of this paper is to give a brief review of the present status of applied single-electronics. I will start with an introduction of the theory of single-electron tunneling (Sec. II). It will allow us to discuss (in Sec. III) the most important single-electron phenomena, devices and circuit components. Analog applications of the devices will be described in Sec. IV, while the prospects of digital applications will be discussed in Sec. V. In the concluding Sec. VI, I will try to summarize my vision of the prospects and problems faced by the field.

Due to the paper length restrictions I will not be able to mention many important contributions to the rapidly growing pool of literature on single-electronics; I am expressing my apology to the authors and hope for their understanding.

II. THEORETICAL BACKGROUND

A. Orthodox Theory

Throughout the history of single-electronics, a unique guiding role has been played by a simple but very effective "*orthodox*" theory which was pioneered (for a particular case) by Kulik and Shekhter [5] and later generalized to other systems - see, e.g., Ref. 7 or Ref. 13 for a detailed review. The theory makes the following major assumptions:

- The electron energy quantization inside the conductors is ignored, i.e. the electron energy spectrum is treated as continuous. Strictly speaking this assumption is valid only if $E_k << k_B T$, but it frequently gives an adequate description of observations as soon as $E_k << E_c$ (cf. Fig. 2).
- The time τ_t of electron tunneling through the barrier is assumed to be negligibly small in comparison with other time scales (including the interval between neighboring tunneling events). This assumption is valid for tunnel barriers used in single-electron devices of practical interest, where $\tau_t \sim 10^{-15}$ s.
- Coherent quantum processes consisting of several simultaneous tunneling events ("*cotunneling*") are ignored. This assumption is valid if the resistance R of all the tunnel barriers of the system is much higher than the quantum unit of resistance R_Q :

$$R >> R_Q, \qquad R_Q = h/4e^2 \approx 6.5\ \text{k}\Omega. \tag{4}$$

The latter relation is of principal importance for single-electronics as a whole.[2]

Despite the limitations listed above, the orthodox theory is in *quantitative* agreement with virtually all the experimental data for systems with metallic conductors (with their small values of the electron wavelength on the Fermi surface, λ_F) and gives at least a qualitative description of most results for most semiconductor structures (where the quantization effects are more noticeable, due to larger λ_F).

---

[2] This field really took off when it was recognized [14, 15] that Eq. (4) ensures the localization of each electron within a particular conducting island of the system at any particular instant. This fact shows that tunnel barriers with low transparency may effectively suppress the quantum-mechanical uncertainty of the electron location. Notice that only this suppression makes controllable single-electron manipulation possible. (In this sense single-electronics *does not* fall into the much advertised category of "quantum electronic devices". Of course, single-electron devices *do* use quantum properties of matter, but so do semiconductor transistors.)

The main result of the theory can be formulated as follows: the tunneling of a single electron through a particular tunnel barrier is always a *random event*, with a certain rate Γ (i.e. probability per unit time) which depends solely on the reduction ΔW of the free (electrostatic) energy of the system as a result of this tunneling event. Within the orthodox theory this dependence may be expressed with a universal formula

$$\Gamma(\Delta W) = (1/e)\, I(\Delta W/e)\, [1 - \exp\{-\Delta W/k_B T\}]^{-1}, \qquad (5)$$

where $I(V)$ is the "seed" dc I-V curve of the tunnel barrier in the absence of single-electron charging effects. (In many cases, the Ohmic approximation $I(V) = V/R$ is quite acceptable.) ΔW may be readily found from the system's electrostatics; a few simple examples will be considered below. Frequently the following general expressions are rather useful:

$$\Delta W = e(V_i + V_f)/2, \qquad (6a)$$

or

$$\Delta W = e(V_i - V_t), V_t \equiv e(C^{-1})_{kl} - e[(C^{-1})_{kk} + (C^{-1})_{ll}]/2, \qquad (6b)$$

where V_i and V_f are voltage drops across the barrier before and after the tunneling event, respectively, while $\boldsymbol{C}^{-1}$ is the reciprocal capacitance matrix of the system, and k and l are the numbers of the islands separated by this particular barrier.

Figure 3a shows the dependence given by Eq. (5); at low temperatures ($k_B T << \Delta W$) only tunneling events decreasing the electrostatic energy (and dissipating the difference) are possible, and their rate is proportional to ΔW. The latter fact is easy to comprehend: an increase in applied voltage increases the number of electron states in the source electrode which may provide an electron capable of tunneling into an empty state of the drain electrode.

Though Eqs. (5) and (6) are rather simple, the calculation of properties of even some basic single-electron systems runs into a technical problem: in many situations, several tunneling events are possible at the same time, and the orthodox theory only gives the chances of a particular outcome. Hence, some sort of statistical calculation scheme becomes inevitable. For systems with relatively few islands, i.e. with a limited set of possible charge states $\{i\}$, Eq. (5) may be plugged into the system of "master" equations [5, 14, 15]:

$$dp_i/dt = \sum_j (\Gamma_{j \to i}\, p_j - \Gamma_{i \to j}\, p_i) \qquad (7)$$

describing the time evolution of probability p_i of each state. After this system has been solved, the probabilities p_i may be used for a straightforward calculation of average values and fluctuations of any variable. A nice example of the implementation of this approach is the series of computer programs SETTRANS for the fast calculation of dc I-V curves and white noise of single-electron transistors, created by A. Korotkov.[3]

For more complex systems the multi-dimensional space of all possible charge states may become too large, and the only practical method is to simulate the random dynamics of the system by a Monte Carlo method [16]. In this procedure, Eq. (5) is used to establish the correct statistics of the randomly generated events. After a sufficient number of implementations have been

[3] MS-DOS versions of these programs are available via anonymous ftp from the site hana.physics.sunysb.edu/pub/settrans/dos.

accumulated, variables of interest may be evaluated by averaging over this ensemble. Several programs of this type have been developed by various research groups. Of those publicly available, SIMON developed by C. Wasshuber and his collaborators at the Technical University of Vienna, Austria [17] features a graphical user interface and also allows an approximate account of cotunneling.[4] On the other hand, MOSES developed by R. Chen and collaborators at Stony Brook[5] only has a text interface and is limited to the orthodox theory, but allows a broader range of circuit elements and analyses. The currently available version 1.1 of MOSES is also considerably faster than the available version 1.3 of SIMON [18]. In certain cases, a combination of both numerical methods may be useful [19].

B. Effects Beyond the Orthodox Theory

Experiments with single-electron devices have indicated several features which are not accounted for by the orthodox theory. In non-superconducting systems, the most important effects are:

1). *Cotunneling*. This effect was first predicted in 1989 [20] and observed experimentally soon after [21] (for a review, see Ref. 50). The essence of the effect is that the tunneling of several (N>1) electrons through different barriers at the same time is possible as a single coherent quantum-mechanical process. The rate of this process is crudely $(R_Q/R)^{N-1}$ times less than that for the single-electron tunneling described by Eq. (5) of the orthodox theory. If the condition expressed by Eq. (4) is satisfied, this ratio is rather small; cotunneling can nevertheless be clearly observed within the Coulomb blockade range where orthodox tunneling is suppressed - see Sec. III below.

2). *Discrete Energy Levels*. For very small islands, the quantum splitting E_k between electron energy levels may become larger than E_c and k_BT (see Fig. 2 and its discussion in Sec. I). The generalization of the orthodox theory to this case has been carried out by Averin and Korotkov [23] who considered a situation where tunneling is only possible between islands with discrete levels and larger electrodes where electrons still have a continuous spectrum. They have shown that if the tunneling barriers are not extremely thin, i.e. their seed tunneling rate Γ_0 is not too large ($\hbar\Gamma_0 < k_BT$), the situation may again be described with master equations similar to Eq. (7) of the orthodox theory, but with a different energy dependence of the tunneling rate to/from a certain quantum level:

$$\Gamma(\Delta W) = \Gamma_0 [1 + \exp\{-\Delta W/k_BT\}]^{-1}. \qquad (8)$$

This dependence (Fig. 4a) repeats (and results from) the Fermi distribution of electrons in the bulk electrode. (In fact, the orthodox rate (5) may be obtained as a sum of the rates (8) over all the levels of a continuous spectrum of the island). Another difference is that the summation in the master equations should be extended over two indices: one for the total number of electrons (as in Eq. (7)), and another for the electron distribution between the energy levels, at a fixed number of electrons. This makes the solution to master equations more complex.

[4] Information on the distribution of SIMON can be found on the Web site http://members.magnet.at/catsmeow/.

[5] MOSES 1.1 is available in both MS-DOS and UNIX versions via anonymous ftp from the site hana.physics.sunysb.edu/pub/moses.

If the system has more than one quantum dot, tunneling between them may become important. If the energy loss effects are not too significant, this tunneling leads only to coherent hybridization of the quantum dot levels, similar to that well studied in atomic and molecular physics. Inelastic tunneling from an island to bulk electrodes, described by Eq. (8), may bring a substantial dissipation into this system and suppress the system coherence - see, e.g., experiments [24-26] with "artificial molecules", and review [12].

In general, energy quantization effects have not yet led to suggestions for any new practical applications, with the exception of single-electron spectroscopy (Sec. IV.B) which is still limited to fundamental physics studies, and some highly controversial logic device proposals (Sec. V.B). This is why a review of single-electron devices can be based mostly on the predictions of the orthodox theory.

III. BASIC SINGLE-ELECTRON DEVICES

Let us start with a discussion of cases in which single-electron charging effects do *not* appear. First, consider a tunnel junction with a *fixed voltage V* across it ($V_i = V_f = V$). Here, for two possible directions of electron tunneling, Eq. (6) yields $\Delta W = \pm eV$, and according to Eq. (5) the net current is $I = e \times [\Gamma(eV) - \Gamma(-eV)] = I(V)$, i.e. we have come back to the seed dc *I*-*V* curve. This is natural, since in this system a single-electron tunneling event does not change *V*, i.e. the single-electron charge quantization does *not* lead to any noticeable effects,[6] even if the junction size is very small. A possible way to describe the same fact is to say that the large stray capacitance of the external electrodes leading to the junction adds up to the junction capacitance (however small), so that the total capacitance *C* does not satisfy the condition (3).[7]

Even more importantly, the orthodox theory predicts that the effects of single-electron discreteness may be ignored in *any* solid state device which does not have small conducting islands separated from the external electrodes by sufficiently high tunnel barriers. (The quantitative criterion of the notion "high barrier" is provided by Eq. (4)). The most important practical example may be a small-size MOSFET which does not exhibit any immediate single-electron effects even if the average number of carriers in its channel is smaller than one, since in these devices the channel-contact resistance is typically much lower than R_Q. The physical interpretation of this fact is that in systems without sufficiently high tunnel barriers the electron wavefunctions are well extended, and electrons cannot be treated as classical, localized particles.

Now let us turn to situations in which the single-electron charging effects *do* appear.

A. Single-Electron Box

Figure 5a shows the conceptually simplest device, the "*single-electron box*".[8] The device consists of just one small island separated from a larger electrode ("*electron source*") by a tunnel

---

[6] Besides shot noise which appears at $eV/2 > k_BT$.

[7] More detailed analysis [14, 15] shows that even if the stray capacitance is carefully eliminated, the single-electron charging effects would not show up, because the lead impedance $Z(\omega)$ is typically much less than the quantum unit of resistance (4), and as a result, quantum fluctuations of the environment smear out the charging effects. A quantitative theory of this smearing has been developed by Nazarov [27]. (A simpler derivation of the same result was given by Devoret *et al*. [28]; see also the review [13].)

barrier. An external electric field may be applied to the island using another electrode ("*gate*") separated from the island by a thicker insulator which does not allow noticeable tunneling. The field changes the electrochemical potential of the island and thus determines the conditions of electron tunneling. Elementary electrostatics shows that the free (Gibbs) energy of the system may be presented as

$$W = Q^2/2C_\Sigma + (C_0/C_\Sigma)QU + \text{const}, \qquad (9)$$

where $Q = -ne$ is the island charge (n is the number of uncompensated electrons), C_0 is the island-gate capacitance, while C_Σ is the total capacitance of the island (including C_0). Usually, this expression is re-written as

$$W = (ne - Q_e)^2/2C_\Sigma + \text{const}, \qquad (10)$$

where parameter Q_e, which is defined as

$$Q_e \equiv UC_0, \qquad (11)$$

is usually called the "*external charge*". The physical sense of this definition only becomes apparent for the case when the electric field between the gate and island is well localized (Fig. 5b); then ($-Q_e$) is just the polarization charge of the island which is bound by the gate field and is thus taken out of the energy balance of the tunnel junction.

From the definition (9) it is evident that in contrast with the discrete total charge of the island, the variable Q_e is *continuous*, and may be a fraction of the elementary charge e. At low temperatures Eq. (5) shows that the single-electron tunneling merely minimizes W; an elementary calculation using Eq. (10) shows that Q is a step-like function of Q_e, i.e. of the gate voltage (Fig. 5c), with a fixed distance between the neighboring steps:

$$\Delta Q_e = e, \qquad \Delta U = e/C_0 = \text{const}. \qquad (12)$$

If the temperature is increased to $k_BT \sim E_c$, this "*Coulomb staircase*" is gradually smeared out by thermal fluctuations.

The physics of the Coulomb staircase is very simple: increasing gate voltage U attracts more and more electrons to the island. The discreteness of electron transfer through low-transparency barriers necessarily makes this increase step-like. This is all very natural and apparently trivial. What *is* surprising is that even such a simple device allows a reliable addition/subtraction of single electrons to/from an island with an enormous (and unknown) number of background electrons, of the order of 1 million in typical low-temperature experiments with 100-nm-scale aluminum islands. This is of course simply a consequence of the enormous strength of the unscreened Coulomb interaction, which has already been discussed in Sec. I.

Notice, however, two major drawbacks of the single-electron box as an electronic circuit component. First, it does not have internal memory: the number n of the electrons in the box is a unique function of the applied voltage U, so that this structure cannot be used for information

---

[8] The basic properties of this system were well understood by Lambe and Jaklevic [4] in the context of their experiments with granular tunnel structures, while its quantitative theory was given by Kulik and Shekhter [5]. Experimentally, however, the properties of a single device were not measured until 1991 [29].

storage. The second problem is that the box cannot carry dc current, so that an ultrasensitive electrometer is necessary to measure its charge state - see, e.g., Ref. 29.

B. Single-electron Transistor

The latter drawback may be easily corrected by splitting the tunnel junction of the single-electron box and applying a dc voltage V between the two, now separate, parts of the external electrode (Fig. 6a). The resulting "*single-electron transistor*"[9] is probably the most important device in this field. The device is reminiscent of a usual MOSFET, but with two tunnel barriers embedded in a small conducting island, instead of the usual inversion channel.

The expression for the electrostatic energy W of the system

$$W = (ne - Q_e)^2/2C_\Sigma - eV[n_1C_2 + n_2C_1]/C_\Sigma + \text{const} \qquad (13)$$

is an evident generalization of Eq. (5). Here n_1 and n_2 are the number of electrons passed through the tunnel barriers 1 and 2, respectively, so that $n = n_1 - n_2$, while the total island capacitance C_Σ is now a sum of C_0, C_1, C_2, and whatever stray capacitance the island may have. The external charge Q_e is again defined by Eq. (11) and is just a convenient way to present the effect of the gate voltage U.

Figure 6b shows typical dc I-V curves of this system. At small source-drain voltage V there is no current, since any tunneling event would lead to an increase of the total energy ($\Delta W < 0$) and hence according to Eq. (5) at low enough temperatures ($k_BT << E_c$) the tunneling rate is exponentially low. (Cotunneling provides in this region a weak current proportional to R_Q^2/R_1R_2 [20, 21], where $R_{1,2}$ are the tunnel barrier resistances; as far as $R_{1,2} >> R_Q$, this current is small.) This suppression of dc current at low voltages is known as the *Coulomb blockade*.[10]

At a certain *threshold voltage* V_t the Coulomb blockade is overcome, and at much higher voltages the dc I-V curve gradually approaches one of the offset linear asymptotes: $I \to (V + \text{sign}(V)\times e/2C_\Sigma)/(R_1+R_2)$. On its way, the I-V curve exhibits quasi-periodic oscillations of its slope, closely related in nature to the Coulomb staircase in the single-electron box, and expressed especially strongly in the case of a strong difference between R_1 and R_2.

The most important property of the single-electron transistor is that the threshold voltage, as well as the source-drain current in its vicinity, is a periodic function of the gate voltage, with the period given by Eq. (12). This periodicity is evident from Eqs. (10) and (13): if U is changed by $\Delta U = e/C_0$, Q_e changes by e, and may be exactly compensated for by one of the electrons tunneling into/from the island. The physical reason for this periodic dependence U (the so-called "*Coulomb blockade oscillations*") is clear from Figs. 5b and 6a: the effect of the gate voltage is equivalent to the injection of charge $Q_e = C_0U$ into the island and thus changes the balance of the charges at tunnel barrier capacitances C_1 and C_2, which determines the Coulomb blockade threshold V_t. In the orthodox theory, the dependence V_t (U) is piece-linear and periodic (Fig. 6c).

The first successful experimental implementation of the single-electron transistor was carried out by Fulton and Dolan [31], using a relatively simple technique in which two layers of

[9] It was invented in 1985 [15, 30], on the background of the earlier work on double-junction systems without the gate [3, 5] and on a similar Cooper-pair system [14].

[10] This term was introduced in Ref. 15, but the phenomenon itself had been qualitatively understood much earlier, initially for different systems - see, e.g., Refs. 1, 2.

aluminum are evaporated *in-situ* from two angles through the same suspended mask formed by direct e-beam writing. (This technique, pioneered by G. Dolan [32], has become standard for 100-nm-scale metallic single-electron devices.) Since then single-electron transistors have been demonstrated in numerous experiments using a wide variety of device geometries, materials, and techniques. Of course some of the methods used may be more suitable for future integrated circuit fabrication than others (right now, *none* of them is fast or reproducible enough for VLSI applications). Unfortunately, the paper length restrictions do not allow me to go into any detailed analysis and critical comparison of these techniques, so I will only mention the most important recent trend.

Over the past few years there has been rapid progress in the fabrication of the first transistors with 10-nm-scale islands, with electron addition energies above 10 mV - see Refs. 33-45 and Table 1. The most advanced of these devices, with E_a beyond ~100 meV, exhibit noticeable Coulomb blockade oscillations at room temperature.[11]

Table 1. Some high-E_a single-electron transistors.

Materials (Island; Barrier)	Fabrication Method	Highest E_a (meV)	Ref.
Al; AlO_x	Evaporation through an e-beam-formed mask	23	[39]
CdSe; organics	Nanocrystal binding to prepatterned Au electrodes	60	[44]
Al; AlO_x	Evaporation on a Si_3N_4 membrane with a nm-scale orifice	92	[42]
Ti; Si	Metal deposition on prepatterned silicon substrates	120	[43]
Carboran molecule	E-beam patterned, thin-film gate; STM electrode	130	[40]
Si; SiO_2	E-beam patterning + oxidation of a SIMOX layer	150	[37]
Nb, NbO_x	Anodic oxidation using scanning probe	1,000	[45]

As the transistor island becomes smaller, the effects of energy quantization may become important. The application of the double-index master equations to the single-electron transistor shows that its dc *I-V* curves may be quite complex [50]. However, the situation at small source-drain voltage is much simpler. In fact, Fig. 6c shows that on each period of the Coulomb blockade oscillations there is one special point $Q_e = e(n + 1/2)$, at which the Coulomb blockade is completely suppressed, and the *I-V* curve has a finite slope at low voltages Fig. 6b). Another way to express the same property is to say that the linear conductance $G \equiv dI/dV_{|V=0}$ of the transistor as a function of the gate *U* voltage exhibits sharp peaks. Theory shows that even if the electron quantization effects are substantial, the peak position may be found from a very natural "resonance tunneling" condition [9, 50, 51]: an energy level inside the island (with the account of the gate field potential) should be aligned with the Fermi levels in source and drain, which coincide at $V \to 0$. This rule yields a simple equation for the gate voltage distance between the neighboring Coulomb blockade peaks:

$$\Delta U = (C_\Sigma / C_0)\, E_a/e. \qquad (14)$$

[11] Several high E_a values recorded for bare double-junction systems (without a gate) should also be mentioned [46-49].

If the charging effects dominate ($E_c >> E_k$) this relation is reduced to Eq. (12) of the orthodox theory, but at strong quantization ($E_k >> E_c$) the distance between the Coulomb blockade oscillation peaks, as well as the height G_{max} of the peaks, may vary from level to level.

C. Single-electron Trap

A different generalization of the single-electron box (Fig. 5a) may be obtained by replacing the single tunnel junction with a one-dimensional array of $N > 1$ islands separated by tunnel barriers (Fig. 7a).[12] The main new feature of this system is its *internal memory* (bi- or multistability): within certain ranges of applied gate voltage U the system may be in one of two (or more) charged states of its edge island.

The reason for this multistability is as follows: due to electric polarization effects an electron located in one of the islands of the array extends its field to a certain distance [16, 55]. In terms of the island numbers, this distance is of the order of

$$M = (C/C_0)^{1/2}, \qquad (15)$$

where C_0 is the effective stray capacitance of the island, while C is the mutual capacitance between the neighboring islands (usually dominated by that of the tunnel junction). This *"single-electron soliton*" interacts with the array edges (is attracted to them) at a distance of the order of M. As a result, the electrostatic self-energy of the soliton has a maximum

$$W_{max} \approx (e^2/2C)\times\min(M, N/4) \qquad (16)$$

somewhere in the middle of the array (see the middle trace in Fig. 7b). By applying sufficiently high gate voltage $U = U_+$ the energy profile may be tilted enough to drive an electron into the edge island; if the array is not too long ($N \le M$), other electrons feel its repulsion and do not follow. If the gate voltage is subsequently decreased to the initial level, the electron is trapped in the edge island, behind the energy barrier. In order to remove the electron from the trap, the voltage has to be reduced further, to $U_- < U_+$ (the upper trace in Fig. 7b). As a result, the $n(U)$ dependence exhibits regions of bi- or multi-stability, in which the charge state of the trap depends on its prehistory (Fig. 7c).

The lifetime of a certain state within the multi-stability region is fundamentally limited by the thermal activation over the energy barrier, and cotunneling [20, 56]. The first effect is exponentially low in E_c/k_BT (see Eq. (5) and its discussion), while the second effect falls exponentially with the array length N [48, 51]. As a result, electron retention time may be very long [56].

After several preliminary attempts [52, 57], single-electron traps with retention time of at least 12 hours (limited only by the observation time) were successfully demonstrated [58] at low temperatures. Their quantitative characteristics were found [59] to be close to the theoretical predictions, with allowance for the uncertainties of island geometry and randomness of background charge (see Sec. IV.C below). Later similar experiments were carried out by another group [60].

D. Single-electron Turnstile and Pump

[12] To my knowledge, this device was first discussed in 1991 [52, 53], but in fact it may be considered just a particular operation mode of the single-electron turnstile (see Sec. D below) which was invented earlier [54].

Combining both generalizations of the single-electron box, described in Sec. C and D, we naturally arrive at the device shown in Fig. 8a. This "*single-electron turnstile*" was suggested and demonstrated by a French-Dutch collaboration in 1990 [54]. At $V = 0$, the device operates exactly like the single-electron trap: one electron may be pulled into the central island (at random, from either source or drain) increasing the gate voltage U beyond a certain threshold; then it may be pushed out by decreasing U. The application of a modest drain-source bias $V \neq 0$ breaks the source-drain symmetry: now an electron is always picked up from the source when U goes up and delivered to the drain when U goes back down. If the gate voltage is cycled periodically, one electron is transferred from source to drain each period.

The latter function may be performed even better by another device, the "*single-electron pump*" ([61], Fig. 8b). Here rf waveforms $U_i(t)$ applied to each gate electrode are phase-shifted forming a potential wave gliding along the island array. This wave picks up an electron from the source and carries it down to the drain in very much the same way that the charge-coupled devices (see, e.g., Ref. 62) transfer multi-electron bundles. Notice that this device does not need dc source-drain voltage: the direction of the transferred electron is determined by that of the running wave of electric potential.

E. SET Oscillators

Much of the initial excitement around single-electron tunneling was induced by the prediction [15] that it could be used to generate narrowband oscillations with a frequency fundamentally proportional to dc current:

$$f_{SET} = I/e. \tag{17}$$

Conceptually, the simplest system capable of proving these "*SET*" (from "single-electron tunneling") oscillations may be formed from a single-electron box (Fig. 5a) by replacing the capacitance C_0 with an Ohmic resistor R_s that satisfies the following requirement:

$$R_s >> R >> R_Q. \tag{18}$$

Figure 9a shows the resulting simple device, while Fig. 9b illustrates its dynamics. Theory says that SET oscillations should arise as soon as applied dc voltage V exceeds the Coulomb blockade threshold $V_t = e/2C$ and gradually disappear in background shot noise at $I \geq 0.1e/RC$. Experimental implementation of this device is not, however, easy for the following reason.

The theory of SET oscillations implies that what we call the Ohmic resistor provides a *continuous* transfer of charge, i.e. is capable of transferring sub-single-electron amounts of electricity in order to recharge the island capacitance in time intervals between the subsequent tunneling events (Fig. 7b). This assumption, though seemingly counterintuitive, is supported by the observation that the macroscopic diffusive conductors do not exhibit shot noise at voltages $V > k_B T/e$, as should happen at the discrete transfer of electrons (and as really happens, e.g., in tunnel junctions). The theoretical explanation of the continuous conduction in such conductors is based on the extended character of the electron - see, e.g., Ref. 7. For the implementation of a narrowband SET oscillator, however, the Ohmic resistor has to combine the continuous transfer of charge with very high resistance (~1 MΩ or higher) and very small stray capacitance ($\sim C << e^2/k_B T$).

After a decade-long effort by several groups [63-69], this goal has been only partly met: continuous transport was demonstrated in ultra-thin-film strips with specific resistance up to about

10 kΩ/μm, i.e. $R_s \sim 10^5$ Ω for 10-μm-scale length which gives a still acceptable capacitance for sub-1-Kelvin experiments. The resulting range R_s/R_Q is too small to satisfy the strong conditions (18); this is why only questionable evidence of SET oscillations in a single-junction system has been obtained [64]. (The SET oscillations with frequency expressed by Eq. (17) were observed more reliably although indirectly [70] in 1D junction arrays which may provide quasi-sub-electron transport of charge [16, 71].)

F. Superconductor Systems

In systems with superconducting electrodes the single particle charging effects may be more complicated. What follows is a list of the major new features:

1). The seed dc *I-V* curve of a single junction, which participates in Eq. (5), may be very nonlinear even at small (millivolt - scale) voltages, due to superconducting energy gap Δ in the density of states - see, e.g., Chapter 3 of Ref. [72]. In particular, due to this feature, the charge sensitivity of single-electron transistors with superconducting electrodes may be considerably better than in the normal state [73].

2). If a superconducting island has an even total number of electrons, at low temperatures ($k_BT << \Delta$) they are all bound into Cooper pairs. This is why the addition of a new, odd electron requires the energy $E_a + \Delta$, while the addition of the next, even electron, takes $E_a - \Delta$. These "*parity effects*" predicted in 1992 [74] and repeatedly observed experimentally (see, e.g., Refs. 75-77) may substantially affect the dynamics of single-electron devices.

3). If the normal resistance of a tunnel barrier is relatively low, $R \leq (\Delta/E_c)R_Q$, the combination of charging and Josephson coupling makes tunneling of *single Cooper pairs* possible. Since Cooper-pair tunneling is always elastic, its properties differ considerably from that of single electrons. For example, the superconducting versions of single-electron devices may have quantized energy levels [14]; this level structure has been observed in recent experiments [78, 79] with so-called *Bloch transistors*, i.e. Cooper-pair analogs of single-electron transistors, see Fig. 6a.[13] Another important property of the Bloch transistor is that it may exhibit a finite source-drain supercurrent with amplitude being a 2*e*-periodic function of Q_e. This prediction [80, 81] has been confirmed in numerous experiments - see, e.g. Ref. 82. In resistively-coupled superconductor devices (such as that shown in Fig. 9a) the Cooper-pair tunneling may result in the generation of so-called "*Bloch oscillations*" [14] with frequency

$$f_B = I/2e. \qquad (19)$$

either instead of or on top of the SET oscillations. These oscillations (which present a dual quantum-mechanical analog of the usual Bloch oscillations in solids, see, e.g., Ref. 83) have been observed experimentally [63].

IV. ANALOG APPLICATIONS

A. Supersensitive Electrometry

[13] Bloch transistor was first suggested and analyzed in 1986 [80, 81].

If the source-drain voltage V applied to a single-electron transistor is slightly above its Coulomb blockade threshold V_t, source-drain current I of the device is extremely sensitive to the gate voltage U. In fact, Fig. 6b shows that even the changes δU corresponding to sub-single-electron variations δQ_e of the external charge lead to measurable variations of I. This extremely high sensitivity has been suggested [30] as a basis for supersensitive electrometry. Calculations based on the orthodox theory have shown [84] that the sensitivity of such an electrometer is not very impressive if the internal capacitance C_i of the signal source is large on the scale of e^2/k_BT (at sub-1-K temperatures, above ~ 0.1 pF). On the other hand, if the source is so small and so close to the single-electron transistor that C_i of the order of the capacitances of the transistor $C_{1,2}$, white noise limits the charge sensitivity at an extremely low level, $(\delta Q_e)_{min}/\Delta f^{1/2} < 10^{-5}\ e/\sqrt{\text{Hz}}$, for the devices with routinely achieved 100-nm-scale islands (here Δf is the measurement bandwidth).

Since the technology of fabrication of tunnel barriers for single-electron devices is still in its infancy, they apparently contain many electron trapping centers and other two-level systems capable of producing "telegraph noise" - random low-frequency variations of the barrier conductance. This may explain the fact that the excess $1/f$-type noise resulting from these variations exceeds [85] the fundamental white noise up to very high frequencies (apparently at least a few MHz). Only in high-frequency experiments [86] has the white noise been observed (and shown to vary in accordance with the theoretical predictions). This is why the best charge resolution obtained at relatively low frequencies (~10 Hz) was somewhat lower than $10^{-4}\ e/\sqrt{\text{Hz}}$ [87-89]. Nevertheless, even with this "high" noise, these electrometers are some 6 orders of magnitude more sensitive that the best commercially available instruments, and about 100 times more sensitive than specially designed low-temperature semiconductor devices (see, e.g., Ref. 90, 91). In a very recent work [92] in which GHz-range modulation was used to get away from a part of the $1/f$ noise, a charge sensitivity close to $10^{-5}e/\sqrt{\text{Hz}}$ (at ~1 MHz) was demonstrated. This result gives hope that electrometers with the white-noise-limited sensitivity ($\sim 10^{-5}e/\sqrt{\text{Hz}}$ at helium temperatures and $\sim 10^{-4}\ e/\sqrt{\text{Hz}}$ at room temperatures) will be routinely available in the near future[14].

The high sensitivity of single-electron transistors has already enabled several groups to use them as electrometers in unique physical experiments. For example, they have made possible unambiguous observations [75-77] of the parity effects in superconductors, mentioned in Sec. II.G above. Absolute measurements of extremely low dc currents ($\sim 10^{-20}$ A) have been demonstrated [94]. The transistors have also been used in the first measurements of single-electron effects in single-electron boxes [29] and traps [52, 57-60]. A modified version of the transistor has been used for the first proof of the existence of fractional-charge excitations in the fractional quantum Hall effect [95]. Another recent example is the sensitive measurement of local variations in the chemical potential of 2D electron gas in GaAs/AlGaAs heterostructures [96, 97]. Further application of these unique electrometers in scientific experimentation is certainly imminent.

Finally, a new exciting field has been opened by the work of a Lucent Technologies group [98] who have managed to fabricate a single-electron transistor on the tip of a scanning probe and with its help implement a new type of scanning microscopy, combining submicron spatial resolution with sub-single-electron sensitivity. This novel technique has already been used to observe single charged impurities in GaAs/AlGaAs heterostructures.

---

[14] Another important trend is the integration of single-electron transistors with field-effect transistors providing the next amplification stage, and more importantly the matching of the very high output impedance of the SET to that of usual RF transmission lines. This allows the useful bandwidth of the single-electron transistor electrometers to be raised to tens MHz - see, e.g., Refs. 89, 93.

B. Single-electron spectroscopy

Another useful spin-off of single-electron electrometry is the possibility of measuring the electron addition energies (and hence the energy level distribution) in quantum dots and other nanoscale objects, pioneered by M. Kastner's group at MIT [99].

There are two natural ways to carry out such measurements. The first is to use the quantum dot as the island of the single-electron box, capacitively coupled to the single-electron transistor or other sensitive electrometer [90, 100]. The second is to use the quantum dot directly as the island of a weakly biased single-electron transistor ($V \to 0$), and measure the gate voltages U_n providing the sharp increase of the source-drain conductance G - see Eq. (14) and its discussion. The latter method is technically simpler (only one small island is needed) and is preferred by most groups. Moreover, the height of the conduction peak gives additional information on the corresponding electron wavefunction distribution in the dot (see, e.g., Refs. 90, 101).

Single-electron spectroscopy was first applied to laterally-confined "puddles" of 2D electron gas in semiconductor heterostructures with lateral [102] or vertical [103] tunneling to source and drain. Recently, this technique was also used to study electron addition spectra of nanometer metallic particles [42, 104], naturally formed nanocrystals [44, 105], C_{60} buckyballs [46], and carbon nanotubes [106, 107], with good prospects to have it extended to numerous nanoobjects, first of all organic macromolecules and clusters [40, 47, 49]. Presently single-electron spectroscopy is developing virtually independently of other applications of single-electronics. This is why I will make no attempt to review it in any detail; for recent reviews the reader is referred, e.g., to Ref. 12 . I would like, nevertheless, to offer one remark.

Most of the semiconductor quantum dots studied experimentally by single-electron spectroscopy have shown that their energy spectra are irreproducible and only distantly related to those of the idealized simple objects studied in most theoretical works. This is quite understandable taking into account the fact that the dots have numerous electron scattering centers and/or shape irregularities. (These objects are sometimes called "*artificial atoms*", but so far these atoms are certainly not as tidy as the natural ones.) In the presence of uncontrollable inhomogeneities, the only available approach to sort out single-electronics data is statistical. The few past years were marked by rapid experimental and theoretical progress in this direction, especially after it was recognized that in some cases the results may be adequately described by the well-developed random matrix theory - see, e.g., Ref. 108.

This progress should not conceal the fact that there is very little chance of practical application of single-electron devices with random electron addition energies, especially in integrated circuits (see Sec. V below). In this context the only hope is that better nanofabrication techniques will give us more reproducible structures in future. The recent unique experiments by S. Tarucha, L. Kouwenhoven and their collaborators [109] gave the first evidence of a semi-quantitative agreement between the experiment and quantum calculations assuming a simple dot geometry, presumably indicating that reproducible quantum dots may eventually be possible after all. Unfortunately, even that would hardly solve the related problem of random background charges - see Sec. V.C below.

C. DC Current Standards

Another possible application of single-electron tunneling is fundamental standards of dc current. The initial suggestion for such a standard [14, 15] was to phase lock SET oscillations (17)

or Bloch oscillations (19) in a simple oscillator (Fig. 9), with an external rf source of a well characterized frequency *f*. The phase locking would provide the transfer of a certain number *m* of electrons per period of external rf signal and thus generate dc current which is fundamentally related to frequency as $I = mef$. Later it turned out to be more convenient to use such a stable rf source to drive devices such as single-electron turnstiles and pumps (see Sec. III.E above), which do not exhibit coherent oscillations in the autonomous mode.

Already the first experiments [54] with the 2+2-junction turnstile have shown that its relative accuracy $\delta I/I$ can be as good as $\sim 10^{-3}$. The following theoretical work [110-113] has indicated that even better accuracy may be provided by the pumps, since these devices allow a more gentle transfer of the single-electron along its array, and leave less margin for the parasitic processes of thermal activation and cotunneling which may result in error (say, the occasional transfer of an extra electron). An additional advantage of the pump is the possibility of compensating for the random background charge of each island (see below) with a specially tuned dc voltage bias applied to each gate. Theory indicates [113] that the known effects limit the accuracy of a 5-junction turnstile with typical present-day parameters and waveforms at the level of $\sim 10^{-12}$ at $f \sim 10$ MHz, and even down to 10^{-16} if special waveforms are used.

The best experimental effort so far gave an accuracy of 1.5×10^{-8} [114], presumably limited by the photo-excitation of extra electrons by some multi-GHz electromagnetic radiation creeping into the system. Though finding and mending these radiation leaks may present a problem, apparently it can be solved as evidenced by the above-mentioned experiments with single-electron traps [58, 60]. Thus I have no doubt that a dc current standard with relative accuracy better than 10^{-10} (sufficient for all the suggested applications - see, e.g., Ref. 115) can be implemented using pump-type devices.

A greater challenge is a substantial increase in the output current of single-electron standards (presently in the pA range) which would allow much broader application of these devices in metrology. A direct increase of the drive frequency *f* in pump-type devices runs into the problem of rapidly growing dynamic error rate, as soon as it becomes comparable to $1/RC$ [111-113]. One way to avoid this problem is to use a single-Cooper-pair version of the pump; here tunneling is elastic, and the drive frequency may be much higher, eventually limited only by the energy gap of the superconducting materials used at a few tens GHz ($I = ef \sim$ few nA). Unfortunately, these devices are still plagued with the occasional quasiparticle "poisoning", the possible reasons for which are not well understood - see, e.g., Ref. 74.

Another way may be getting rid of the tunneling altogether. In fact, instead of waiting until an electron tunnels through a barrier separating two islands of a pump, it would be much better to carry it over, trapped in a potential well moving along a solid state structure, just as is done with multi-electron bundles in charge-coupled devices [62]. An interesting attempt to implement such a structure using surface-acoustic waves in a GaAs channel is described in Ref. 116. I believe, however, that a more straightforward way would be a direct scaling down of electric-field-controlled silicon-based CCD structures, simultaneously with their cooling to sub-Kelvin temperatures (which may require an increase of electrode doping levels to avoid carrier freeze-out). To my knowledge, this approach has not yet been explored.

D. Temperature Standards

Recently, an unexpected avenue toward a new standard of absolute temperature has been developed by J. Pekola and his collaborators [117-119], on the basis of 1D single-electron arrays.

At low temperatures, arrays with $N>>1$ islands exhibit dc I-V curves generally similar to those of single-electron transistors (see, e.g., Fig. 6b), with a clear Coulomb blockade of tunneling at low voltages ($|V|<V_t$) and approaching the linear asymptote $V = NRI$ + const at $|V|>>V_t$. If the temperature is raised above E_c/k_B, thermal fluctuations smear out the Coulomb blockade, and the I-V curve is almost linear at all voltages: $G \equiv dI/dV \approx G_n \equiv 1/NR$. The only remaining artifact of the Coulomb blockade is a small dip in the differential conductance around V=0, with amplitude $\Delta G/G_n \approx - E_c/6k_BT$ and the FWHM width

$$\Delta V = 5.44\, Nk_BT/e. \qquad (20)$$

Theoretical analysis based on the orthodox theory has shown [118, 119] that equation (20) is surprisingly stable with respect to almost any variations of the array parameters (with the important exception of a substantial spread in the junctions' resistances), providing a remarkable opportunity to use the arrays for absolute thermometry, since the fundamental constants are known with high accuracy. Each particular array may give high (~1%) accuracy of T within less than one decade of temperature variations, but for arrays with different island size (and hence different E_c) these ranges may be shifted and overlap. Thus it is possible to have an absolute standard of temperature with a very broad (say, two-decade) total range from several circuits fabricated on a single chip.

This development is very encouraging, but since all this work is recent, some time is needed to see whether these new devices will be able to compete with (or even replace) the established temperature standards.

E. Resistance Standards

According to a theoretical prediction [80, 81], in the resistively-biased Bloch transistor, Bloch oscillations (19) may coexist with the usual Josephson oscillations with frequency

$$f_J = 2eV/h. \qquad (21)$$

Moreover, these two oscillations may phase lock, resulting in the fundamental quantization of the off-diagonal component of the conductance matrix of this three-terminal device:

$$R_\perp = V/I = (m/n)(h/e^2), \qquad (22)$$

where m and n are small integers. A more practical way to the same relation may be the simultaneous phase locking of both the Bloch and Josephson oscillations with the same external microwave source.

Relation (21) is similar to that taking place at the quantum Hall effect and promises even higher fundamental accuracy. This phenomenon has not yet been explored experimentally, because the implementation of narrow-band Bloch oscillations requires micron-scale resistors with $R_s \sim 1$ MΩ, which are still at the developmental stage. However, very recent results in this direction [69] are encouraging.

F. Detection of Infrared Radiation

The first calculations [120] of the videoresponse ("photoresponse") of single-electron systems to electromagnetic radiation with frequency $f \sim E_C/h$ have shown that generally the response differs from that following from the well-known Tien-Gordon theory [121] of photon-assisted

tunneling. In fact, this famous result is based on the assumption of independent (uncorrelated) tunneling events, while in single-electron systems the electron transfer is typically correlated. Nevertheless, further work [122] has shown that the Tien-Gordon formula *is* applicable to the individual tunneling *rates*:

$$\Gamma(\Delta W, A) = \sum_{k=-\infty}^{\infty} J_k^2(eA/hf) \times \Gamma(\Delta W + khf, 0). \qquad (23)$$

where A is the amplitude of the microwave voltage across the junction, f is the radiation frequency, while $J_k(x)$ are the first-order Bessel functions of argument x. This formula is believed to be valid for any system which may be described with master equations similar to Eq. (7), regardless of the exact formula for the background tunneling rate $\Gamma(\Delta W, 0) \equiv \Gamma(\Delta W)$. Moreover, for most important interesting cases, e.g. near the Coulomb blockade threshold, Eq. (23) is also valid for the dc current as a whole. These predictions have been confirmed experimentally - see, e.g., Refs. 122-124.

This fact implies that single-electron devices, especially 1D multi-junction arrays with their low cotunneling rate, may be used for ultrasensitive video- and heterodyne detection of high-frequency electromagnetic radiation, similar to the superconductor-insulator-superconductor (SIS) junctions and arrays (see, e.g., Refs. 125, 126). The single-electron arrays may have two advantages over their SIS counterparts: lower shot noise (because the Coulomb blockade in systems with $N>>1$ islands in series may provide lower leakage currents than the superconducting energy gap), and convenient adjustment of the threshold voltage (by changing the junction size and hence E_C). This opportunity is especially promising for detection in the few-terahertz frequency region, where no background-radiation-limited detectors are yet available.

A major obstacle on the path toward the extension of this approach to imaging may be the randomness of the background charge (see Sec. V.C below) which may make capacitive gating of each island necessary. This may be acceptable for single detectors, but not for multiple-pixel focal-plane arrays.

Another interesting opportunity is the use of single-electron transistors as pre-amplifiers and/or single-electron counters for semiconductor infrared detectors - see experiments [94].

V. PROSPECTS FOR DIGITAL APPLICATIONS

Most of the opportunities described in the previous section are very promising, but in terms of contemporary electronics as a whole they still look like niche applications. From the very formulation of single-electronics as an applied discipline [6, 30, 127], the most intriguing question was whether single-electron devices will be able to compete with semiconductor transistor circuits in mainstream, digital electronics. Several paths toward this goal have been explored.

A. Voltage State Logics

The first opportunity [30] is to use single-electron transistors (Fig. 6a) in the *"voltage state"* mode. In this mode, the input gate voltage U controls the source-drain current of the transistor which is used in digital logic circuits, similarly to the usual field-effect transistors (FETs). This means that the single-electron charging effects are confined to the interior of the transistor, while externally it looks like the usual electronic device switching multi-electron currents, with binary unity/zero presented with high/low dc voltage levels (physically not quantized). This concept

simplifies the circuit design which may ignore all the single-electron physics particulars, except the specific dependence of the source-drain current I on voltages V and U - see Fig. 6b,c.

For a digital circuit designer, there is both good and bad news in this dependence. On the one hand, the alternating transconductance of the single-electron transistor (Fig. 6c) makes possible a very simple design of complementary circuits using transistors of just one type [30, 128][15]. On the other hand, it makes the exact copying of CMOS circuits impossible, and in order to get substantial parameter margins, even the simplest logic gates have to be re-designed. The re-designed and optimized circuits (Fig. 10) may operate well within a relatively wide parameter window [130]. However, their operation range starts shrinking under the effect of thermal fluctuations as soon as their scale $k_B T$ reaches approximately $0.01E_a$ [130]. (For other suggested versions of the voltage state logic [128, 131], the temperature range apparently is even narrower). The maximum temperature may be increased by replacing the usual (single-island, double-junction) single-electron transistors for short 1D arrays with distributed gate capacitances [132]. For example, 5-junction transistors allow a 3-fold increase of T_{max}, for the price of bulkier circuits. However, according to Fig. 2, in order to operate at room temperature even with this increase the transistor island size has to be extremely small (<1 nm).

One more substantial disadvantage of voltage state circuits is that neither of the transistors in each complementary pair is closed too well, so that the static leakage current in these circuits is fairly substantial, of the order of 10^{-4} e/RC. The corresponding static power consumption is negligible for relatively large devices operating at helium temperatures. However, at the prospective room-temperature operation this power becomes on the order of 10^{-7} Watt per transistor. Though apparently low, this number gives an unacceptable static power dissipation density (>10 kW/cm^2) for the hypothetical circuits which would be dense enough (>10^{11} transistors per cm^2) to present a real challenge for the prospective CMOS technology.

B. Charge State Logics

The latter problem may be avoided by using another type of logic device in which single bits of information are presented by the presence/absence of single electrons at certain conducting islands *throughout the whole circuit*. In these circuits the static currents and power vanish, since there is no dc current in any static state.

This approach was first explored theoretically in 1987 [133]. In the suggested circuits an extra electron could be propagated along considerable externally-timed shift-register-type segments of the circuit, while resistively-coupled transistors provided splitting of the signal and binary logic operations. Unfortunately the suggested circuits required resistors and also had very narrow parameter margins. Since then, several families of charge state logics have been suggested - see, e.g., Refs. 134-150. Some of them [138, 141, 147] have developed further the initial concept of electron propagation [133], but using more practical, capacitively-coupled circuits. In most suggestions, however, the electron is confined in a cell consisting of one or a few islands, while the logic switching is achieved via electrostatic [134-137, 140, 142, 144-148, 150] or spin [139, 143,149] coupling of the cells.

A deeper classification of single electron logics may be based on where they take the energy necessary for logic operations: from dc power supply [133, 134, 141, 147], ac power supply

[15] This is true for both resistively-coupled [30] and capacitively-coupled [128] transistors. Unfortunately, the resistively-coupled devices are more sensitive to thermal fluctuations [129] (on top of the difficulties with implementation of small resistors - see below).

(also playing the role of global clock) [134, 140, 142, 145], or just from the energy of an external signal [135-139, 143-146, 149, 150]. The latter category of devices implies the use some (typically unspecified) inter-stage amplifiers in order to compensate for the energy lost inside the logic stages.[16]

Only a few of these concepts have been analyzed in detail, especially at finite temperatures. To my knowledge, the most robust single-electron logic circuits suggested till now are those based on the so-called "*SET Parametron*" [142]. The simplest version of the device uses three small islands separated by two tunnel barriers (Fig. 11a). The central island is slightly shifted out of the center line. A periodic "clock" electric field $\boldsymbol{E}_c$ keeps an extra electron in the central island during a part of the clock period. At some instant, the electron transfer to one of the edge islands becomes energy advantageous (the sign of ΔW changes from negative to positive). If the system were completely symmetric, the choice between the two edge islands would be random, i.e. the system would undergo what is called spontaneous symmetry breaking. However, even a small additional field $\boldsymbol{E}_s$ applied by a similar neighboring device(s) may determine the direction of electron tunneling at the decision-making moment. Once the barrier ΔW created by the further change of the clock field has become large enough, the electron is essentially trapped in one of the edge islands, and the field $\boldsymbol{E}_s$ may be turned off. Now the device itself may serve as a source of the signal field $\boldsymbol{E}_s$ for the neighboring cells. The sign of this field (i.e. of the electric dipole moment of the device) presents one bit of information.

Figure 11c shows a shift register based on SET Parametrons. The direction of the shift of the central island of each next device is shifted by $\pi/3$ within the *yz* plane. The circuit is driven by electric field $\boldsymbol{E}_c(t)$ rotating in the same plane and providing the periodic switching on the SET parametrons, with an appropriate phase shift. As a result, each digital bit (one per three cells) is being shifted by 3 cells along the structure each clock period. Logic gates may be implemented in the same way [142]. Geometric modeling and numerical simulation of these circuits within the framework of the orthodox theory have shown that they may operate correctly within approximately ±20% intervals of clock amplitude. Estimates show that the maximum operation temperature of these logic circuits is of the order of that of voltage mode circuits, i.e. of the order of $0.01E_c/k_B$, if the bit error rate is in the practically acceptable range (below $\sim 10^{-20}$).

A new, potentially useful feature of the charge state logics is the natural internal memory of their "logic gates" (more proper terms are "finite-state cells" or "timed gates"), thus combining the functions of combinational logic and latches. This feature (very similar to that of the ultrafast RSFQ logic [151]) makes natural the implementation of deeply pipelined and cellular automata architectures. The main disadvantage of these circuits in comparison with voltage state logic is the lack of an effective means of transferring a signal over large distances: crudely speaking, this technology does not allow simple wires, just shift registers.

I should also mention in passing the recent proposals [152-155] to use single-electron or single-Cooper-pair structures for quantum computing. These proposals are so new that they should be analyzed in much more detail before any judgement is rendered. The only comment I can offer at this stage is that the practical implementation of these devices would be even harder than the "classical" charge state logics, since quantum computing also requires a high degree of coherence of the charge (or spin) states to be maintained.

C. Problems, Problems…

[16] Some of these proposals are highly controversial - see, e.g., the discussion in Refs. 140, 148-150.

The first big problem with all the known types of single-electron logic devices is the requirement $E_c \sim 100\ k_B T$, which in practice means sub-nanometer island size for room temperature operation (Fig. 2).[17] If we are not just talking about single-device demos but VLSI circuits, this fabrication technology level is still nowhere in sight. Moreover, even if these islands are fabricated by any sort of nanolithography, their shape will hardly be absolutely regular. Since in such small conductors the quantum kinetic energy gives a dominant contribution to the electron addition energy ($E_k >> E_c$, see Fig. 2), even small variations in island shape will lead to unpredictable and rather substantial variations in the spectrum of energy levels and hence in the device switching thresholds.

We may dream, of course, about using some naturally made, reproducible objects such as Au_{55} clusters, or C_{60} buckyballs, or some other macromolecules. (Fortunately, single-electronics imposes no fundamental restrictions on the island material, besides being "conductive", i.e. having no excessive energy gaps around the Fermi level). It must not be forgotten, however, that these objects have to be aligned with other islands and possibly conducting nanowires, and separated from them by tunnel barriers with well-reproducible capacitances and tunnel resistances. The much-advertised "self-assembly" (which nowadays means mostly the formation of uniformly packed 2D arrays of clusters or macromolecules) is not enough! The research in this area should eventually address the issue of island placement on the preliminarily defined points with nanometer precision, and I have not heard about any simple solution to this problem.[18]

The second major problem with single-electron logic circuits is the infamous *randomness of the background charge*. Figure 12 illustrates this problem with the example of the single-electron transistor. Let a single charged impurity be trapped in the insulating environment, say on the substrate surface, at a distance a from the island, comparable to its size. The impurity will polarize the island, creating on its surface an image charge Q_0 of the order of e. This charge is effectively subtracted from the external charge Q_e (see Eq. (11)) which determines the Coulomb blockade thresholds V_t. As is evident from Fig. 6b,c, this shift may be large, of the order of $(V_t)_{max}$, even from a simple impurity. Using a very optimistic estimate of 10^{10} cm^{-2} for the minimum possible concentration surface/interface charge trap concentration (see, e.g. Ref. 156), and assuming that the minimum device density of practical interest is 10^{10} cm^{-2}, we get that about one of 1,000 devices with 1-nm islands will have a considerable background charge fluctuation ($|Q_0| > 0.1\ e$).[19] Presumably, this is unacceptable for any VLSI application.

There is a slight chance that this problem (which is dominant in present-day experiments with relatively large devices) will just go away when the islands are scaled down to sub-nanometer size. In fact, the same image charge Q_0 which causes all the trouble always attracts the initial impurity with the Coulomb force scaling as a^{-2}. If this force exceeds the impurity pinning force, it will diffuse toward the particle and finally fall out on its surface where it is no longer dangerous (at this point, Q becomes equal to e and is immediately compensated by one of the tunneling

[17] I do not believe that any practical advantage these circuits may offer would ever justify their cooling to helium (or lower) temperatures.

[18] The electrostatic trapping technique described in Ref. 49 is certainly interesting, but it is not clear how it could be extended to integrated circuits.

[19] Devices with vertical transport are less sensitive to charge impurities located at relatively large distances, because of electrostatic screening by external electrodes [157]. For room temperature operation, however, the cross-section area of these structures should be so small (comparable to the square of the tunnel barrier thickness), that the screening would not be substantial.

electrons). Since some evidence of such "self-cleaning" has been noticed even for particles with a~100 nm [4, 158], this process may become quite effective at $a \sim 1$ nm. Unfortunately, I am not aware of any detailed experimental study of this problem, despite the fact that its crucial importance for applications has been discussed in the literature at least since 1992 [53].

Another possibility is to look for single-electron logic devices which would be insensitive to the background charge. I know of two such proposals: the voltage stage logic based on resistively-biased single-electron transistors [30] and an rf-parametron-type logic based on mutual phase locking of SET oscillators [159]. Both these suggestions rely on Ohmic resistors with continuous (or at least quasi-continuous) transfer of charge which would provide the compensation for the fractional part of the random background charge. The implementation of these resistors for room temperature operation would, however, be very difficult. In fact, theoretical analyses [160, 161] show that in order to provide the continuous transfer of charge a diffusive conductor has to be much longer than the electron-phonon interaction length. For silicon, which is a primary candidate material for these resistors, this length is of the order of 30 nm (see, e.g., Ref. 162), i.e. much larger than the desirable size of the whole device. Moreover, the stray capacitance of such a resistor would be much larger than that of the island itself, dramatically reducing its charging energy and hence the maximum operation temperature.

All these problems put the very idea of using single-electron devices for logic functions very much in doubt. In addition, even if this logic is implemented, it will hardly be extremely fast, because of the high output impedance of single-electron devices ($Z \sim R >> R_Q \sim 10$ kΩ). For example, the charging time of an interconnect as short as 100 μm through a 100 kΩ impedance is of the order of 1 ns, which is hardly an exciting speed. Finally, the fields in which the greatest asset of single-electron devices, their potentially enormous density, are most needed, are not logic but rather random access memories and long-term data storage systems. Fortunately, these are precisely the fields in which encouraging ideas have emerged during the past few years.

D. Background-Charge-Insensitive Memory

Generally speaking, the single-electron trap (Fig. 7a) complemented by an electrometer for sensing its charge state, may already be considered a memory cell with non-destructive readout (NDRO). However, due to the background charge randomness, the 1D array of small islands used in the trap is not a perfect circuit component for the transfer of single electrons. Figure 13 shows the statistical distribution of the Coulomb blockade threshold and the energy barrier height of such arrays, calculated with the assumption of the random background charge of each island. It is evident that these statistics are not good enough for VLSI circuits: even if the junctions are exactly similar there is a considerable chance that the Coulomb blockade will be almost completely suppressed, and hence the memory cell incapable of keeping an electron inside. (The situation with randomly shaped arrays is even worse: the two tunnel junctions with highest resistances typically define the electron transport, effectively turning the array into a single-electron transistor with its relatively high cotunneling rate - see, e.g., the experimental results in Ref. 163). The background charge also makes the single-electron transistor readout unreliable: a random charged impurity may easily imitate the electron trapped in the memory cell.

The memory concept suggested in Ref. 164 (Fig. 14) allows both these problems to be circumvented. A digital bit is stored in a relatively large conducting island (floating gate) in the form of 10 to 20 extra electrons which may be injected through a tunnel barrier using the Fowler-Nordheim process. During this WRITE process the injected electrons ramp up the electric potential U of the floating gate, so that the external charge Q_e of the single-electron transistor is ramped up

by $n'e$, with $n'<n$ ($n'\sim3$). This ramp up causes n' oscillations of the transistor current (Fig. 6c). These oscillations are picked up, amplified, and rectified by a sense amplifier (one MOSFET seems sufficient for this purpose), the resulting signal V_{out} serves as the output. The main idea of this proposal is that the random background charge will cause only an unpredictable shift of the initial phase of the current oscillations, which does not affect the rectified signal. This concept has been verified in recent experiments [165] with a low-temperature prototype of the memory cell.

Notice that the readout in this memory is destructive: READ 0 is combined with WRITE 1 (the absence of output signal during WRITE 0 is achieved by turning off the source-drain voltage V), and requires the subsequent restoration of the initial contents of the cell. This operation, however, is not much more complex than refresh in an ordinary DRAM. The second relatively minor drawback is the need for a sense amplifier/rectifier. Estimates show that since the signals are pre-amplified with the single-electron transistor with its very low noise, one FET amplifier may serve up to 100 memory cells and hence the associated chip real estate per bit is minor. Figure 14b shows a possible layout of the memory cell for room temperature operation; even with due account of the sense amplifiers and drivers it is consistent with the very impressive 10^{11} bit/cm^2 density. The estimated power density (~3 W/cm^2, mostly in the sense amplifiers) also seems quite acceptable.

A very attractive feature of this "*SET/FET hybrid*" design is the relatively mild fabrication requirements: room temperature operation is possible with an electron addition energy of about 250 meV. Figure 2 shows that this level requires a minimum feature (transistor island) size of about 3 nm, i.e. much larger than that required for purely single-electron digital circuits. The reason for this considerable relief is that in this hybrid memory the single-electron transistor is used in essentially analog mode, as a sense preamplifier/modulator, and can tolerate a substantial rate of thermally activated tunneling events. Another big advantage of this memory is the absence of storage capacitors which are so typical for present-day DRAM and make a further increase in their density so difficult (and apparently impossible beyond ~3×10^9 bits/cm^2).

E. Crested Tunnel Barriers

The largest apparent drawback of the hybrid SET/FET memory proposal is the slowness of the WRITE process. In fact, it relies on the process of Fowler-Nordheim tunneling, similar to that used in the ordinary non-volatile, field-alterable memories (EEPROM, etc. - see, e.g., Ref. 166). This process is known to be rather insensitive to the applied voltage. For example, open-point lines in Figure 16 show the tunnel current through, and the time scale of the floating gate recharging time via a typical uniform silicon dioxide tunnel barrier (Fig. 15a,b), for two values of its thickness d. In order to deserve the name "non-volatile", the charge storage ("retention") time has to be at least 10 years (~3×10^8 s), so that, for example, for d = 12 nm the voltage V applied during the charge storage has to be below ~5 V. A simple analysis of the hybrid memory cell operation shows that the maximum voltage applied during WRITE cannot be larger than twice that value in this particular case ~10 V. Figure 16 shows that even at this maximum voltage, the floating gate recharging would take a few milliseconds, possibly tolerable for some flash memories [166], but unacceptably long for bit-addressable applications. A change in either the barrier thickness (see, e.g., the line for d = 8 nm in Fig. 16) or height does not help.

This problem stems from the uniformity of the ordinary tunnel barriers, and can be readily solved using specially shaped "*crested*" barriers [167].[20] In fact, according to the standard

[20] A positive effect of "graded" tunnel barriers on the speed of field-induced electron injection (in that case, thermoionic) was noticed long ago [168]. However, triangulary-shaped barriers studied in that work could not provide short erase time and hence the bit-addressable memory operation as a whole.

quasiclassical theory of tunneling, the barrier transparency is affected mostly by its highest part. In ordinary barriers the highest point is close to the electron source, and is virtually unaffected by the applied voltage (besides small charge image effects which are not shown in Fig. 15, but have been taken into account in the calculation of plots in Fig. 16).

Now let us consider a "crested" barrier shown in Fig. 15c, with the highest point U in the middle. This height U_m is now very sensitive to the external voltage V, decreasing at least as fast as $U_m = U - eV/2$ due to the "field leverage" effect (Fig. 15d). Because of this barrier suppression, the current changes much faster - see the solid-point lines in Fig. 16. For the particular case shown in that figure, $V = 4.5$ V can be selected as a point which allows a good retention time of ~ 10 years, while the recharging time at 9 V is faster than 10 ns.

Of course, a barrier of parabolic shape is much harder to fabricate.[21] Calculations show, however, that trilayer barriers (Fig. 15e,f) may have quite comparable tunneling characteristics. For example, a crested trilayer barrier with $U = 3.6$ V, $d = 5$ nm, $m = 0.48\ m_0$, $\varepsilon = 8.5$; $U' = 2.0$ V, $d' = 2$ nm, $m' = 0.2m_0$, $\varepsilon' = 7.5$ (the parameters correspond to the Si_3N_4/AlN/ Si_3N_4 system) may also provide a sub-10-ns WRITE time at a ~10-year retention. Notice that these calculations have been carried out for well-known materials; it is quite probable that further research will lead to other materials which will allow the barrier performance to be improved even further.

F. NOVORAM

The similarity between the SET/FET hybrids (Fig. 14) and the usual non-volatile memory cells forces us to consider whether the only remaining single-electron component of the cell, the single-electron transistor, may be replaced with a more ordinary device, say a MOSFET scaled down to sub-10-nm dimensions (so that the memory density would not be sacrificed). Until very recently, it was believed that silicon MOSFETs can retain useful performance only if their channel is longer than ~30 nm (see, e.g., Ref. 169). A very recent analysis [170] has shown, however, that silicon *n*-MOSFETs with an undoped (intrinsic) channel and appropriate (dual-gate) geometry (Fig. 17a) may retain a high degree of control by gate voltage even when their gate length is below 10 nm. The reason is that electrons from doped source and drain may penetrate the undoped channel by a distance of a new nm from each side, comparable with the device length (Fig. 17b).[22] When in channel, these electrons move ballistically, without any noticeable scattering. As a result, the effective carrier mobility and hence transconductance is rather high. Figure 17c shows that only when scaled down below ~8 nm the transistors lose the voltage gain necessary for logic applications, but they retain a steep subthreshold curve with high open/closed current ratio (~10^8) even at a channel length ~6 nm.

This remarkable scalability (if confirmed experimentally) will hardly be useful for the usual DRAMs with their storage capacitor problems. However, a 6-nm-gate MOSFET would fit perfectly into the 10-nm space shown in Fig. 14b,c, replacing the single-electron transistor. Moreover, such a memory cell would allow the nondestructive readout with simpler peripheral circuitry. The only additional requirement is that of low noise: the current of the full-selected

[21] This would be relatively easy to do with silicon (using the ionization of shallow donors) or with A_3B_5 compounds allowing epitxial growth (using the gradual change of the composition - see, e.g., Re. 168). However, the resulting energy barriers are not high enough to provide sufficiently long retention time at room temperature.

[22] High contact doping (e.g., 3×10^{20} cm^{-3}) ensures that the number of dopants within the relevant regions of source and drain is high enough, so that device-to-device statistical fluctuations of parameters are relatively small.

transistor (if open by the floating gate charge corresponding to binary 1) has to be well above the aggregate noise of all semi-selected transistors in the same bit line sector. A quantitative analysis of the noise performance of the nanoscale ballistic MOSFETs is still due, but preliminary estimates by our Stony Brook group show that the noise may be sufficiently low. Hence, the combination of crested barriers and nanoscale ballistic transistors may transform the usual floating-gate devices into unique non-volatile random-access memories (NOVORAM [167]) scalable all the way down to ~ 6-nm minimum feature size.

F. Other Single-Electron and Few-Electron Memories

The theoretical developments described above were preceded (and stimulated) by several important experimental works. In particular, K. Yano and his Hitachi co-workers have demonstrated [171] that MOSFETs with a granular silicon channel may show memory effects, apparently related to the capture of single electrons in certain stand-alone grains of the channel (Fig. 18). After capture, the electron changes the conductivity of the more conductive parts of this channel. The disadvantage of this geometry is that the grain geometry, and hence the memory cell switching thresholds are inherently irreproducible. This drawback could not be eliminated even when the Hitachi group started to use *several* electrons for coding each bit (for some reason still using the term "single-electron memory") [172]. I believe that this problem does not leave any hope for the implementation of practical memories based on this principle. (This opinion is apparently not shared by K. Yano and his colleagues - see their paper in this issue. [23])

A step in the right direction was made in experiments by the team of S. Tiwari at IBM [174], in which the electron-capturing islands and a MOSFET channel are physically separated; now the channel does not have to be granular and its parameters may be quite reproducible. As in the hybrid SET/FET memory discussed above, and the recent work of the Hitachi group, the data bits were stored as *few-electron* charges, thus avoiding the detrimental effects of the random background charge on the WRITE process. [24]

Similar experiments, but with a smaller structure (~7-nm floating gate, ~10-nm MOSFET, Fig. 19) were carried out by S. Chou and his colleagues at the University of Minnesota [129]. In these experiments the floating gate was so small that the addition of a single electron changed the transistor current considerably. The prospects for the use of this charge quantization effect are, however, questionable in view of the background charge randomness: even a single charged impurity will shift the electron injection threshold considerably, making the operation irreproducible from cell to cell. I believe that a more important result of this remarkable work is the first experimental proof that the current in a MOSFET with a ~10-nm-long channel may be gate-modulated by more than two orders of magnitude, despite using a "wrapped-around" gate instead of more optimal dual-gate geometry. (Similar experiments, but with somewhat larger devices, are described in Ref. 176.) The only major step which separates this work from NOVORAM is the replacement of the uniform SiO_2 tunnel barrier with the crested barrier (Fig. 15).

Figure 20 presents a summary of my current vision of the prospects of the development of semiconductor bit-addressable memories. The DRAM development predictions have been borrowed from the recent industrial forecast [177]. I believe that it will be very difficult to push

[23] Recently the Hitachi group presented [173] an "early prototype" of a 128 Mb memory chip using these cells, but the fraction of correctly operating bits has not been announced.

[24] An almost similar device was explored earlier by another group [163], but with the charge injection carried out through a random junction array. As was discussed above, this circuit component is inherently irreproducible.

these memories beyond 64 Gbit integration (density ~6 Gb/cm^2), mostly due to problems with the storage capacitor scaling. This would leave us with ~70-nm fabrication technologies. Since room-temperature SET/FET hybrids are only feasible starting from ~3-nm minimum feature size, this enormous technological gap would be virtually impossible to cross. Fortunately, it seems that NOVORAM may provide a reliable bridge over this gap.

Moreover, I expect that NOVORAM may present a serious challenge for DRAMs even at the present technological level, since the non-volatility it offers is very important for low-power electronics applications. If this transition from DRAM to NOVORAM really happens (see the dashed arrow in Fig. 20), the gradual technology improvement from one memory generation to the next which has characterized the last three decades of semiconductor electronics, may continue and eventually bring us terabit-scale integrated circuits.

G. Electrostatic Data Storage

Crested barriers may make possible not only terabit-scale memories, but also revive the long-cherished idea of ultradense electrostatic data storage. For example, Figure 21 shows a possible design [178] of a storage system using a SET/FET hybrid. This hybrid (a single-electron transistor loaded on a MOSFET amplifier at a distance of a few microns) would be fabricated on a tip-shaped chip playing the role of a READ/WRITE head. The data bits are stored as multi-electron charge bundles trapped in nanoscale conducting grains deposited on top of a crested tunnel barrier. It is important that since each charge bundle is stored in a few (~10) grains, their exact shape and location are not important, so the storage medium production does not require any nanofabrication.

WRITE is performed by the application of the same voltage V_W to both input terminals, relative to the conducting ground layer of the moving substrate. The resulting electric field of the tip induces rapid tunneling of electrons from the ground through the crested barrier into a ~50-nm-wide group of grains. For READ, the single-electron transistor is activated by source-drain voltage $2V_R \geq V_t$. In this state it is very sensitive to the electric field created by the group of charged grains it is being flown above.

Simple estimates show that with a 50-nm tip-to-substrate distance (only a few time less than in the best present-day magnetic storage systems), the electrostatic system is capable of a density ~10 Terabits per square inch, i.e. about two orders of magnitude higher than the best prospects for the magnetic competition of which I am aware. In sharp contrast with previous ideas for the implementation of electrostatic data storage (see, e.g., Ref. 179) the use of crested barriers may provide a very broad bandwidth of both WRITE and READ operations, up to 1 Gbps per channel, possibly quite adequate even for this enormous bit density. The recent experiments at Lucent Technologies [98] (which were already mentioned in Sec. IV.A above) may be considered as the first step toward the implementation of this idea.

VI. CONCLUSION

Single-electronic devices have already proved their value as tools in scientific research. Several applications of these devices in metrology, including the fundamental standards of current, resistance, and temperature also seem quite promising. Another prospective application field is terahertz radiation detection and (possibly) imaging.

The situation with digital single-electronics is much more complex. The concepts of single-electron logic circuits suggested so far face tough challenges: either that of removing the random background charge or alternatively that of providing continuous charge transfer in nanoscale resistors. I am not familiar with any realistic suggestion how to *solve* either of these problems. Fortunately, there is at least one suggestion (the SET/FET hybrids) how to *circumvent* these problems in memory, i.e. exactly where the ultrahigh device density is most needed.

This still leaves us with the most important problem, the fabrication. Despite recent progress in the fabrication of *single* devices with a-few-nm minimum features, prospects for the fabrication of VLSI *circuits* with the same resolution are still very distant. Indeed, the methods used in this research field (mostly direct electron-beam writing and scanning probe manipulation) are hardly scalable to whole-wafer or even whole-chip level, because of their very low speed. The development of VLSI nanofabrication methods (e.g., multiple-electron-beam writing) will certainly require many years and many billions of dollars. Moreover, it is possible that because of technological and/or economic limitations these remarkable opportunities will never be realized.

However, the recent ideas may have indicated how to make this technological development gradual, almost evolutionary - see Fig. 20 and its discussion. Simultaneously, the development of room-temperature single-electron devices may provide some important spin-offs for the digital world even at the low-integration-scale stage - see, for example, the discussion of electrostatic data storage in Sec. V.G above. This is why I continue to be optimistic about the future prospects for this interesting field of applied physics.

ACKNOWLEDGMENTS

The author is grateful to Dr. T. Ishii for the permission to use Fig. 18, and to Dr. A. Korotkov for the permission to use Fig. 13 (both prior to publication), to Dr. C. Wasshuber for providing his unpublished data on the comparison of performance of single-electron Monte-Carlo simulators, and to Prof. D. Averin, Dr. D. Dixon, and anonymous referees for critical reading of the manuscript and valuable remarks. It is my pleasure to acknowledge also the wonderful hospitality of Prof. Hans Mooij and his associates in TU Delft, The Netherlands, where the final editing of the manuscript has been carried out. The research in various fields of fundamental and applied single-electronics at Stony Brook is supported in parts by the AFOSR, OER, and ONR/DARPA.

References

[1] C.J. Gorter, "A possible explanation of the increase of the electric resistance of thin metal films at low temperatures and small field strength", *Physica*, vol. 15, pp. 777-780, August 1951.

[2] C.A. Neugebauer and M.B. Webb, "Electrical conduction mechanism in ultrathin, evaporated metal films", *J. Appl. Phys*., vol. 33, pp. 74-82, January 1962.

[3] H.R. Zeller and I. Giaever, "Tunneling, zero-bias anomalies, and small superconductors", *Phys. Rev*., vol. 181, pp. 789-799, May 1969.

[4] J. Lambe and R.C. Jaklevic, "Charge-quantization studies using tunnel capacitor", *Phys. Rev. Lett*., vol. 22, pp. 1371-1375, June 1969.

[5] I.O. Kulik and R.I. Shekhter, "Kinetic phenomena and charge discreteness effects in granular media", Zh. Eksp. Teor. Fiz. vol. 62, pp. 623-640 [*Sov. Phys. - JETP*, vol. 41, pp. 308-316], February 1975.

[6] K.K. Likharev, "Correlated discrete transfer of single electrons in ultrasmall tunnel junctions", *IBM J. Res. Devel*., vol. 32, pp. 144-158, January 1988.

[7] D.V. Averin and K.K. Likharev, "Single-electronics: Correlated transfer of single electrons and Cooper pairs in small tunnel junctions", in *Mesoscopic Phenomena in Solids*, ed. by B. Altshuler, P. Lee and R. Webb. Amsterdam: Elsevier, 1991, p. 173-271.

[8] *Single Charge Tunneling*, ed. by H. Grabert and M.H. Devoret. New York: Plenum, 1992.

[9] H. van Houten, C.W.J. Beenakker, and A.A.A. Staring, "Coulomb blockade oscillations in semiconductor nanostructures", in: *Single Charge Tunneling*, ed. by H. Grabert and M.H. Devoret. New York: Plenum, 1992, pp. 167-216.

[10] M.A. Kastner, "Artificial Atoms", *Physics Today*, vol. 46, pp. 24-31, January 1993.

[11] U. Meirav and E.B. Foxman, "Single-electron phenomena in semiconductors", *Semicond. Sci. Technol*. vol. 10, pp. 255-284, October 1995.

[12] L.P. Kouwenhoven, C.M. Markus, P.L. McEuen, S. Tarucha, R.M. Westervelt, and N.S. Wingreen, "Electron transport in quantum dots", in *Mesoscopic Electron Transfer*, ed. by L. Sohn *et al*. Dordrecht: Kluwer, Dordrecht, 1997, pp. 105-215.

[13] G.-L. Ingold and Yu.V. Nazarov, "Charge tunneling rates in ultrasmall junctions", in *Single Charge Tunneling*, ed. by H. Grabert and M.H. Devoret. New York: Plenum, 1992, pp. 21-108.

[14] K.K. Likharev and A.B. Zorin, "Theory of the Bloch-wave oscillations in small Josephson junctions", *J. Low Temp. Phys*., vol. 59, pp. 347-382, February 1985.

[15] D.V. Averin and K.K. Likharev, "Coulomb blockade of tunneling, and coherent oscillations in small tunnel junctions", *J. Low Temp. Phys*., vol. 62, pp. 345-372, February 1986.

[16] K.K. Likharev, N.S. Bakhvalov, G.S. Kazacha, and S.I. Serdyukova, "Single-Electron Tunnel Junction Array: An Electrostatic Analog of the Josephson Transmission Line", *IEEE Trans. Magn*., vol. 25, pp. 1436-1439, March 1989.

[17] C. Wasshuber and H. Kosina, *Superlattices and Microstructures*, "A single-electron device and circuit simulator", *Superlattices and Microstructures*, vol. 21, pp. 37-42, January 1997; C. Wasshuber, H. Kosina, and S. Selberherr, "SIMON - A simulator for single-electron tunnel devices and circuits", *IEEE Trans. on Computer Aided Design*, vol. 16, pp. 937-944, September 1997.

[18] C. Wasshuber, private communication, February 1998.

[19] S. Amakawa, H. Majima, H. Fukui, M. Fujishima, and K. Hoh, "Single-electron circuit simulation", *IEICE Trans. on Electronics*, vol. E81-C, pp. 21-29, January 1998.

[20] D.V. Averin and A.A. Odintsov, "Macroscopic quantum tunneling of the electric charge in small tunnel junctions", *Phys. Lett. A*, vol. 140, pp. 251-257, September 1989.

[21] L. J. Geerligs, D.V. Averin, and J.E. Mooij, "Observation of macroscopic quantum tunneling through the Coulomb energy barrier", *Phys. Rev. Lett*., vol. 65, pp. 3037-3040, December 1990.

[22] D.V. Averin and Yu.V. Nazarov, "Macroscopic quantum tunneling of charge and co-tunneling", in *Single Charge Tunneling*, ed. by H. Grabert and M.H. Devoret. New York: Plenum, 1992, pp. 217-248.

[23] D.V. Averin and A.N. Korotkov, "Correlated single-electron tunneling via mesoscopic metal particles: effects of energy quantization", *J. Low Temp. Phys*. vol. 80, pp. 173-185, August 1990.

[24] F.R. Waugh, M.J. Berry, D.J. Mar, R.M. Westervelt, K.L. Campan, and A.C. Gossard, "Single electron charging in double and triple quantum dots", *Phys. Rev. Lett*., vol. 75, pp. 705-708, July 1995; F.R. Waugh, M.J. Berry, C.H. Crouch, C. Livermore, D.J. Mar, R.M. Westervelt, K.L. Campan, and A.C. Gossard, "Measuring interactions between tunnel-coupled quantum dots", *Phys. Rev. B*, vol. 53, pp. 1413-1420, January 1996.

[25] N.C. van den Vaart, S.F. Godijn, Yu.V. Nazarov, C.J.P.M. Harmans, J.E. Mooij, L.W. Mollenkamp, and C.T. Foxton, "Resonant tunneling through two discrete energy states", *Phys. Rev. Lett*., vol. 74, pp. 4702-4705, June 1996; T.H. Oosterkamp, S.F. Godijn, M.J. Uilenreef, Yu.V. Nazarov, N.C. van der Vaart, and L.P. Kouwenhoven, "Changes in the magnetization of a double quantum dot", *LANL e-Print Archive* (http://xxx.lanl.gov), cond-mat/9802118, February 1998.

[26] R.H. Blick, R.J. Haug, J. Weis, D. Pfannkuche, K. v. Klitzing, and K. Eberl, *"*Single electron tunneling through a double quantum dot: The artificial molecule*"*, *Phys. Rev. B*, vol. 53, pp. 7899-7902, March 1996.

[27] Yu.V. Nazarov, "Anomalous current-voltage characteristics of tunnel junctions*", Zh. Eksp. Teor. Fiz*. vol. 95, pp. 975-984 [*Sov. Phys. - JETP*, vol. 68, pp. 561-567], March 1989.

[28] M.H. Devoret, D. Esteve, H. Grabert, G.-L. Ingold, H. Pothier, and C. Urbina, "Effect of the electromagnetic environment on the Coulomb blockade in ultrasmall tunnel junctions", *Phys. Rev. Lett*., vol. 64, pp. 1824-1827, April 1990.

[29] P. Lafarge, H. Pothier, E.R. Williams, D. Esteve, C. Urbina, and M.H. Devoret, "Direct observation of macroscopic charge quantization", *Z. Phys. B*, vol. 85, pp. 327-332, November 1991.

[30] K.K. Likharev, "Single-Electron Transistors: Electrostatic Analogs of the DC SQUIDs", *IEEE Trans. on Magn*., vol. 23, pp. 1142-1145, March 1987.

[31] T.A. Fulton and G.D. Dolan, "Observation of single-electron charging effects in small tunnel junctions", *Phys. Rev. Lett*., vol. 59, pp. 109-112, July 1987.

[32] G.D. Dolan, "Offset works for lift-off photoprocessing", Appl. Phys. Lett., vol. 31, pp. 337-339, September 1977.

[33] Y. Takahashi, M. Nagase, H. Namatsu, K. Kurihara, K. Iwdate, Y. Nakajima, S. Horiguchi, K. Murase, and M. Tabe, "A fabrication technique for Si single electron transistor operation at room temperature", *Electron. Lett*., vol. 31, pp. 136-138, January 1995.

[34] A. Ohata, H. Niyama, T. Shibata, K. Nakajima, and A. Torumi, "Silicon-based single-electron tunneling transistor operated at 4.2 K", Jpn. J. Appl. Phys., pt. 1, vol. 34, pp. 4485-4487, August 1995.

[35] E. Leobandung, L. Guo, Y. Wang, and S.Y. Chou, "Observation of quantum effects and Coulomb blockade in silicon quantum-dot transistors at temperatures over 100 K*", Appl. Phys. Lett*., vol. 67, pp. 938-940, August 1995; E. Leobandung, L. Guo, and S.Y. Chou, "Single hole quantum dot transistors in silicon", *Appl. Phys. Lett*., vol. 67, pp. 2338-2340, October 1995.

[36] K. Matsumoto, M. Ishii, K. Segawa, Y. Oka, B.J. Vartanian, and J.S. Harris, "Room temperature operation of a single electron transistor made by the scanning tunneling

microscope nanooxidation process for the TiO_x/Ti system", *Appl. Phys. Lett*. vol. 68, pp. 34-36, January 1996.

[37] Y. Takahashi, H. Namatsu, K. Kurihara, K. Iwdate, M. Nagase, and K. Murase, "Size dependence of the characteristics of Si silicon-electron transistors on SIMOX substrates", *IEEE Trans. on Electron. Dev*., vol. 43, pp. 1213-1217, August 1996.

[38] H. Ishikuro, T. Fujii, T. Sarya, G. Hashiguchi, T. Hiramoto, and T. Ikoma, "Coulomb blockade oscillations at room temperature in a Si quantum wire MOSFET transistor fabricated by anisotropic etching on a SOI substrate", *Appl. Phys. Lett*., vol. 68, pp. 3585-3587, June 1996.

[39] Y. Nakamura, C.D. Chen, and J.S. Tsai, "100-K operation of Al-based single-electron transistors", *Jpn. J. Appl. Phys*., vol. 35, pt. 2, pp. L1465-L1467, November 1996.

[40] E.S. Soldatov, V.V. Khanin, A.S. Trifonov, S.P. Gubin, V.V. Kolesov, D.E. Presnov, S.A. Yakovenko, and G.B. Khomutov, "Room temperature molecular single-electron transistor", *Pis'ma v Zh. Eksp. Teor. Fiz*., vol. 64, pp. 510-514 [*JETP Lett*., vol. 64, pp. 556-558], October 1996; E.S. Soldatov, V.V. Khanin, A.S. Trifonov, S.P. Gubin, V.V. Kolesov, D.E. Presnov, S.A. Yakovenko, G.B. Khomutov, and A.N. Korotkov, "Room Temperature Molecular Single-Electron Transistor", *LANL e-Print Archive* (http://xxx.lanl.gov), cond-mat/9610155, March 1997.

[41] K. Matsumoto, "STM/AFM nano-oxidation process to room-temperature-operated single-electron transistor and other devices", *Proc. IEEE*, vol. 85, pp. 612-628, April 1997.

[42] D.C. Ralph, C.T. Black, and M. Tinkham, "Gate-voltage studies of discrete electronic states in aluminum nanoparticles", *Phys. Rev. Lett*., vol. 78, pp. 4087-4090, May 1997.

[43] S. Altmeyer, A. Hamidi, B. Spangenberg, and H. Kurz, "77 K single electron transistors fabricated with 0.1 μm technology", *J. Appl. Phys*., vol. 81, pp. 8118-8120, June 1997.

[44] D. Klein, R. Roth, A.K.L. Lim, A.P. Alivisatos, and P. McEuen, "A single-electron transistor made from a cadmium selenide nanocrystal", *Nature*, vol. 389, pp. 699-701, October 1997.

[45] J. Shirakashi, K. Matsumoto, N. Miura, and M. Konagai, "Single-electron charging effects in Nb/Nb oxide-based single electron transistors at room temperature", Appl. Phys. Lett., vol. 72, pp. 1893-1995, April 1998.

[46] C. Schönenberger, H. van Houten, and H.C. Donkersloot, "Single-electron tunneling observed at room temperature by scanning-tunneling microscopy", *Europhys. Lett*., vol. 20, pp. 249-254, October 1992.

[47] R.P. Andres, T. Bein, M. Dorogi, S. Feng, J.I. Henderson, C.P. Kubiak, W. Mahoney, R.G. Osifchin, and R. Reifenberger, "Coulomb staircase at room temperature in a self-assembled molecular nanostructure", *Science*, vol. 272, pp. 1323-1325, May 1996;

[48] D. Porath and O. Millo, "Single electron tunneling and level spectroscopy of isolated C_{60} molecules", *J. Appl. Phys*., vol. 81, pp. 2241-2244, March 1997; D. Porath, Y. Levi, M. Tarabiah, and O. Millo, "Tunneling spectroscopy of isolated C_{60} molecules in the presence of charging effects", *Phys. Rev. B*, vol. 56, pp. 9829-9833, October 1997.

[49] A. Bezryadin, C. Dekker, and G. Schmid, "Electrostatic trapping of single conducting nanoparticles between nanoelectrodes", *Appl. Phys. Lett*., vol. 71, pp. 1273-1275, September 1997.

[50] D.V. Averin, A.N. Korotkov, and K.K. Likharev, "Theory of single-electron charging of quantum wells and dots", *Phys. Rev. B*, vol. 44, pp. 6199-6211, September 1991.

[51] C.W.J. Beenakker, "Theory of Coulomb-blockade oscillations in the conductance of a quantum dot", *Phys. Rev. B*, vol. 44, pp. 1646-1656, July 1991.

[52] T.A. Fulton, P.L. Gammel, and L.N. Dunkleberger, "Determination of Coulomb-blockade resistances and observation of the tunneling of single electrons in small-tunnel-junction circuit", *Phys. Rev. Lett*., vol. 67, pp. 3148-3151, November 1991.

[53] D.V. Averin and K.K. Likharev, "Possible Applications of the Single Charge Tunneling", in *Single Charge Tunneling*, ed. by H. Grabert and M.H. Devoret. New York: Plenum, 1992, pp. 311-322.

[54] L.J. Geerligs, V.G. Anderegg, P.A.M. Holweg, J.E. Mooij, H. Pothier, D. Esteve, C. Urbina, and M.H. Devoret, "Frequency-locked turnstile device for single electrons", *Phys. Rev. Lett.*, vol. 64, pp. 2691-2694, May 1990.

[55] K.K. Likharev and K.A. Matsuoka, "Electron-Electron Interaction in Linear Arrays of Small Tunnel Junctions", *Appl. Phys. Lett.*, vol. 67, pp. 3037-3039, May 1995.

[56] L.R.C. Fonseca, A.N. Korotkov, K.K. Likharev, and A.A Odintsov, " Numerical Study of the Dynamics and Statistics of Single Electron Systems", *J. Appl. Phys.*, vol. 78, pp. 3238-9125, September 1995.

[57] P. Lafarge, P. Joyez, H. Pothier, A. Cleland, T. Holst, D. Esteve, C. Urbina, and M. Devoret, "Observation directe de la quantification de la charge macroscopique*", C.R. Acad. Sci. Paris*, vol. 314, pp. 883-888, April 1992.

[58] P. Dresselhaus, J. Li, S. Han, L. Ji, J.E. Lukens, and K.K. Likharev, "Measurement of single electron lifetimes in a multijunction trap", *Phys. Rev. Lett.*, vol. 72, pp. 3226-3229, May 1994; L. Ji, P.D. Dresselhaus, S. Han, K. Lin, W. Zheng, and J. Lukens, "Fabrication and characterization of single-electron transistors and traps", *J. Vac. Sci. Technol. B*, vol. 12, pp. 3619-3622, November-December 1994.

[59] K.A. Matsuoka, K.K. Likharev, P. Dresselhaus, L. Ji, S. Han, and J. Lukens, "Single-electron traps: A quantitative comparison of theory and experiment", *J. Appl. Phys.*, vol. 81, pp. 2269-2281, March 1997.

[60] V.A. Krupenin, S.V. Lotkhov, and D.E. Presnov, "Factors of instability of single electron memory in $Al/AlO_x/Al$ structures at low temperatures", *Zh. Teor. Eksp. Fiz*. vol. 111, pp. 344-357 [*JETP*, vol. 84, p. 190], January 1997.

[61] H. Pothier, P. Lafarge, P.F. Orfila, C. Urbina, D. Esteve, and M.H. Devoret, "Single electron pump fabrication with ultrasmall normal tunnel junctions", *Physica B*, vol. 169, pp. 1598-574, February 1991.

[62] *Charge-Coupled Devices*, ed. by D.F. Barbe. Berlin: Springer, 1980.

[63] L.S. Kuzmin and D. Haviland, "Observation of the Bloch oscillations in an ultrasmall Josephson junction", *Phys. Rev. Lett.*, vol. 67, pp. 2890-2893, November 1991; D.B. Haviland *et al*. Z. Phys. B 85, 339 1991.

[64] L.S. Kuzmin and Yu.A. Pashkin, "Single electron tunneling oscillations in a current-biased Josephson junction", *Physica B*, vol. 194-196, pp. 1713-1714, February 1993.

[65] A.N. Cleland, J.M. Schmidt, and J. Clarke, "Influence of the environment on the Coulomb blockade in submicrometer normal-metal tunnel junctions", *Phys. Rev. B*, vol. 45, pp. 2950-2961, February 1992.

[66] T. Henning, "Coulomb Blockade Effects in Anodized Niobium Nanostructures", *LANL e-Print Archive* (http://xxx.lanl.gov), cond-mat/9710037, October 1997.

[68] P. Joyes, D. Esteve, and M.H. Devoret, "How is Coulomb blockade suppressed in high-conductance tunnel junctions?", *Phys. Rev. Lett.*, vol. 80, pp. 1956-1959, March 1998.

[69] W. Zheng, J.R. Friedman, D.V. Averin, S. Han, and J. Lukens, "Coulomb Blockade and Universal Scaling in Resistively Isolated Tunnel Junctions", Report at the APS March Meeting Los Angeles, March 1998, and to be published.

[70] P. Delsing, L.S. Kuzmin, K.K. Likharev, and T. Claeson, "Time-correlated single-electron tunneling in one-dimensional arrays of ultrasmall tunnel junctions", *Phys. Rev. Lett.*, vol. 63, pp. 1861-1865, October 1989.

[71] K. Matsuoka and K. Likharev, "Shot noise of single-electron tunneling in 1D arrays", *LANL e-Print Archive* (http://xxx.lanl.gov), cond-mat/9801219, January 1997.

[72] M. Tinkham, *Introduction to Superconductivity*, 2nd ed. McGraw-Hill, New York, 1996.

[73] A.N. Korotkov, "Charge sensitivity of superconducting single-electron transistor", *Appl. Phys. Lett.*, vol. 69, pp. 2593-2595, October 1996.

[74] D.V. Averin and Yu.V. Nazarov, "Single-electron charging of a superconductor island", *Phys. Rev. Lett.*, vol. 69, pp. 1993-1996, September 1992.

[75] M.T. Tuominen, J.M. Hergenrother, T.S. Tighe, and M. Tinkham, "Experimental evidence for parity-based 2*e* periodicity in a superconducting single-electron-tunneling transistor", *Phys. Rev. Lett.*, vol. 69, pp. 1997-2000, September 1992; J.G. Lu, J.M. Hergenrother, and M. Tinkham, "Magnetic-field-induced crossover from 2*e* to *e* periodicity in the superconducting single-electron transistor", *Phys. Rev. B*, vol. 53, pp. 3543-3549, February 1996.

[76] T.M. Eiles, J.M. Martinis, and M.H. Devoret, "Even-odd asymmetry of a superconductor revealed by the Coulomb blockade of Andreev reflection", *Phys. Rev. Lett.*, vol. 72, pp. 1862-1865, March 1993.

[77] P. Lafarge, P. Joyes, D. Esteve, C. Urbina, and M.H. Devoret, "Measurement of the even-odd free-energy difference of an isolated superconductor", *Phys. Rev. Lett.*, vol. 70, pp. 994-997, February 1993; "Two-electron quantization of the charge on a superconductor", *Nature*, vol. 365, pp. 422-424, September 1993.

[78] D.J. Flees, S. Han, and J. Lukens, "Interband transitions and band gap measurements in Bloch transistors", *Phys. Rev. Lett.*, vol. 78, pp. 4817-4820, June 1997.

[79] Y. Nakamura, C.D. Chen, and J.S. Tsai, "Spectroscopy of energy-level splitting between two macroscopic quantum states of charge coherently superposed by Josephson tunneling", *Phys. Rev. Lett.*, vol. 79, pp. 2328-2331, September 1997.

[80] K. Likharev, "Coexistence of Bloch and Josephson effects, and resistance quantization in small-area layered superconductor structures". Preprint #29/1986. Moscow: Department of Physics, Moscow State University, October 1986.

[81] K.K. Likharev and A.B. Zorin, "Simultaneous Bloch and Josephson oscillations, and resistance quantization in small superconducting double junctions", *Jpn. J. Appl. Phys.* vol. 26, suppl. 3, pp. 1407-1408, August 1987.

[82] P. Joyes, P. Lafarge, A. Filipe, D. Esteve, and M.H. Devoret, "Observation of parity-induced suppression of Josephson tunneling in the superconducting single-electron transistor", *Phys. Rev. Lett.* 72, 2458-2461, April 1994.

[83] J. Ziman, *Principles of the Theory of Solids*, 2nd ed. Cambridge, UK: Cambridge Univ. Press, 1972, Sec. 6.8.

[84] A.N. Korotkov, D.V. Averin, K.K. Likharev, and S.A. Vasenko, "Single-Electron Transistors as Ultrasensitive Electrometers", in *Single Electron Tunneling and Mesoscopic Devices*, ed. by H. Koch and H. Lübbig. Berlin: Springer, 1992, pp. 45-60; A.N. Korotkov, "Intrinsic noise of the single-electron transistor", *Phys. Rev. B*, vol. 49, pp. 10381-10392, April 1994.

[85] A.B. Zorin, F.-J. Ahlers J. Niemeyer, T. Weimann, and H. Wolf, "Background charge noise in metallic single-electron tunneling devices", *Phys. Rev. B*, vol. 53, pp. 13682-13687, May 1996.

[86] H. Birk, M.J.M. de Jong, and C. Schoenenberger, "Shot noise suppression in the single-electron tunneling regime", *Phys. Rev. Lett.*, vol. 75, pp. 1610-1613, August 1995.

[87] G. Zimmerli, T.M. Elies, R.L. Kautz, and J.M. Martinis, "Noise in Coulomb blockade electrometer", *Appl. Phys. Lett.*, vol. 61, pp. 237-239, July 1992.

[88] E.H. Visscher, S.M. Verbrugh, J. Lindeman, P. Hadley, J.E. Mooij, "Fabrication of multilayer single-electron tunneling devices", *Appl. Phys. Lett.*, vol. 66, pp. 305-307, January 1995.

[89] E.H. Visscher, J. Lindeman, S.M. Verbrugh, P. Hadley, and J.E. Mooij, "Broadband single-electron tunneling transistor", *Appl. Phys. Lett.*, vol. 68, pp. 2014-2016, April 1966.

[90] R.C. Ashoori, H.L. Stormer, J.C. Weiner, L.N. Pfeiffer, K.W. Baldwin, S.J. Pearton, and K.W. West, "Single-electron capacitance spectroscopy of discrete quantum levels", *Phys. Rev. Lett.*, vol. 68, pp. 3088-3091, May 1992.

[91] D.J. Mar, R.M. Westervelt, and P.F. Hopkins, "Cryogenic field-effect transistor with single electronic charge sensitivity", *Appl. Phys. Lett.*, vol. 64, pp. 631-633, January 1994.

[92] R. J. Schoelkopf, P. Wahlgren, A.A. Kozhevnikov, P. Delsing, ad D.E. Prober, "The RF-SET: A fast and ultra-sensitive electrometer", accepted for publication in *Science*, April 1998.

[93] J. Pettersson, P. Wahlgreen, P. Delsing, N. Rorsman, D.B. Haviland, H. Zirath, and T. Claeson, "Extending the high frequency limit of a single electron transistor by on-chip impedance transformation, *Phys. Rev. B*, vol. 53, pp. R13272-R13274, May 1996; B. Starmark, P. Delsing, D.B. Haviland, and T. Claeson, "Noise measurements of single electron transistors using a transimpedance amplifier", in: *Ext. Abstr. ISEC'97*. Berlin: PTB, 1997, pp. 391-393.

[94] A.N. Cleland, D. Esteve, C. Urbina, and M.H. Devoret, "Very low noise photodetector based on the single electron transistor", *Appl. Phys. Lett.*, vol. 61, pp. 2820-2822, December 1992.

[95] V.J. Goldman and B. Su, "Resonant tunneling in the quantum Hall regime: measurement of fractional charge", *Science*, vol. 267, pp. 1010-1012, February 1995.

[96] M. Field, C.G. Smith, M. Pepper, K.M. Brown, E.H. Linfield, M.P. Grimshaw, D.A. Ritchie, and G.A.C. Jones, "Coulomb blockade as a noninvasive probe of local density of states", *Phys. Rev. Lett.*, vol. 77, pp. 350-353, July 1996.

[97] Y.Y. Wei, J. Weis, K. v. Klitzing, and K. Eberl, "Single-electron transistor as an electrometer measuring chemical potential variations", *Appl. Phys. Lett.*, vol. 71, pp. 2514-2516, October 1997; "Edge strips in the quantum-Hall regime imaged by a single-electron transistor", submitted to *Phys. Rev. Lett.*, March 1998.

[98] M.J. Yoo, T.A. Fulton, H.F. Hess, R.L. Willett, L.N. Dunklebrger, R.J. Chichester, L.N. Pfeiffer, and K.W. West, "Scanning single-electron transistor microscopy: Imaging individual charges", *Science*, vol. 276, pp. 579-582, April 1997.

[99] P. L. McEuen, E.B. Foxman, U. Meirav, M.A. Kastner, Y. Meir, N.S. Wingreen, and S.J. Wind, "Transport spectroscopy of a Coulomb island in the quantum Hall regime", *Phys. Rev. Lett.*, vol. 66, pp. 1926-1929, April 1991.

[100] N.B. Zhitenev, R.C. Ashoori, L.N. Pfeiffer, and K.W. West, "Periodic and aperiodic bunching in the addition spectra of quantum dots", *Phys. Rev. Lett.*, vol. 79, pp. 2308-2311, September 1997.

[101] J.A. Folk, S.R. Patel, S.F. Godijn, A.G. Huibers, S.M. Cronenwett, C.M. Markus, K. Campman, and A.C. Gossard, "Statistics and parametric correlations of Coulomb blockade peak fluctuations in quantum dots", *Phys. Rev. Lett.*, vol. 76, pp. 1699-1702, March 1996; S.R. Patel, S.M. Cronenwett, D.R. Stewart, A.G. Huibers, C.M. Marcus, C.I. Duruös, J.S. Harris, K. Campman, and A.C. Gossard, "Mesoscopic fluctuations of Coulomb blockade peak spacings", *LANL e-Print Archive* (http://xxx.lanl.gov), cond-mat/9708090, August 1997.

[102] U. Meirav, M.A. Kastner, and S.J. Wind, "Single electron charging and periodic conductance resonances in GaAs nanostructures", *Phys. Rev. Lett.*, vol. 65, pp. 771-774, August 1996.

[103] B. Su, V.J. Goldman, and J.E. Cunningham, "Observation of single-electron charging in double-barrier heterostructures", *Science*, vol. 255, pp. 313-315, January 1992.

[104] D.C. Ralph, C.T. Black, and M. Tinkham, "Spectroscopic measurements of discrete electronic states in single metal particles", *Phys. Rev. Lett.*, vol. 74, pp. 3241-3244, April 1995; C.T. Black, D.C. Ralph, and M. Tinkham, "Spectroscopy of the superconducting gap

in individual nanometer aluminum particles", *Phys. Rev. Lett*. vol. 76, pp. 688-691, January 1996.

[105] D.L. Klein, P.L. McEuen, J.E. Bowen Katari, R. Roth, and A.P. Alivisatos, "An approach to electrical studies of single nanocrystals", *Appl. Phys. Lett.*, vol. 68, pp. 2574-2576, April 1996.

[106] M. Bockrath, D.H. Cobden, P.L. McEuen, N.G. Chopra, A. Zettl, A. Tess, and R.E. Smalley, "Single electron tunneling transport in ropes of carbon nanotubes", *Science*, vol. 275, pp. 1922-1925, March 1997; D.H. Cobden, M. Bockrath, P.L. McEuen, A.G. Rinzer, and R.E. Smalley, "Spin splitting and even-odd effects in carbon nanotubes", *LANL e-Print Archive* (http://xxx.lanl.gov), cond-mat 98/9804154, April 1998.

[107] S.J. Tans, M.H. Devoret, H. Dai, A. Thess, R.S. Smalley, L.J. Geerligs and C. Dekker, "Individual single-wall carbon nanotubes as quantum wires", *Nature*, vol. 386, pp. 474-476, April 1997.

[108] C.W.J. Beenakker, "Random-matrix theory of quantum transport", *Rev. Mod. Phys.*, vol. 69, pp. 731-808, July 1997.

[109] S. Tarucha, D.G. Austing, T. Honda, R.J. van der Hage, and L.P. Kouwenhoven, "Shell filling and spin effects in a few electron quantum dot", *Phys. Rev. Lett.*, vol. 77, pp. 3613-3616, October 1996; L.P. Kouwenhoven, T.H. Oosterkamp, M.W.S. Danoesastro, M. Eto, D.G. Austing, T. Honda, and S. Tarucha, "Excitation Spectra of Circular Few-Electron Quantum Dots", *Science*, vol. 278, pp. 1788-1792, December 1997.

[110] H.D. Jensen and J.M. Martinis, "Accuracy of the electron pump", *Phys. Rev. B*, vol. 46, pp. 13407-13427, November 1992.

[111] D.V. Averin, A.A. Odintsov, and S.V. Vyshenskii, "Ultimate accuracy of single-electron dc current standard", *J. Appl. Phys*., vol. 73, pp. 1297-1308, February 1993.

[112] H. Pothier, P. Lafarge, D. Esteve, C. Urbina, and M.H. Devoret, "Passing electrons one by one: Is a 10^{-8} accuracy achievable?", *IEEE Trans. on Instr. Meas*., vol. 42, pp. 324-330, April 1993.

[113] C.R. Fonseca, A.N. Korotkov, and K.K. Likharev, "A numerical study of the accuracy of single-electron current standards", *J. Appl. Phys*., vol. 79, pp. 9155-9165, June 1996; "Accuracy of the single-electron pump using an optimized step-like rf drive waveform", *Appl. Phys. Lett.*, vol. 69, pp. 1858-1860, September 1996.

[114] M.W. Keller, J.M. Martinis, N.M. Zimmerman, and A.H. Steinbach, "Accuracy of electron counting using a 7-junction electron pump", *Appl. Phys. Lett.*, vol. 69, pp. 1804-1806, September 1996.

[115] A.F. Clark, N.M. Zimmerman, E.R. Williams, A. Amar, D. Song, F.C. Wellstood, C.J. Lobb, and R.J. Soulen, Jr., "Application of single electron tunneling: Precision capacitance ratio measurements, *Appl. Phys. Lett.*, vol. 66, pp. 2588-2590, May 1995.

[116] J.M. Shilton, V.I. Talyanskii, M. Pepper, D.A. Ritchie, J.E.F. Frost, C.J.B. Ford, C.G. Smith, and G.A.C. Jones, "High-frequency single-electron transport in a quasi-one-dimensional GaAs channel induced by surface acoustic waves", J. Phys.: Condens. Matter, vol. 8, pp. L531-L539, August 1996.

[117] J.K. Pekola, K.P. Hirvi, J.P. Kauppinen, and M.A. Paalanen, "Thermometry by arrays of tunnel junctions", *Phys. Rev. Lett.*, vol. 73, pp. 2903-2906, November 1994.

[118] K.P. Hirvi, J.P. Kauppinen, A.N. Korotkov, M.A. Paalanen, and J.P. Pekola, "Arrays of normal tunnel junctions in weak Coulomb blockade regime", *Appl. Phys. Lett.*, vol. 67, pp. 2096-2098, October 1995; K.P. Hirvi, M.A. Paalanen, and J.P. Pekola, "Numerical investigation of one-dimensional tunnel junction arrays at temperatures above the Coulomb blockade regime", *J. Appl. Phys*., vol. 80, pp. 256-263, July 1996.

[119] Sh. Farhangfar, K.P. Hirvi, J.P. Kauppinen, J.P. Pekola, J.J. Toppari, D.V. Averin, and A.N. Korotkov, "One dimensional arrays and solitary tunnel junctions in the weak

Coulomb blockade regime: CBT thermometry", *J. Low Temp. Phys*., vol. 108, pp. 191-215, July 1997.

[120] K.K. Likharev and I.A. Devyatov, "Photoresponse and photosensitivity of single-electron-tunneling systems", *Physica B*, vol. 194-196, pp. 1341-1342, February 1994.

[121] P.K. Tien and J.R. Gordon, "Multiphoton process observed in the interaction of microwave fields with the tunneling between superconductor fields", *Phys. Rev*., vol. 129, pp. 647-651, January 1963.

[122] L.P. Kouwenhoven, S. Jauhar, K. McCormic, D. Dixon, P.L. McEuen, Yu.V. Nazarov, N.C. van der Vaart, and C.T. Foxton, "Photon-assisted tunneling through a quantum dot", *Phys. Rev. B*, vol. 50, pp. 2019-2022, July 1994.

[123] A. Fujiwara, Y. Takahashi, and K. Murase, "Observation of single electron-hole recombination and photon-pumped current in an asymmetric Si single-electron transistor", *Phys. Rev. Lett*., vol. 78, pp. 1532-1535, February 1997.

[124] T.H. Oosterkamp, L.P. Kouwenhoven, A.E.A. Koolen, N.C. van der Vaart, and C.J.P.M. Harmans, "Photon sidebands of the ground state and first excited state of a quantum dot", *Phys. Rev. Lett*., vol. 78, pp. 1536-1539, February 1997.

[125] J.R. Tucker and M.J. Feldman, "Quantum detection at millimeter wavelengths", *Rev. Mod. Phys*., vol. 57, pp. 1055-1113, October 1985.

[126] I.A. Devyatov, L.S. Kuzmin, K.K. Likharev, V.V. Migulin, and A.B. Zorin, "Quantum-statistical theory of microwave detection using superconducting tunnel junctions", J. Appl. Phys., vol. 60, pp. 1808-1828, September 1986.

[127] K.K. Likharev, *Dynamics of Josephson Junctions and Circuits*, New York: Gordon and Breach, 1986, Chapter 16.

[128] J.R. Tucker, "Complementary digital logic based on the Coulomb blockade", *J. Appl. Phys*., vol. 72, pp. 4399-4413, November 1992.

[129] A.N. Korotkov, "Theoretical analysis of the resistively-coupled single-electron transistor", *LANL e-Print Archive*, cond-mat/9803038, March 1998.

[130] A.N. Korotkov, R.H. Chen, and K.K. Likharev, "Possible Performance of Capacitively-Coupled Single-Electron Transistors in Digital Circuits", J. Appl. Phys., vol. 78, pp. 2520-2530, August 1995; R.H. Chen, A.N. Korotkov, and K.K. Likharev, "Single-electron-transistor logic", *Appl. Phys. Lett*., vol. 68, pp. 1954-1956, April 1996.

[131] H. Iwamura, M. Akazawa, and Y. Amemiya, "Single-electron majority logic circuits", *IEICE Trans. on Electron*., vol. E81-C, pp. 42-48, January 1998.

[132] R.H. Chen and K.K. Likharev, "Multiple-Junction Single-Electron Transistors for Digital Applications", Appl. Phys. Lett., vol. 72, pp. 61-63, January 1998.

[133] K.K. Likharev and V.K. Semenov, "Possible logic circuits based on the correlated single-electron tunneling in ultrasmall junctions", in *Ext. Abstr. ISEC'87*. Tokyo, 1987, pp. 128-131.

[134] S.V. Vyshenskii, S.P. Polonsky, and K.K. Likharev, "Single electron logic circuits", June 1990, unpublished (described in detail in Ref. 53).

[135] P. Bakshi, D.A. Broido, and K. Kempa, "Spontaneous polarization of electrons in quantum dashes", J. Appl. Phys., vol. 70, pp. 5150-5152, November 1991.

[136] C.S. Lent, P.D. Tougaw, W. Porod, and G. Bernstein, "Quantum Cellular Automata", *Nanotechnology*, vol. 4, pp. 49-57, January 1993; P.D. Tougaw and C.S. Lent, "Logical devices implemented using quantum cellular automata", *J. Appl. Phys*., vol. 75, pp. 1818-1825, February 1994; C.S. Lent and P.D. Tougaw, "Dynamic behavior of quantum cellular automata", *J. Appl. Phys*., vol. 80, pp. 4722-4736, October 1996.

[137] K. Nomoto, R. Ugajin, T. Suzuki and I. Hase, "Novel logic device using coupled quantum dots", Electron. Lett., vol. 29, pp. 1380-1381, July 1993; "Single electron-photon logic device using quantum dots: Computing with Fock ground states", *J. Appl. Phys*., vol. 79, pp. 291-300, January 1996.

[138] D.V. Averin, L.F. Register, K.K. Likharev, and K. Hess, "Single-electron Coulomb exclusion on the atomic level", *Appl. Phys. Lett.*, vol. 64, pp. 126-128, January 1994.
[139] S. Bandyopadhyay, B. Das, and A.E. Miller, "Supercomputing with spin-polarized single electrons in a quantum coupled structure", *Nanotechnology*, vol. 4, pp. 113-133, April 1994; S. Bandyopadhyay and V. Roychowdhury, "Computational paradigms in nanoelectronics: quantum coupled single electron logic and neuromorphic networks", *Jpn. J. Appl. Phys*., pt. 1, vol. 35, pp. 3350-3362, June 1996.
[140] A.N. Korotkov, "Wireless single-electron logic biased by ac electric field", *Appl. Phys. Lett*., vol. 67, pp. 2412-2414, October 1995.
[141] M.G. Ancona, "Design of computationally useful single-electron digital circuit", *J. Appl. Phys*., vol. 78, pp. 3311-3314, December 1995.
[142] K.K. Likharev and A.N. Korotkov, "Single-Electron Parametron: Reversible Computation in a Discrete State System", *Science*, vol. 273, pp. 763-765, August 1996; A.N. Korotkov and K.K. Likharev, "Single-Electron- Parametron-Based Logic", *LANL e-Print Archive* (http://xxx.lanl.gov), cond-mat 98/05053, May 1998.
[143] A.V. Krasheninnikov and L.A. Openov, "Elementary quantum-dot gates for single-electron computing", Pis'ma v Zh. Eksp. Teor. Fiz., vol. 64, pp. 214-218 [JETP Lett., vol. 64, pp. 231-236], August 1996.
[144] S.N. Molotkov and S.S. Nazin, "Single-electron computing: Quantum dot logic gates", Zh. Eksp. Teor. Fiz., vol. 110, pp. 1439-1452 [JETP, vol. 83, pp. 794-802], October 1996.
[145] C.S. Lent and P.D. Tougaw, "A device architecture for computing with quantum dots", *Proc. IEEE*, vol. 85, pp. 541-557, April 1997.
[146] N.-J. Wu, N. Asahi, and Y. Amemiya, "Cellular-automation circuits using single-electron-tunneling junctions", Jpn. J. Appl. Phys., vol. 36, pp. 2621-2627, May 1997.
[147] N. Asahi, M. Akazawa, and Y. Amemiya, "Single-electron logic device based on the binary decision diagram", *IEEE Trans. on Electron. Dev*., vol. 44, pp. 1109-1116, July 1997; *IEICE Trans. on Electron*., vol. 81, pp. 49-56, January 1998.
[148] V.P. Roychowdhury and M.P. Anantram, "On computing with locally-interconnected architectures in atomic/nanoelectronic systems", in *Proc. IEEE Conf. On Application-Specific Systems, Architectures, and Processors*, ed. by L. Thiele *et al.* Los Alamitos, CA: IEEE Comp. Soc., 1997, pp. 14-23.
[149] A.M. Bychkov, L.A. Openov, and I.A. Semenihin, "Single-electron computing without dissipation", Pis'ma v Zh. Eksp. Teor. Fiz., vol. 66, pp. 275-279 [JETP Lett., vol. 66, pp. 298-303], November 1997.
[150] Y. Fu and M. Willander, "Modeling and design of quantum dot cellular automata", *J. Appl. Phys*., vol. 83, pp. 3186-3191, March 1998.
[151] K.K. Likharev and V.K. Semenov, "RSFQ Logic/Memory Family: A New Josephson-Junction Technology for Sub-Terahertz-Clock-Frequency Digital Systems", *IEEE Trans. on Appl. Supercond.*, vol. 1, pp. 3-28, March 1991; K.K. Likharev, "Superconductors Speed up Computation", *Phys. World*, vol. 10, pp. 39-43, May 1997.
[152] A. Barenko, D. Deutch, A. Ekert, and R. Josa, "Conditional quantum dynamics and logic gates, *Phys. Rev. Lett*., vol. 74, pp. 4083-4086, May 1995.
[153] A. Shnirman, G. Schön, and Z. Hermon, "Quantum manipulation of small Josephson junctions", *Phys. Rev. Lett*., vol. 79, pp. 2371-2374, September 1997.
[154] D. Loss and D.P. DiVincenzo, "Quantum computation with quantum dots", *Phys. Rev. A*, vol. 57, pp. 120-126, January 1998.
[155] D.V. Averin, "Adiabatic quantum computation with Cooper pairs", *Solid State Comm*., vol. 105, pp. 659-664, March 1998.
[156] M.J. Kirton and M.J. Uren, "Noise in solid-state microstructures", *Adv. in Physics*, vol. 38, pp. 367-468, July 1989.

[157] V.A. Krupenin, D.E. Presnov, M.N. Savvateev, H. Scherer, A.B. Zorin, and J. Niemeyer, "Noise in Al single electron transistors of stacked design", *LANL e-Print Archive* (http://xxx.lanl.gov), cond-mat/9804197, April 1998.

[158] L.S. Kuzmin and K.K. Likharev, "Direct experimental observation of the correlated discrete single- electron tunneling", Pis'ma v Zh. Eksp. Teor. Fiz., vol. 45, pp. 389-390 [*JETP Lett*., vol. 45, pp. 495-497], April 1987.

[159] R.A. Kiehl and T. Ohshima, "Bistable locking of single-electron tunneling elements for digital circuitry", *Appl. Phys. Lett*., vol. 67, pp. 2494-2496, October 1995; T. Ohshima and R.A. Kiehl, "Operation of bistable phase-locked single-electron tunneling logic elements", *J. Appl. Phys*., vol. 80, pp. 912-923, July 1996; T. Ohshima, "Stability of binary logic tunneling phase states in dc-biased and ac-pumped single-electron tunnel junctions", *Appl. Phys. Lett*., vol. 69, pp. 4059-4061, December 1996.

[160] K.E. Nagaev, "On the shot noise in dirty metal contacts", *Phys. Lett. A*, vol. 169, pp. 103-107, September 1992; "Influence of electron-electron scattering on shot noise in diffusive conductors", *Phys. Rev. B*, vol. 52, pp. 4740-4743, August 1995.

[161] Y. Naveh, D.V. Averin, and K.K. Likharev, "Effect of Screening on Shot Noise of Diffusive Mesoscopic Conductors", *Phys. Rev. Lett*., vol. 79, pp. 3482-3485, November 1997; "Noise properties and ac conductance of mesoscopic diffusive conductors with screening", *LANL e-Print Archive* (http://xxx.lanl.gov), cond-mat/9801188 (January 1998); "Shot noise in diffusive conductors: A quantitative analysis of electron-phonon interaction effects", *LANL e-Print Archive* (http://xxx.lanl.gov), cond-mat/9803335 (March 1998).

[162] M.V. Fischetti, S.E. Laux, and E. Crabbe, "Understanding hot-electron transport in silicon devices: Is there a shortcut?", *J. Appl. Phys*., vol. 78, pp. 1058-1087, July 1995.

[163] W. Chen, H. Ahmed, and K. Nakazato, "Enhancement of Coulomb blockade in semiconductor tunnel junctions", *Appl. Phys. Lett*., vol. 66, pp. 3170-3172, June 1995.

[164] K.K. Likharev and A.N. Korotkov, "Ultradense Hybrid SET/FET Dynamic RAM: Feasibility of Background-Charge-Independent Room-Temperature Single-Electron Digital Circuits", in *Proc. of 1995 ISDRS*. Charlottesville, VA: Univ. of Virginia, 1995, pp. 355-358; "Hybrid SET/FET Memory", paper in preparation.

[165] C.D. Chen, Y. Nakamura, and J.S. Tsai, "Aluminum single-electron nonvolatile floating gate memory cell", *Appl. Phys. Lett*., vol. 71, pp. 2038-2040, October 1997.

[166] A.K. Sharma, *Semiconductor Memories*. New York: IEEE, 1997, Ch. 3.

[167] K.K. Likharev, "Novel silicon-based nanoscale devices for terabit integration", in *GOMAC'98 Digest of Papers*. Arlington, VA: Defense Technical Information Center, pp. 395-398, March 1998; "Crested Tunnel Barriers for Nonvolatile Semiconductor Memories", to be published.

[168] F. Capasso, F. Beltram, R.J. Malik, and J.F. Walker, "New floating-gate AlGaAs/GaAs memory devices with graded-gap electron injector and long retention times", IEEE Electron Device Lett., vol. 9, pp. 377-379, August 1988.

[169] Y. Taur, D.A. Buchanan, W. Chen, D.J. Frank, K.E. Ismail, S.-H. Lo, G.A. Sai-Halasz, S.G. Viswanathan, H.-J.C. Wann, S.J. Wind, and H.-S. Wong, "CMOS scaling into the nanometer regime", *Proc. IEEE*, vol. 85, pp. 486-504, April 1997.

[170] F. Pikus and K. Likharev, "Nanoscale Field-Effect Transistors: An Ultimate Size Analysis", *Appl. Phys. Lett*., vol. 71, pp. 3661-3663, December 1997; "Nanoscale Field-Effect Transistors with Ballistic Transport", paper in preparation.

[171] K. Yano, T. Ishii, T. Hashimoto, T. Kobayashi, F. Murai, and K. Seki, "Room-temperature single-electron memory", *IEEE Trans. on Electron. Dev*., vol. 41, pp. 1628-1638, September 1994.

[172] T. Ishii, K. Yano, T. Sano, T. Mine, F. Murai, T. Kure, and K. Seki, "A 3-D Single-electron-memory cell structure with $2F^2$ per bit", in *Techn. Digest of IEDM 97*, New York: IEEE, 1997, pp. 924-925; T. Ishii, K. Yano, T. Sano, T. Mine, F. Murai, and K. Seki,

"Verify: Key to the stable single-electron-memory operation", in *Techn. Digest of IEDM 97*, New York: IEEE, 1997, pp. 171-174.

[173] K. Yano, T. Ishii, T. Sano, T. Mine, F. Murai, T. Kure, and K. Seki, "A 128-Mb early prototype for gigascale single-electron memories", in ISSCC'98 Digest of Technical Papers. New York: IEEE, 1998, pp. 344-345, 462.

[174] S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E.F. Crabbé, and K. Chan, "A silicon nanocrystals based memory", *Appl. Phys. Lett*., vol. 68, pp. 1377-1379, March 1996; S. Tiwari, F. Rana, K. Chan, L. Shi, and H. Hanafi, "Single charge and confinement effects in nano-crystal memories", *Appl. Phys. Lett*., vol. 68, pp. 1232-1234, August 1996; H.I. Hanafi, S. Tiwari, and I. Khan, "Fast and long retention-time nano-crystal memory", *IEEE Trans. on Electron. Dev*., vol. 43, pp. 1553-1558, September 1996.

[175] L. Guo, E. Leobandung, and Y. Chou, "A single-electron transistor memory operating at room temperature", *Science*., vol. 275, pp. 649-651, January 1997.

[176] A. Nakajima, T. Futatsugi, K. Kosemura, T. Fukano, and N. Yokoyama, "Room temperature operation of Si single-electron memory with self-aligned floating dot gate", *Appl. Phys. Lett*., vol. 70, pp. 1742-1744, March 1997.

[177] Semiconductor Industry Association. *The National Technology Roadmap for Semiconductors. 1997 Edition.* San Jose, CA: Sematech, 1997; available on the Web site notes.smatech.org/97melec.htm.

[178] K.K. Likharev and A.N. Korotkov, "Analysis of Q_0-independent single-electron systems", in *Abstr. of Int. Workshop on Comput. Electron.* Tempe, AZ, 1995, p. 42; VLSI Design (Amsterdam) **3**, pp. 201-204, December 1997.

[179] R.C. Barrett and C.F. Quate, "Charge storage in a nitride-oxide-silicon medium by scanning capacitance microscopy", *J. Appl. Phys*., vol. 70, pp. 2725-2733, September 1991.

Figures

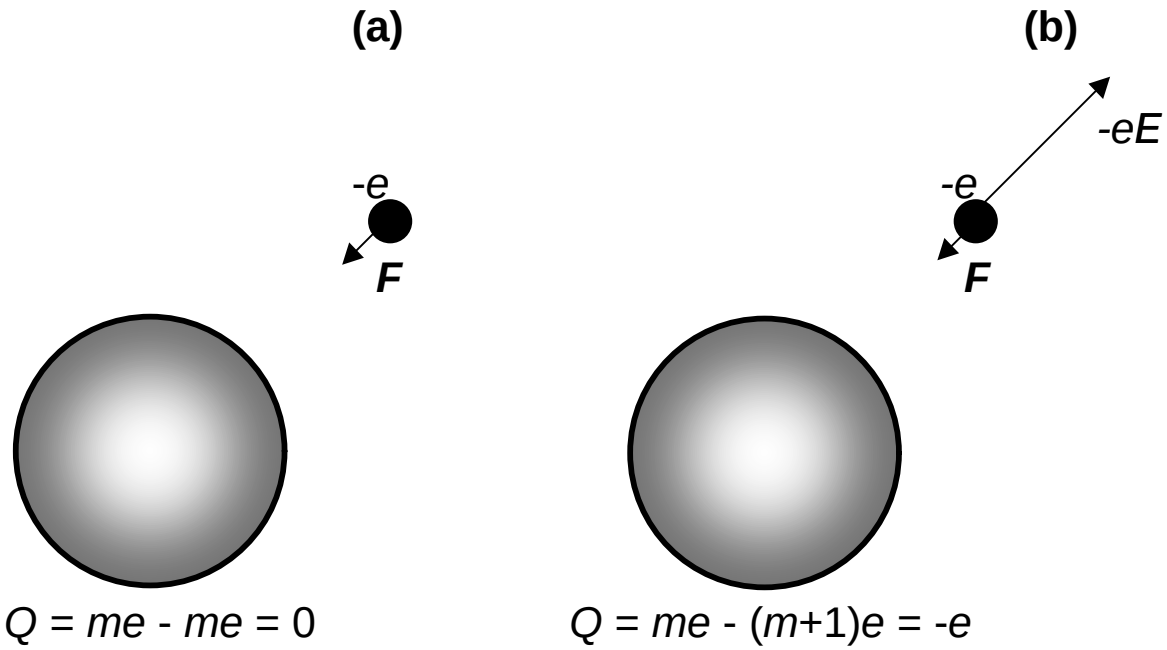


Fig. 1. The basic concept of single-electron control: a conducting island (a) before and (b) after the addition of a single electron. The addition of a single uncompensated electron charge creates an electric field ***E*** which may prevent the addition of the following electrons.

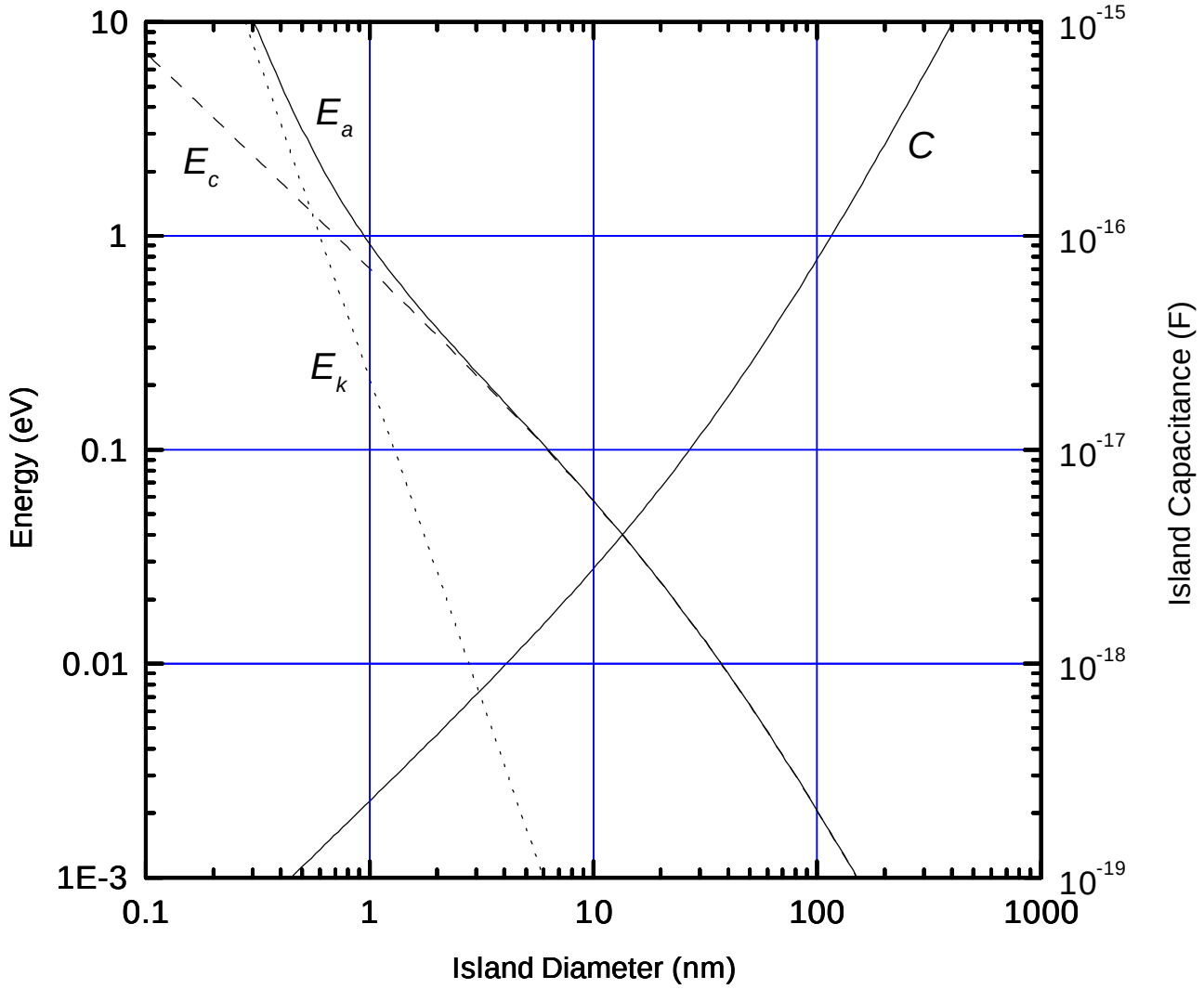


Fig. 2. Single-electron addition energy E_a (solid line), and its components: charging energy E_c (dashed line) and electron kinetic energy E_k (dotted line), as calculated using Eqs. (1) and (2) for a simple model of a conducting island. In this model the island is a round 3D ball with a free, degenerate electron gas (electron density $n = 10^{22}$ cm^{-3}, electron effective mass $m = m_0$), embedded into a dielectric matrix (dielectric constant $\varepsilon = 4$), with 10% of its surface area occupied by tunnel junctions with a barrier thickness $d = 2$ nm.

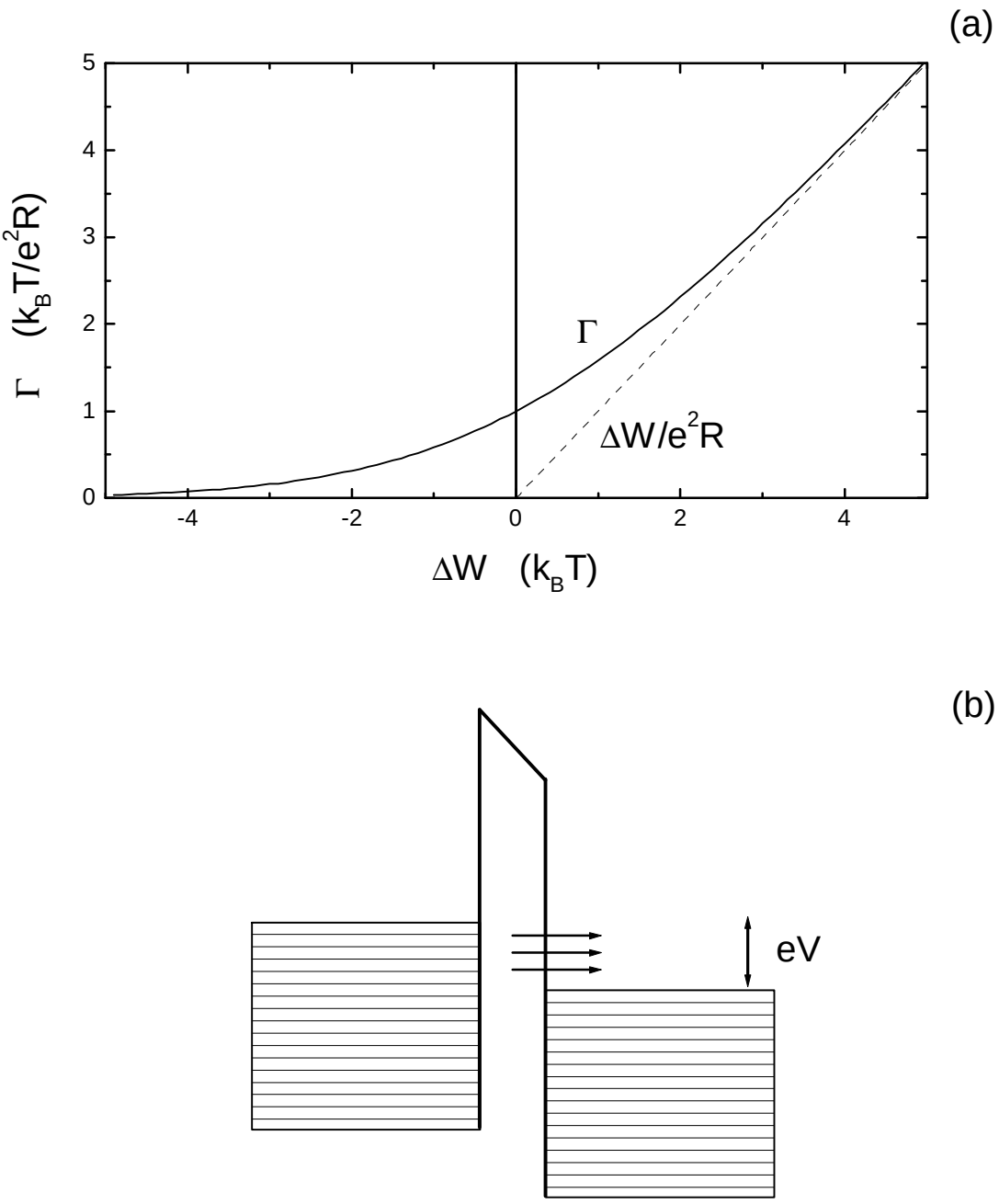


Fig. 3. (a) Single-electron tunneling rate Γ as a function of the electrostatic energy loss ΔW, according to Eq. (5) of the orthodox theory, and (b) an energy diagram of a tunnel junction, explaining why $\Gamma \propto \Delta W$ at $\Delta W >> k_B T$: the rate is proportional to the number of occupied quantum states in the electron source, which contribute to the total probability of tunneling into empty states of the collector.

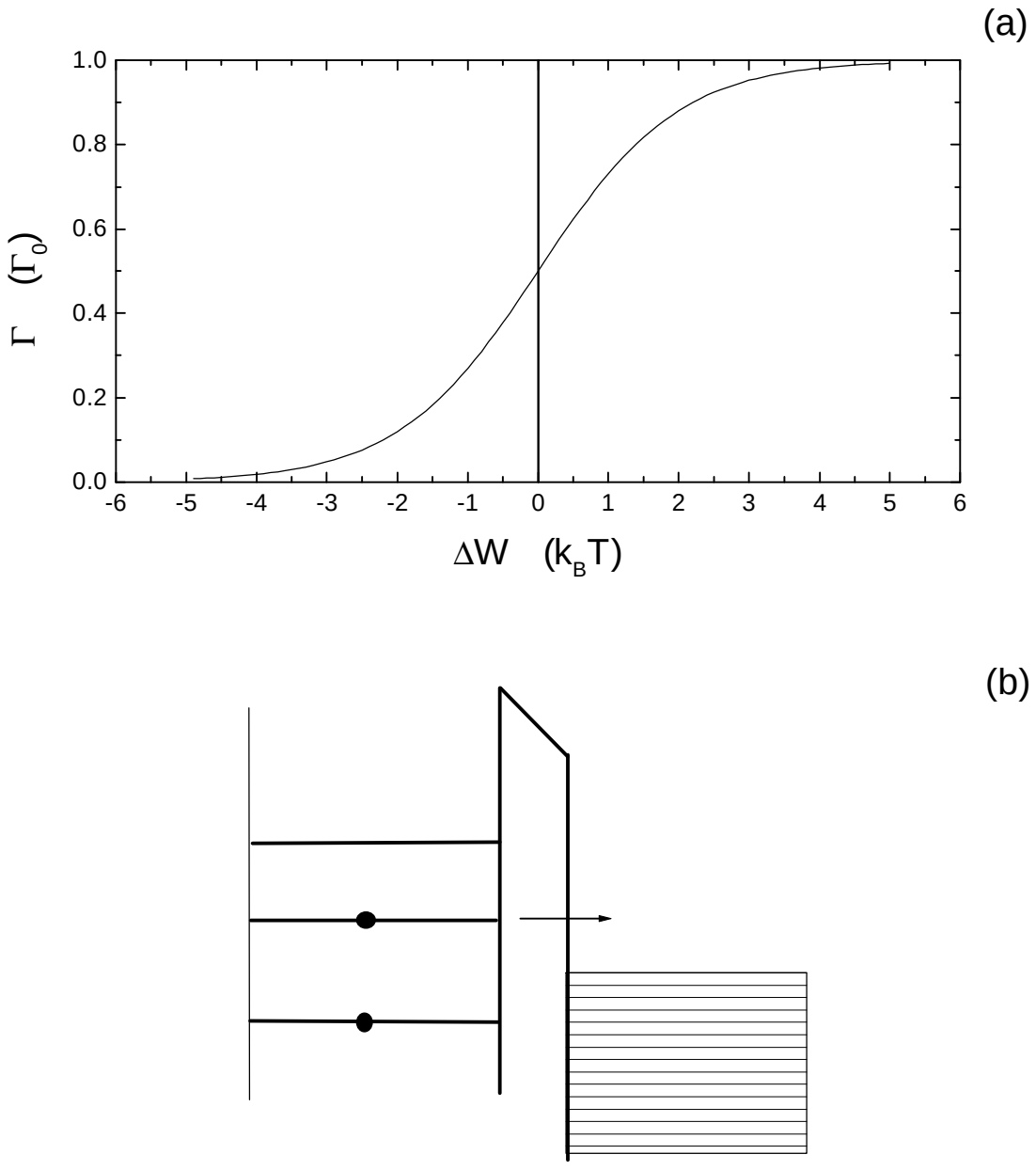


Fig. 4. (a) The rate Γ of electron tunneling from/to a discrete energy level to/from a Fermi-sea continuum according to Eq. (8), and (b) an energy diagram of a tunnel junction explaining why in this case $\Gamma = \Gamma_0 \approx$ const at $\Delta W >> k_B T$ (cf. Fig. 3).

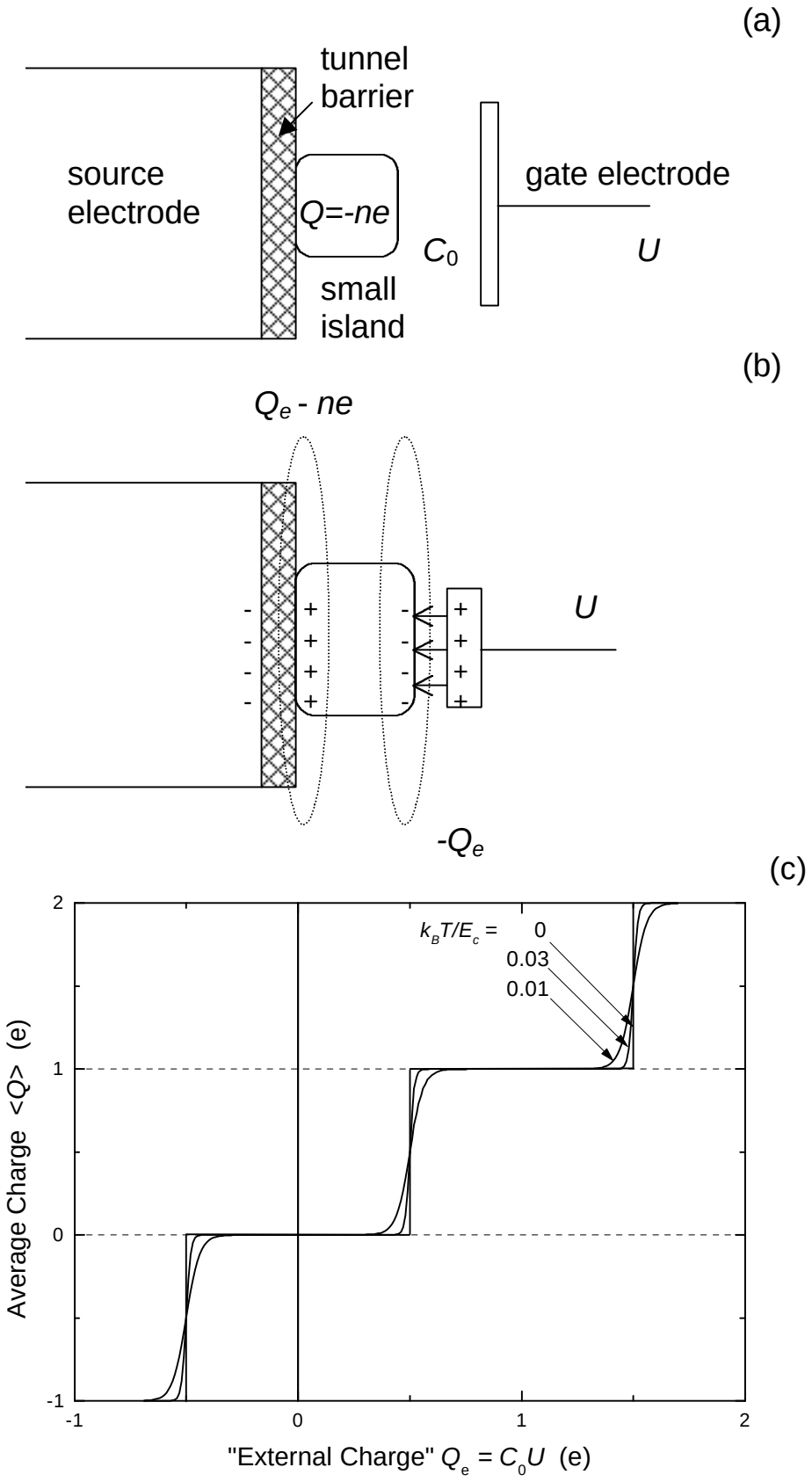
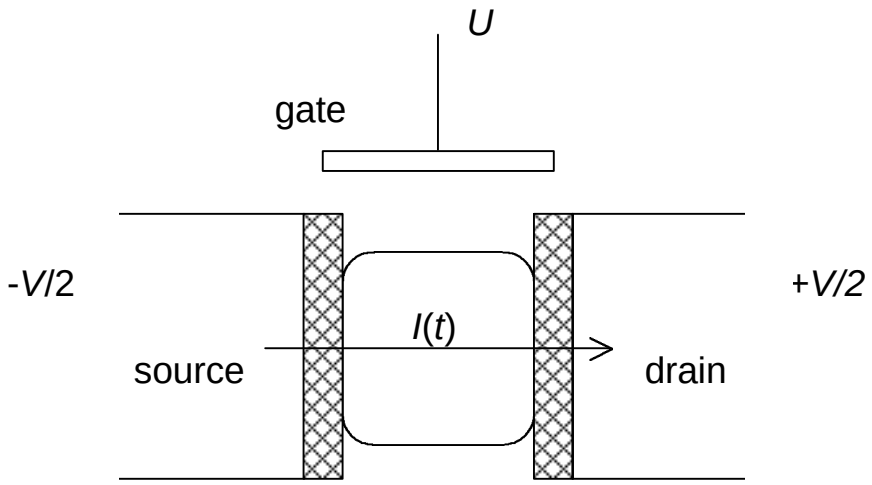
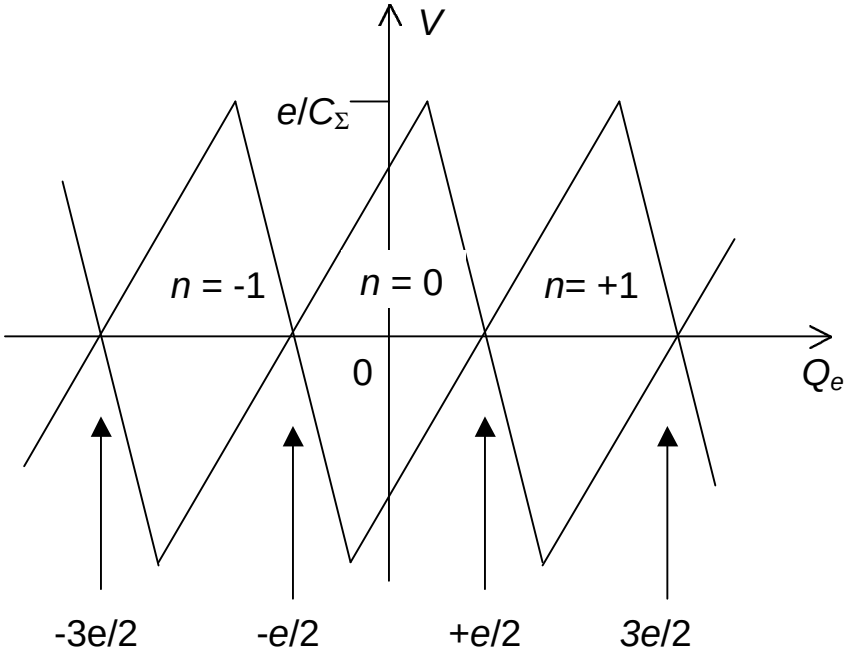


Fig. 5. Single-electron box: (a) schematics, (b) a particular geometry in which the "external charge" $Q_e = C_0U$ can be readily visualized, and (c) the "Coulomb staircase", i.e. the step-like dependence of the average charge $Q = -ne$ on the gate voltage, for several values of temperature.

(a)



(c)



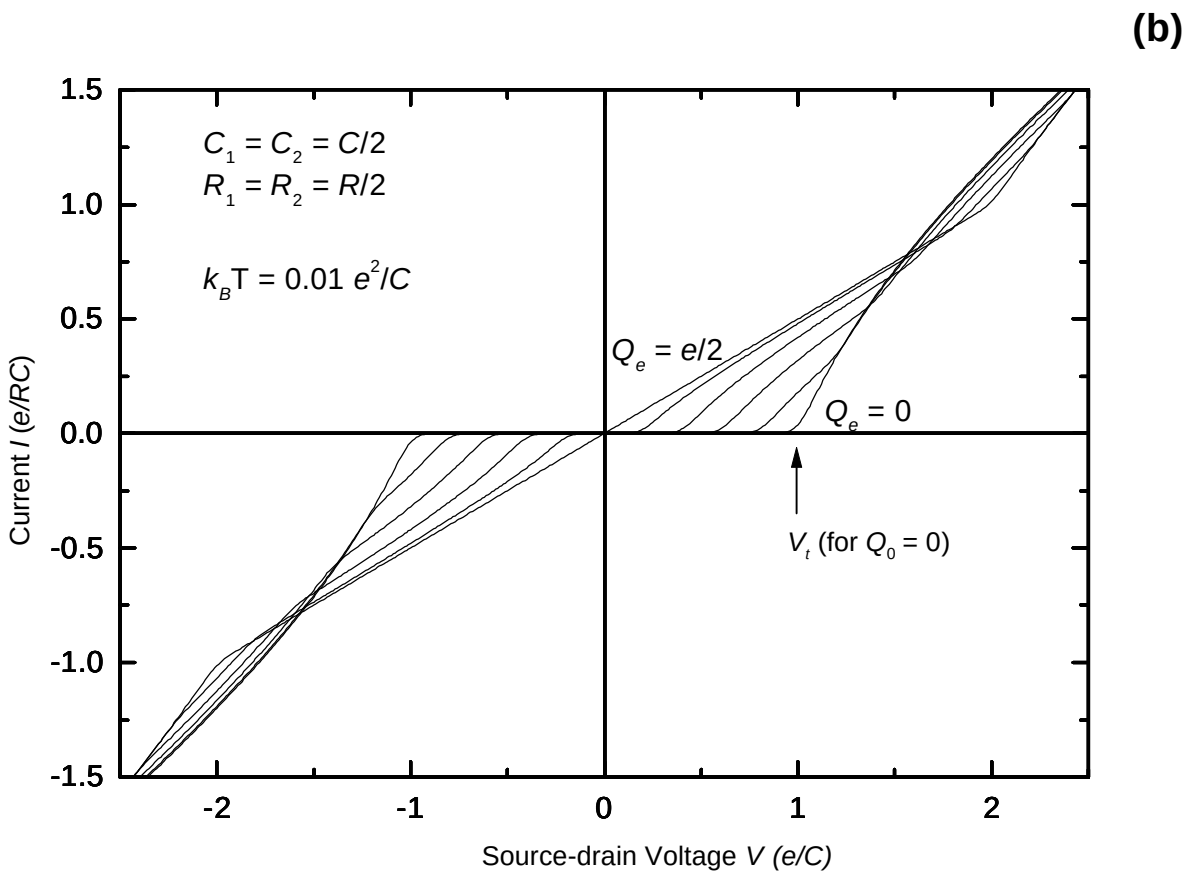
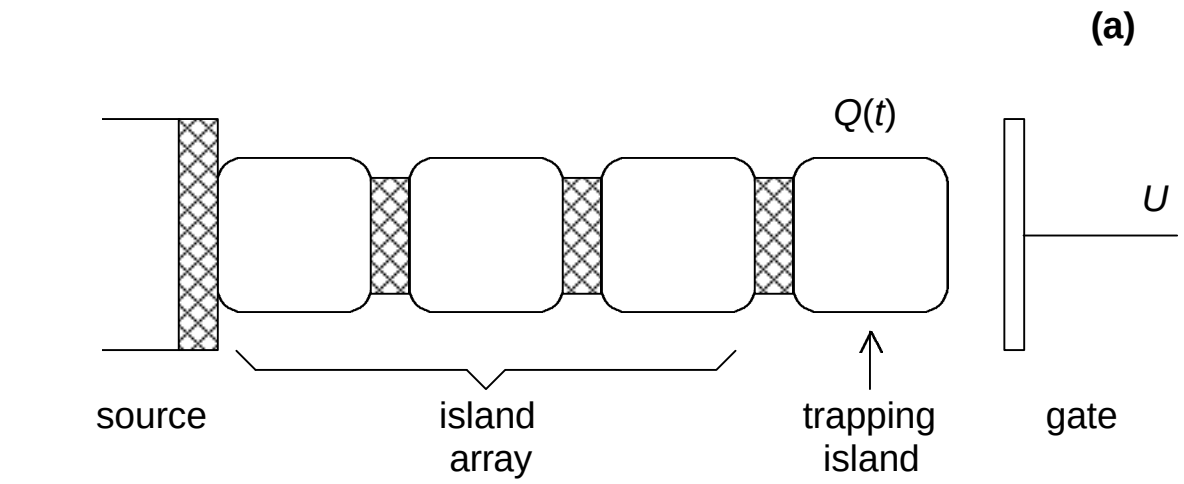
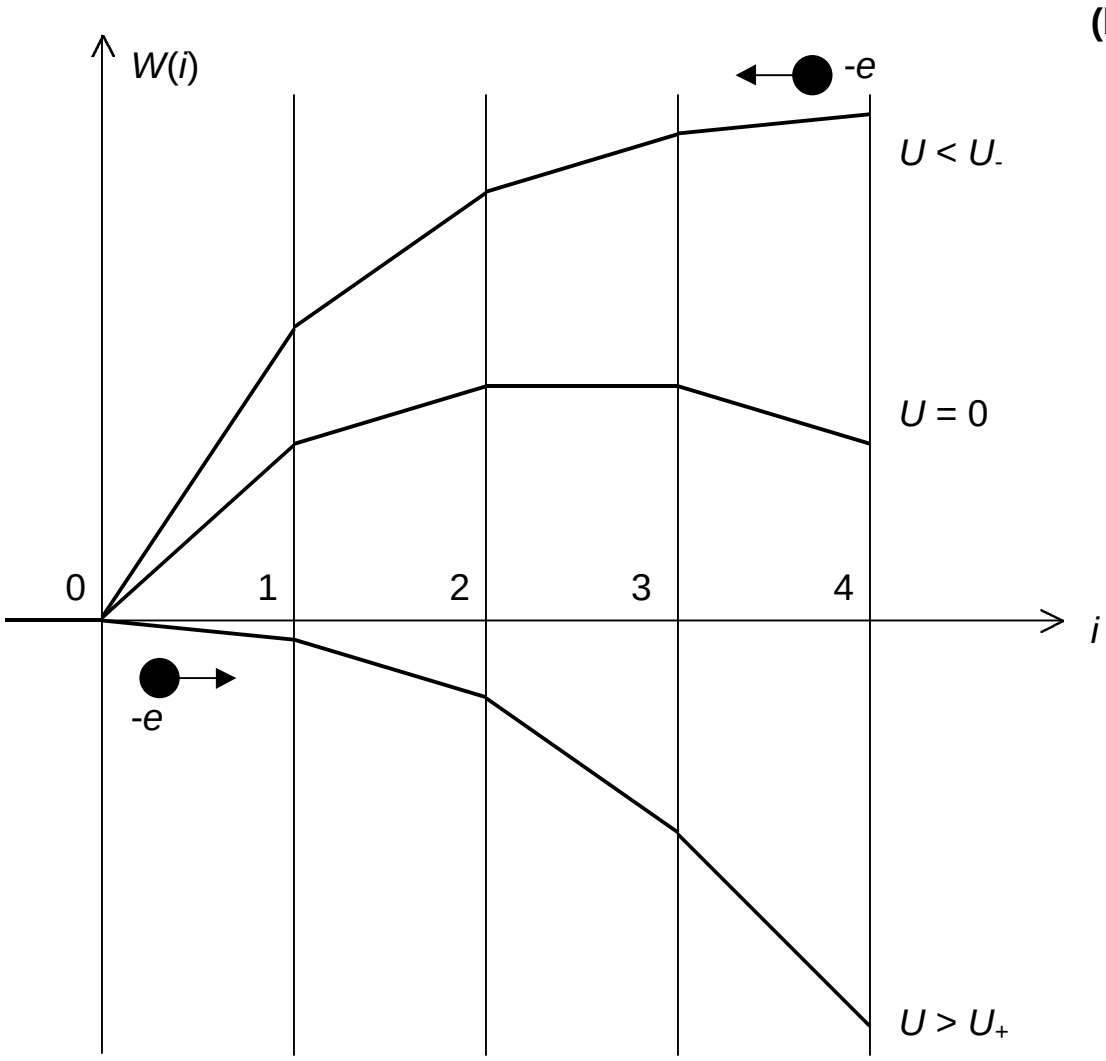


Fig. 6. Capacitively-coupled single-electron transistor: (a) schematics, (b) source-drain dc *I-V* curves of a symmetric transistor for several values of the Q_e, i.e. of the gate voltage, and (c) the Coulomb blockade threshold voltage V_t as a function of Q_e at $T \to 0$.


(a)
Q(t)
U
source
island
array
trapping
island
gate


(b)
W(i)
-e
U < U-
U = 0
0
1
2
3
4
i
-e
U > U+

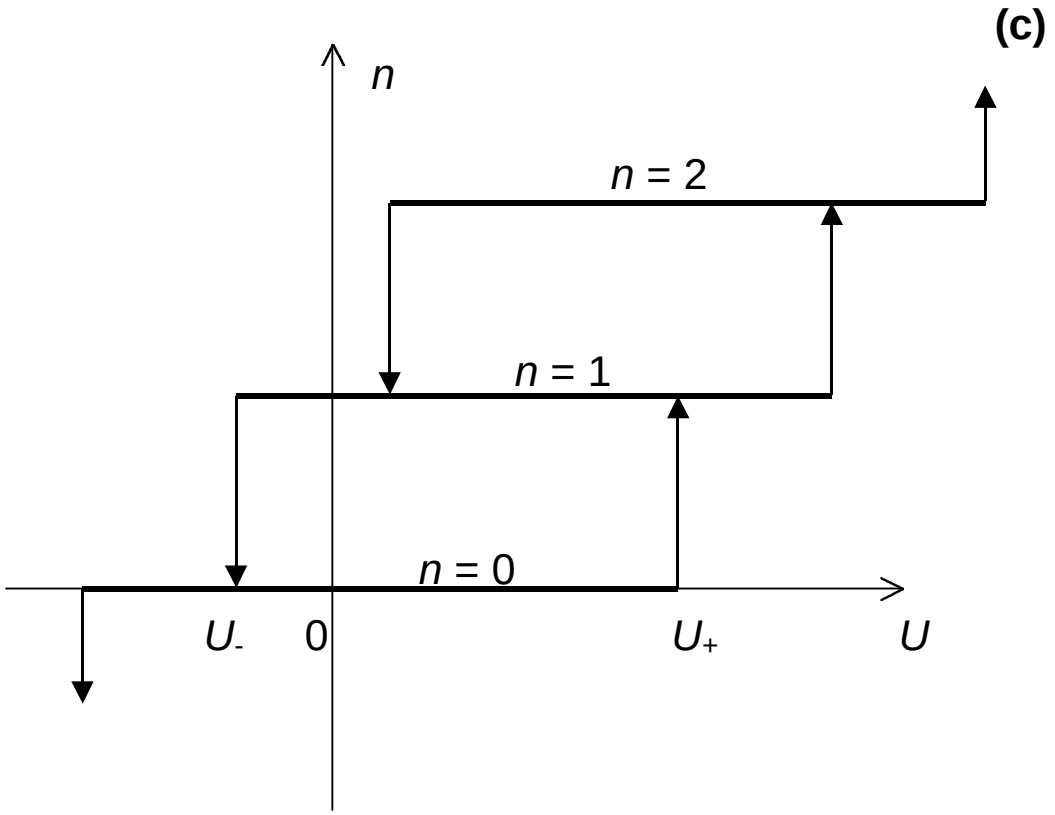


Fig. 7. Single-electron trap: (a) schematics, (b) electrostatic energy of an extra electron as a function of its position for three values of the gate voltage U, and (c) the static characteristic of the device (at $T \to 0$).

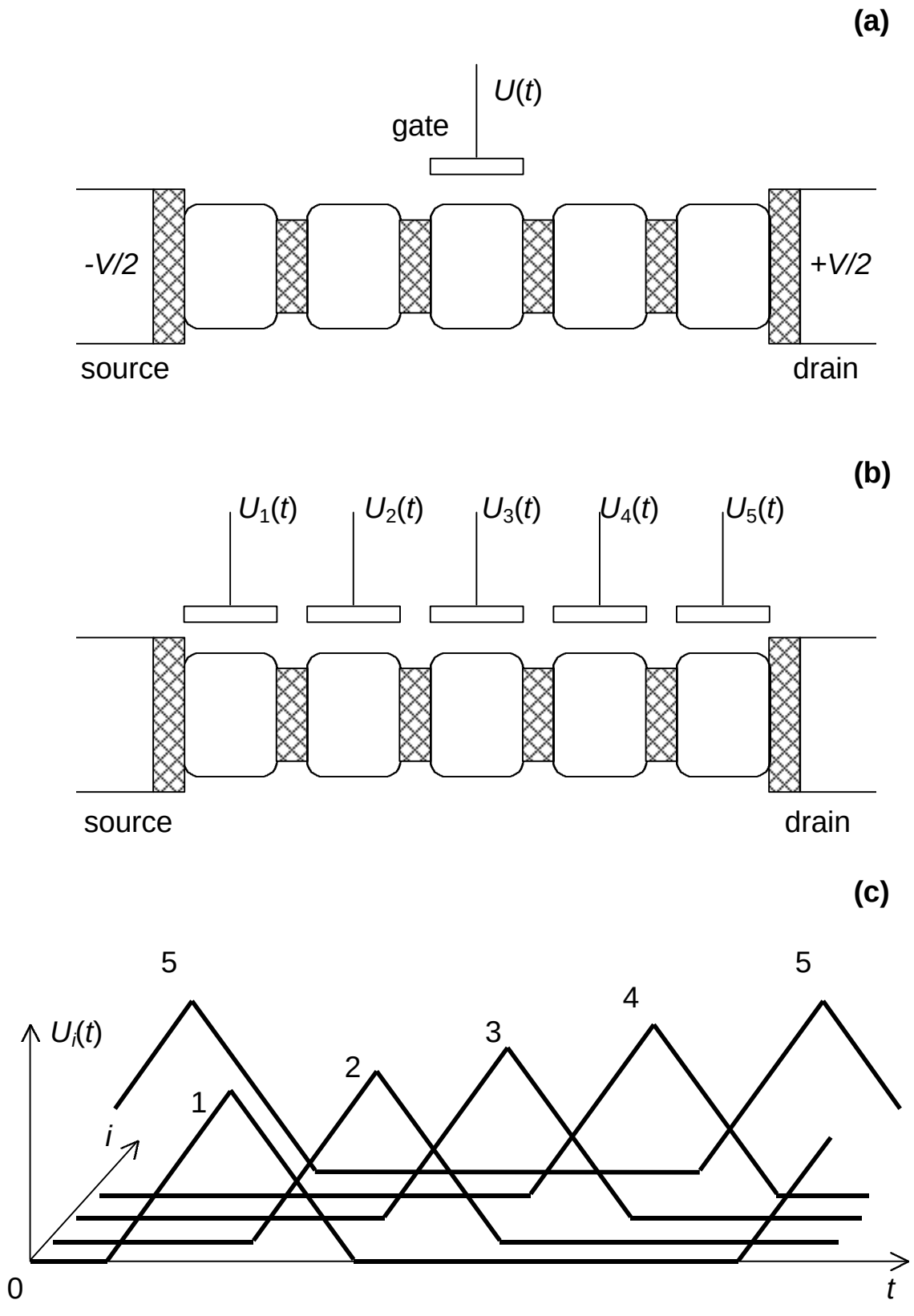


Fig. 8. Single-electron (a) turnstile and (b) pump; (c): a possible set of waveforms applied to the pump gates.

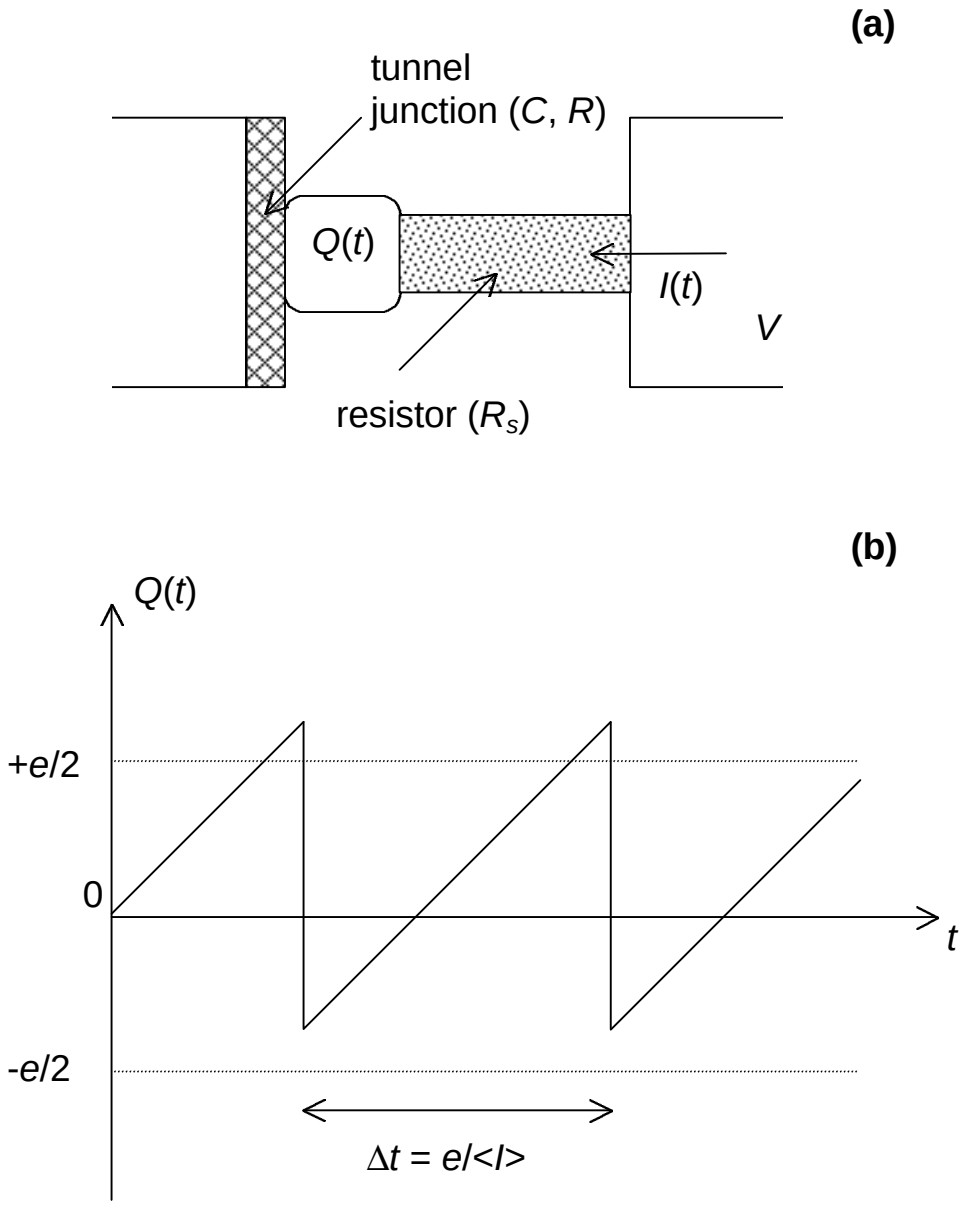


Fig. 9. The simplest single-electron oscillator: (a) schematics and (b) typical dynamics of the tunnel junction charge.

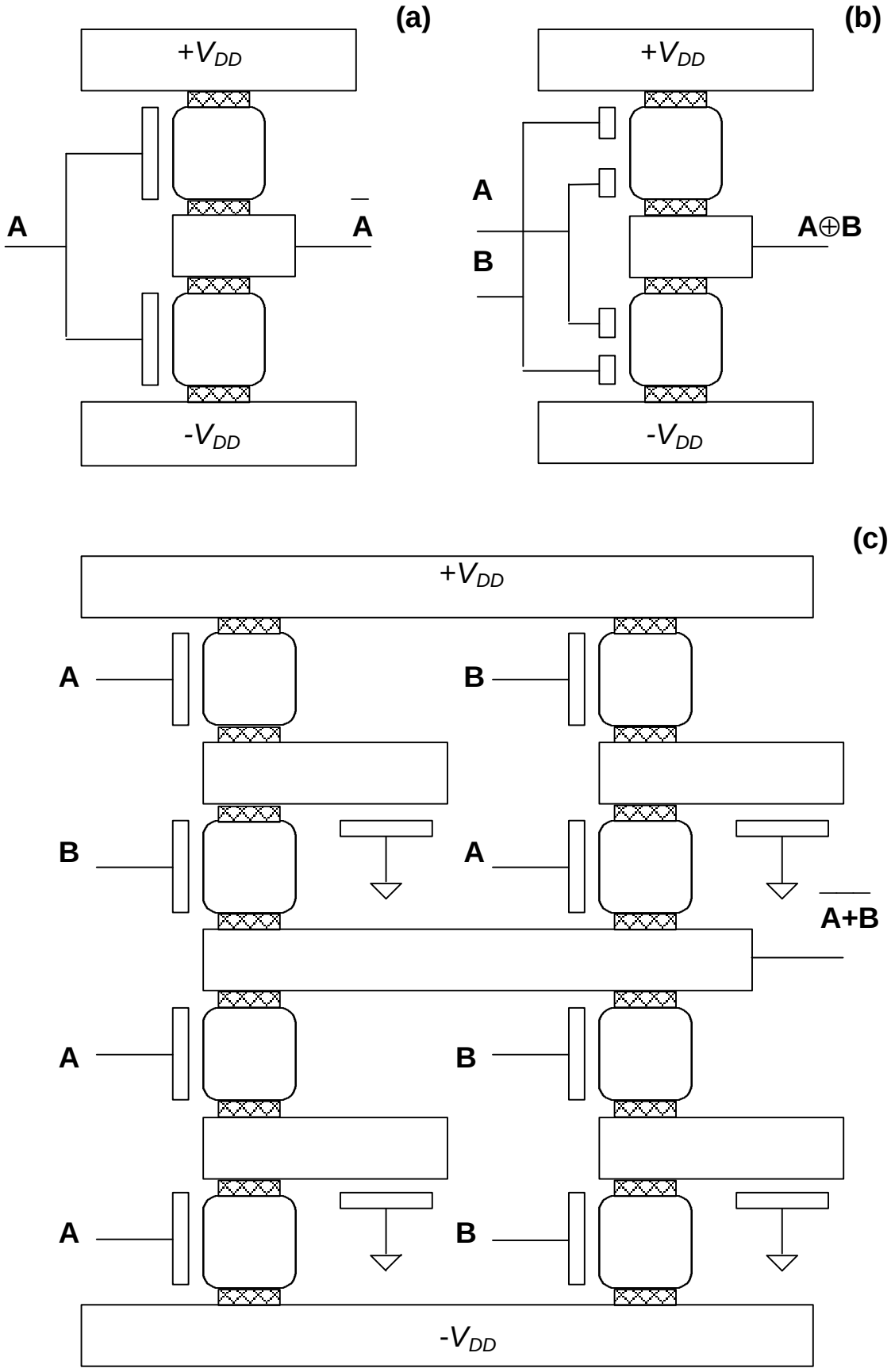
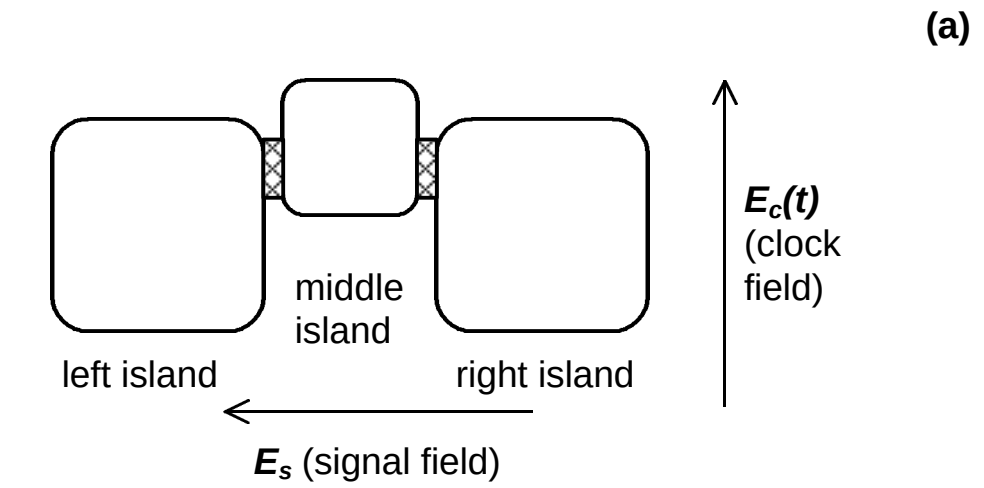
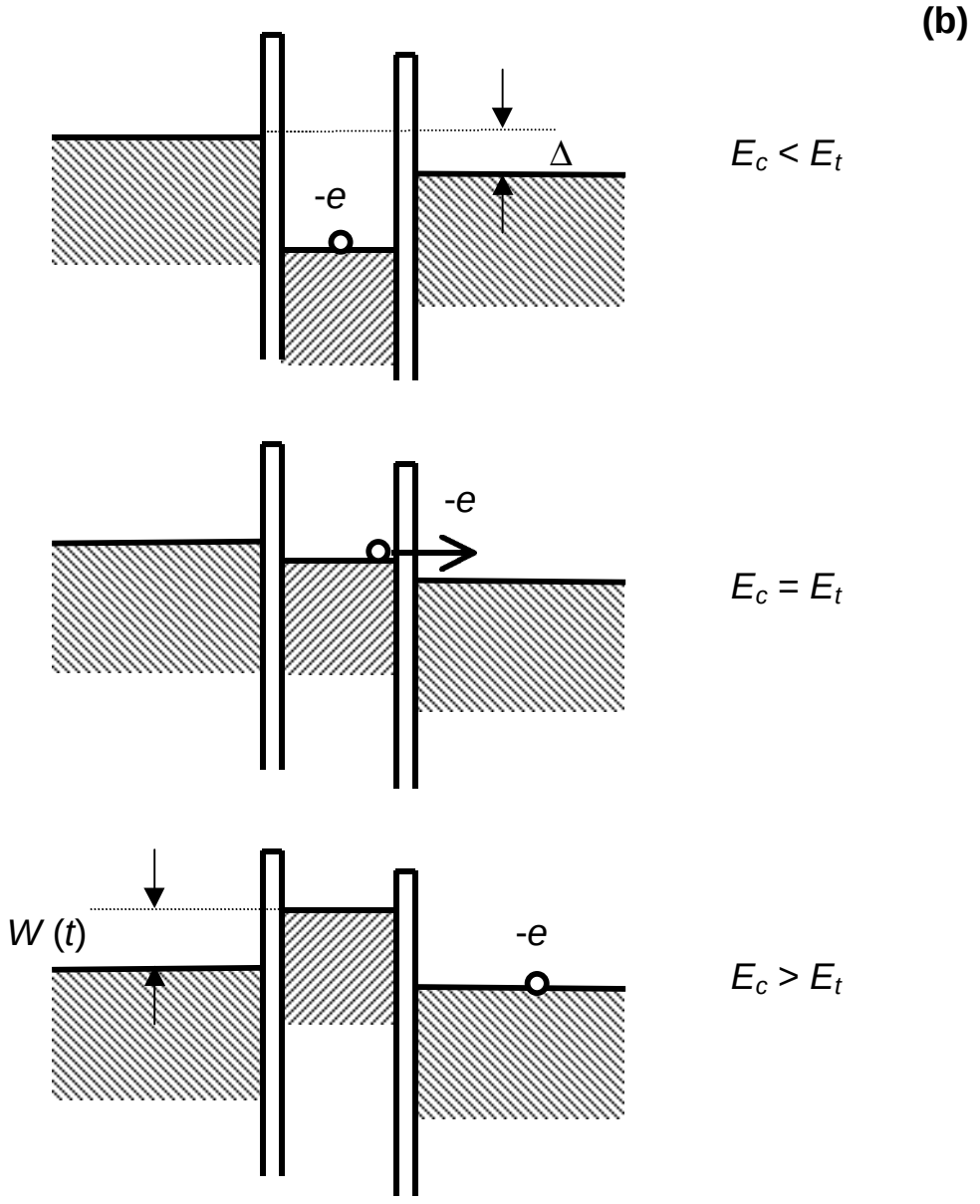


Fig. 10. A set of logic gates of the complementary voltage-state family using capacitively-coupled single-electron transistors: (a) inverter; (b) XOR, and (c) NOR/NAND. (After Ref. 130).


(a)
middle
island
left island
right island
$E_c(t)$
(clock
field)
E_s (signal field)


(b)
Δ
-e
$E_c < E_t$
-e
$E_c = E_t$
W (t)
-e
$E_c > E_t$

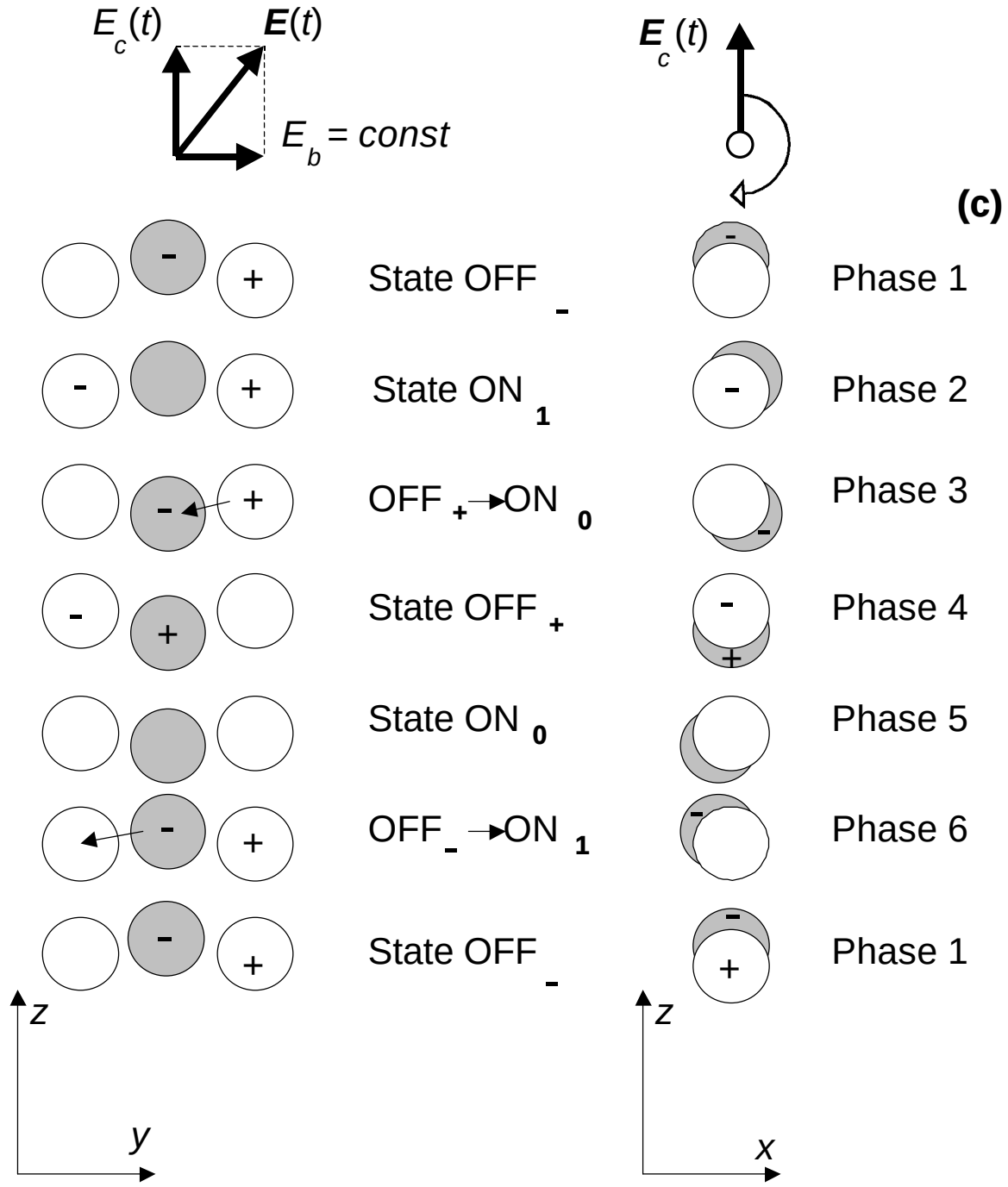


Fig. 11. SET Parametron: (a) schematics and (b) energy diagram at 3 values of the clock field $\boldsymbol{E}_c(t)$. Energy difference Δ between the edge islands is proportional to the signal field $\boldsymbol{E}_s$, while the energy shift $W(t)$ of the middle island is determined by the clock field. (c) Shift register using a variety of SET Parametron cells ("single-exciton parametrons") which do not require the initial charging. (After Ref. 142).

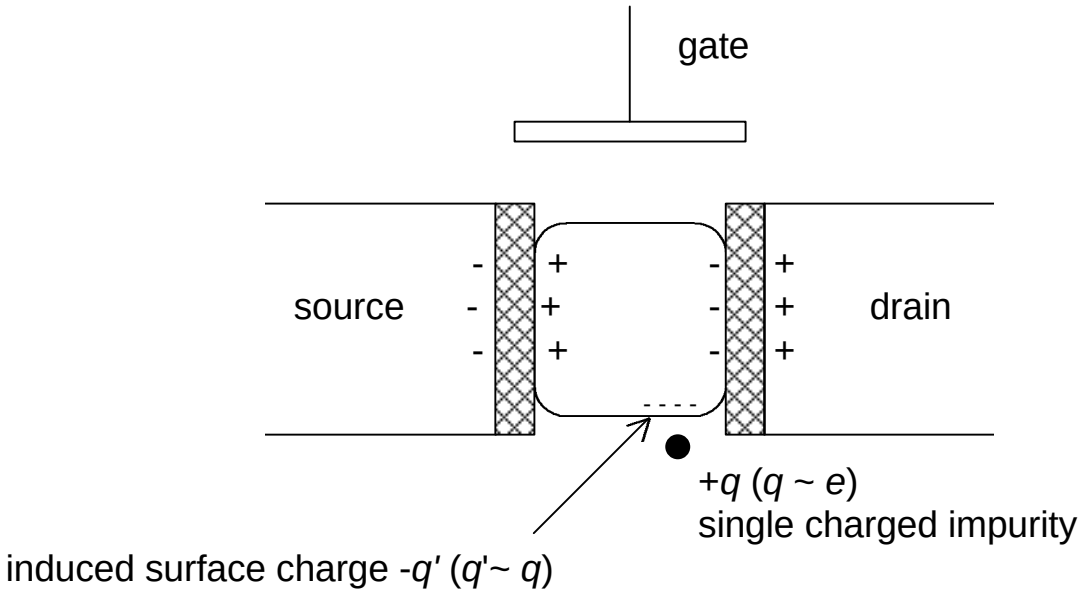


Fig. 12. The effect of a single charged impurity on the single-electron transistor.

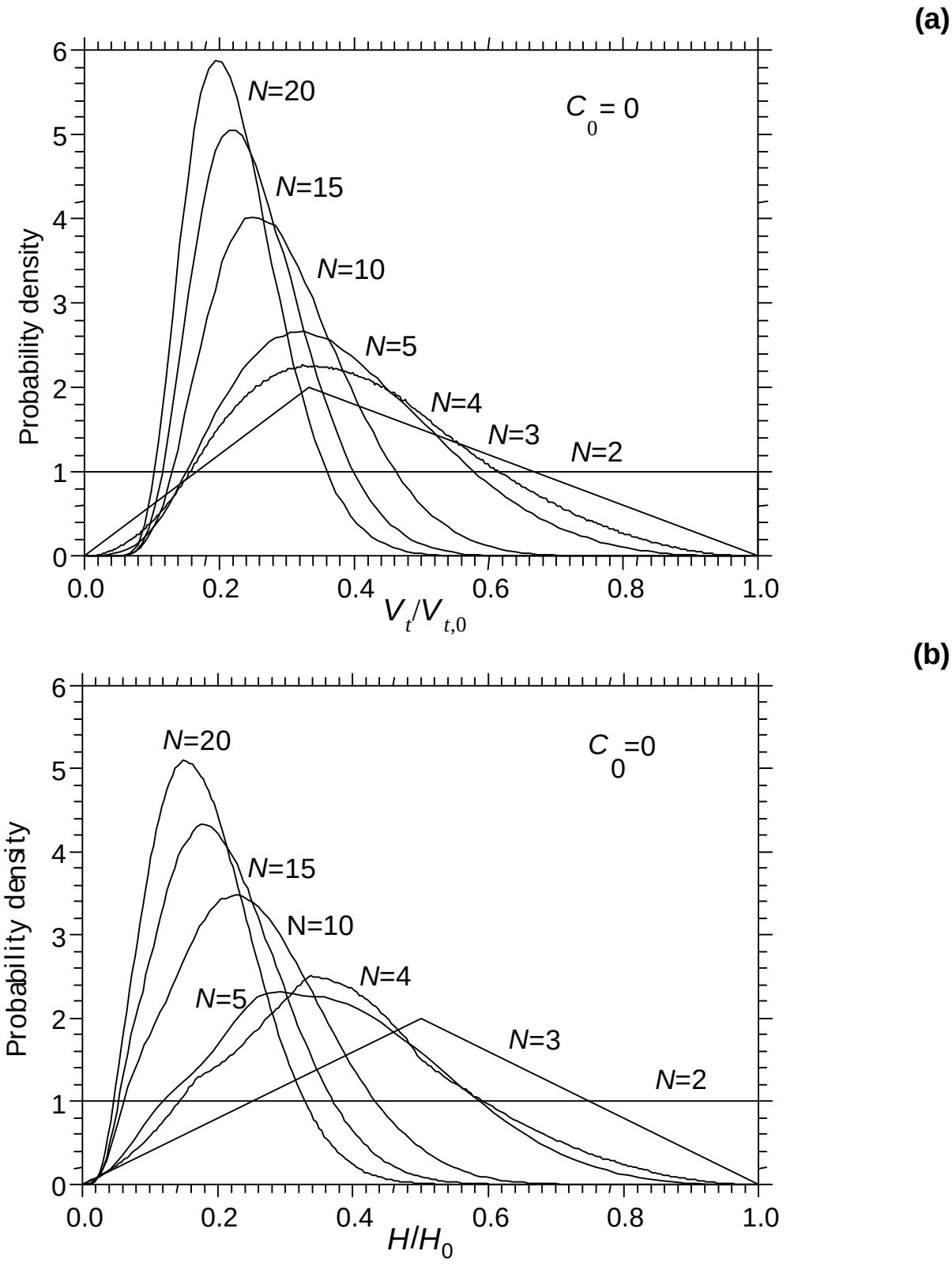


Fig. 13. Histograms of (a) Coulomb blockade threshold voltage V_t, and (b) energy barrier height H for statistical ensembles of 1D single-electron arrays with N tunnel barriers and random background charges of islands. Index 0 corresponds to the values of V_t and H in the absence of background charges. All the junction capacitances C are assumed equal, stray capacitances negligibly small. Figure courtesy of Dr. A. Korotkov (unpublished).

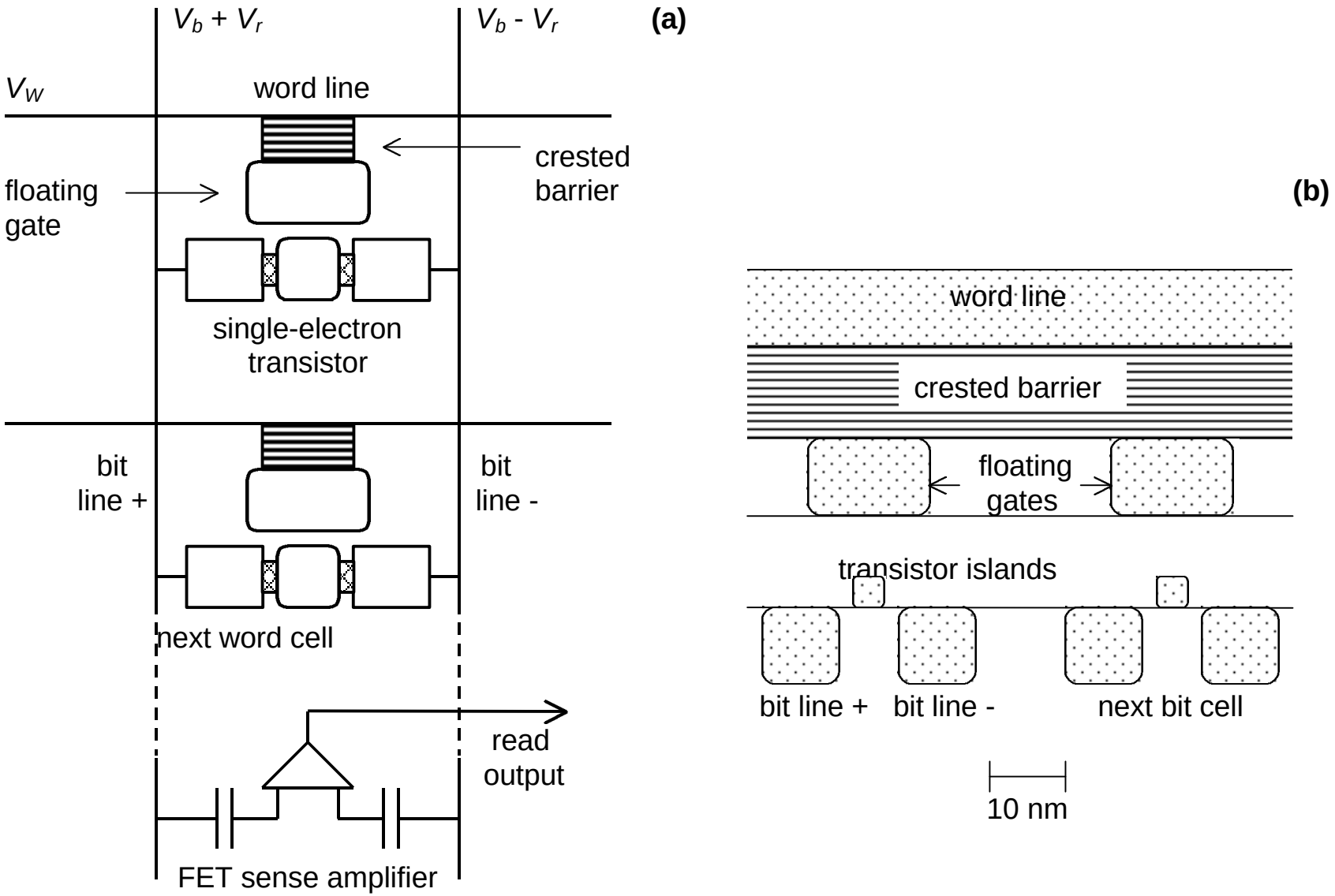


Fig. 14. Hybrid SET/FET memory insensitive to the background charge randomness: (a) schematics, and (b) side view on a possible layout compatible with room-temperature operation and a density of 100 Gbits/cm^2. (After Ref. 164.)

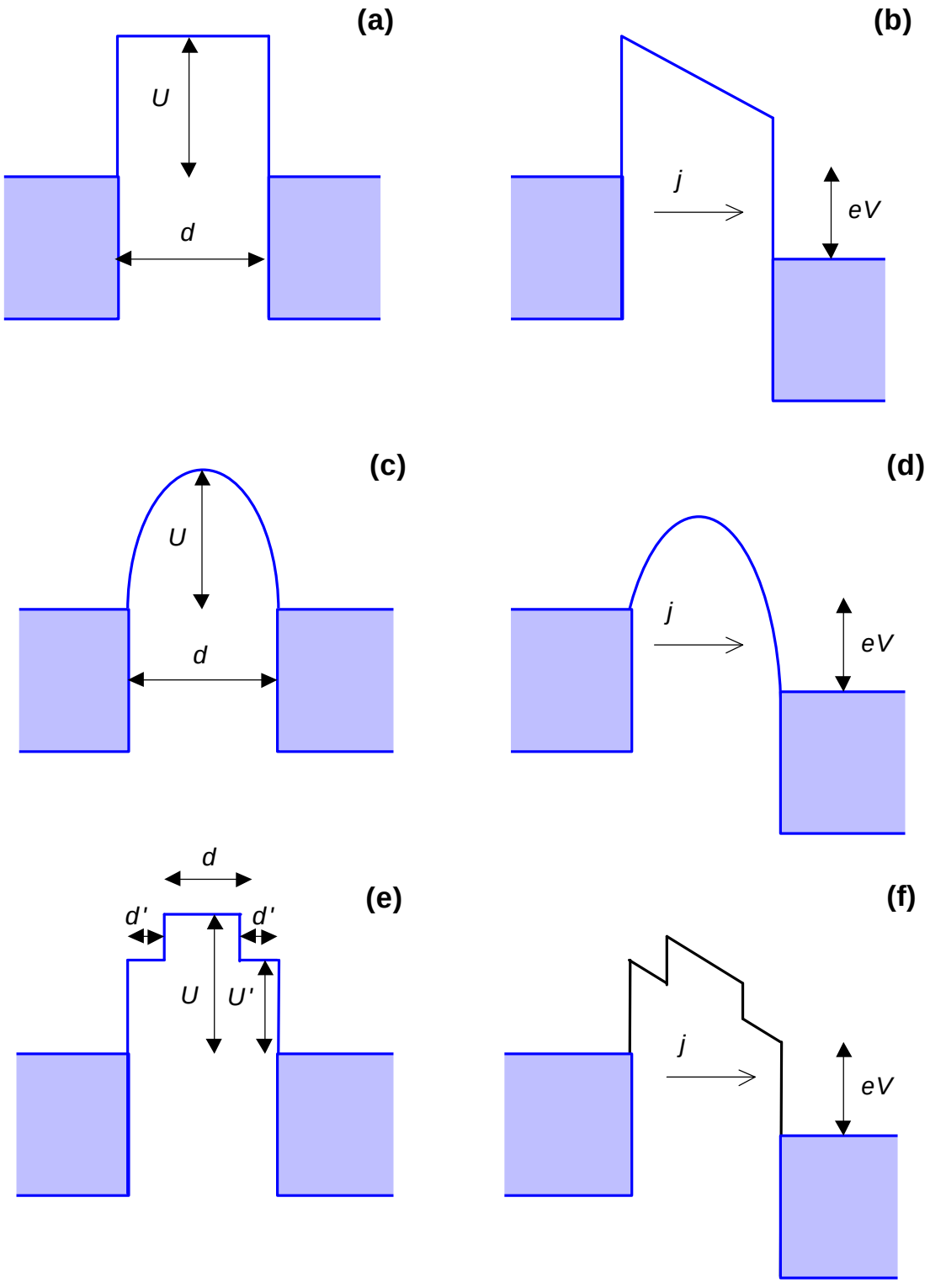


Fig. 15. Various tunnel barriers without (left column) and with (right column) applied electric field: (a, b) Usual uniform barrier (often called "rectangular" or "trapezoidal"). (c, d) Crested barrier with parabolic profile. (e, f) Trilayer crested barrier. (After Ref. 167.)

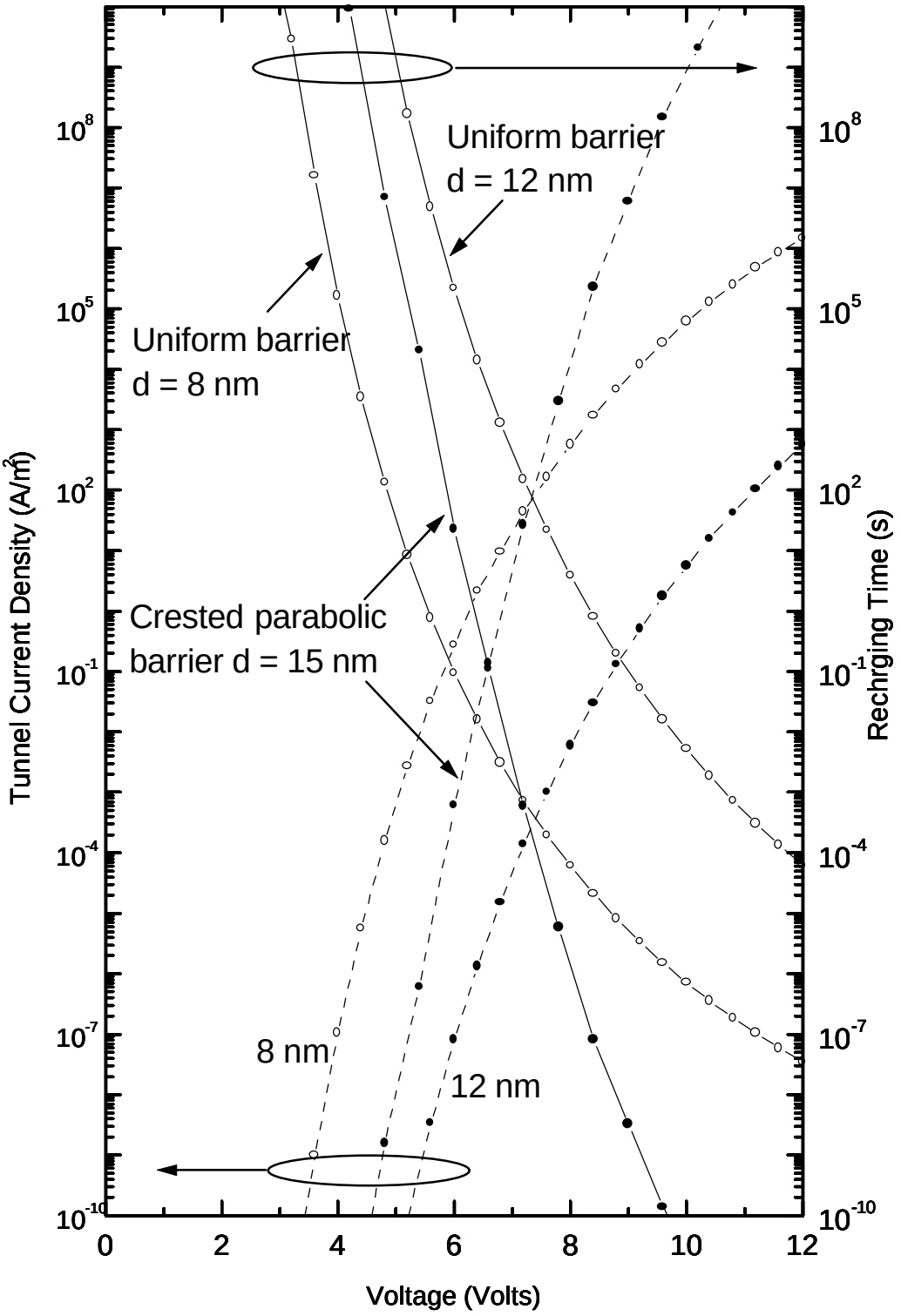
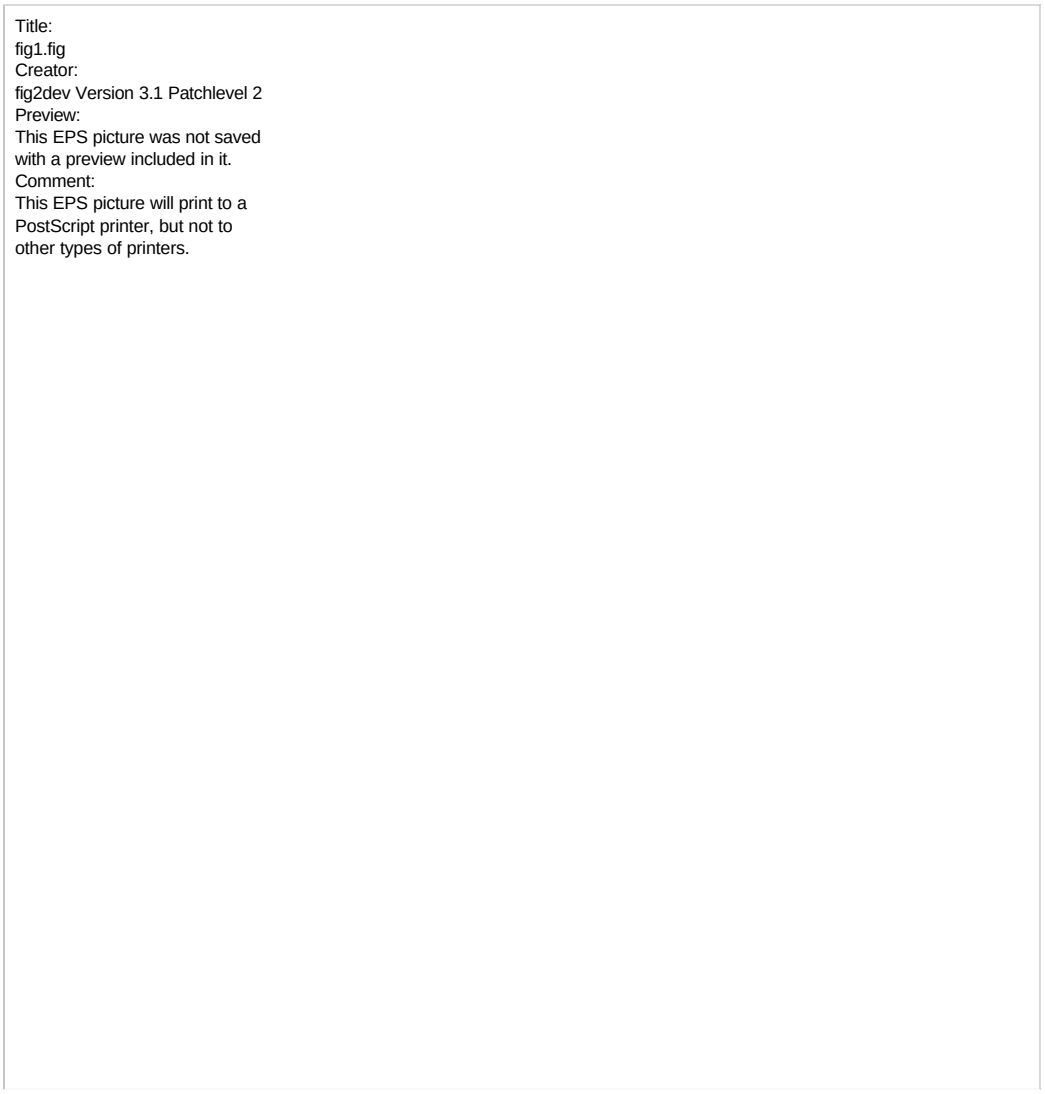


Fig. 16. Tunnel current (solid lines) and floating gate recharging time scale (dashed lines) for usual rectangular barriers with two values of thickness d (open points), and for a crested parabolic barrier shown in Fig. 15c,d (solid points). In all cases the maximum height of the barrier U = 3.2 V, and the electron effective mass under the barrier is $m = 0.3m_0$ (the parameters correspond to a SiO_2 barrier between n^+-doped silicon electrodes. (After Ref. 167.)

(a)



(b)

Fig. 17. Dual-gate *n*-MOSFET with ballistic transfer of electrons along an undoped channel: (a) a simple geometric model, (b) conduction band edge diagram (schematically), and (c) subthreshold characteristics as calculated using a simple semi-analytical model [170]. Contact doping 3×10^{20} cm^{-3}, other parameters: $2s$ = 1.5 nm, d - s = 2.5 nm; source drain voltage is close to 0.5 V. Fine hatching shows the parameter window where the gate leakage exceeds the source current, while coarse hatching shows the window where the holes cannot be ignored (in both regions, large deviations from the calculation results are expected).

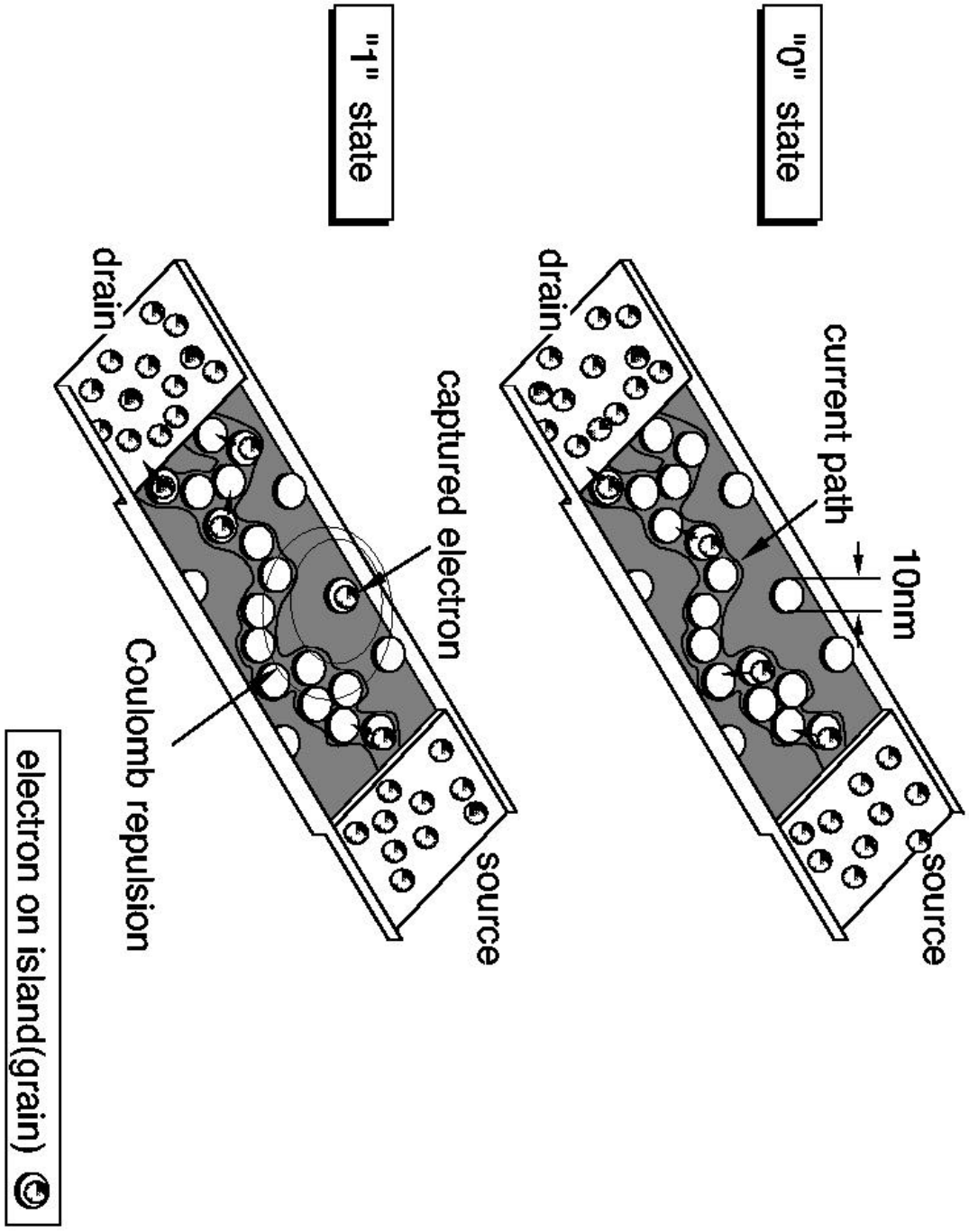


Fig. 18. A cartoon showing the operation principle of Hitachi's memory cell. A single electron captured in a silicon grain may block transfer of electrons along a percolation current path. (Courtesy of Dr. T. Ishii).

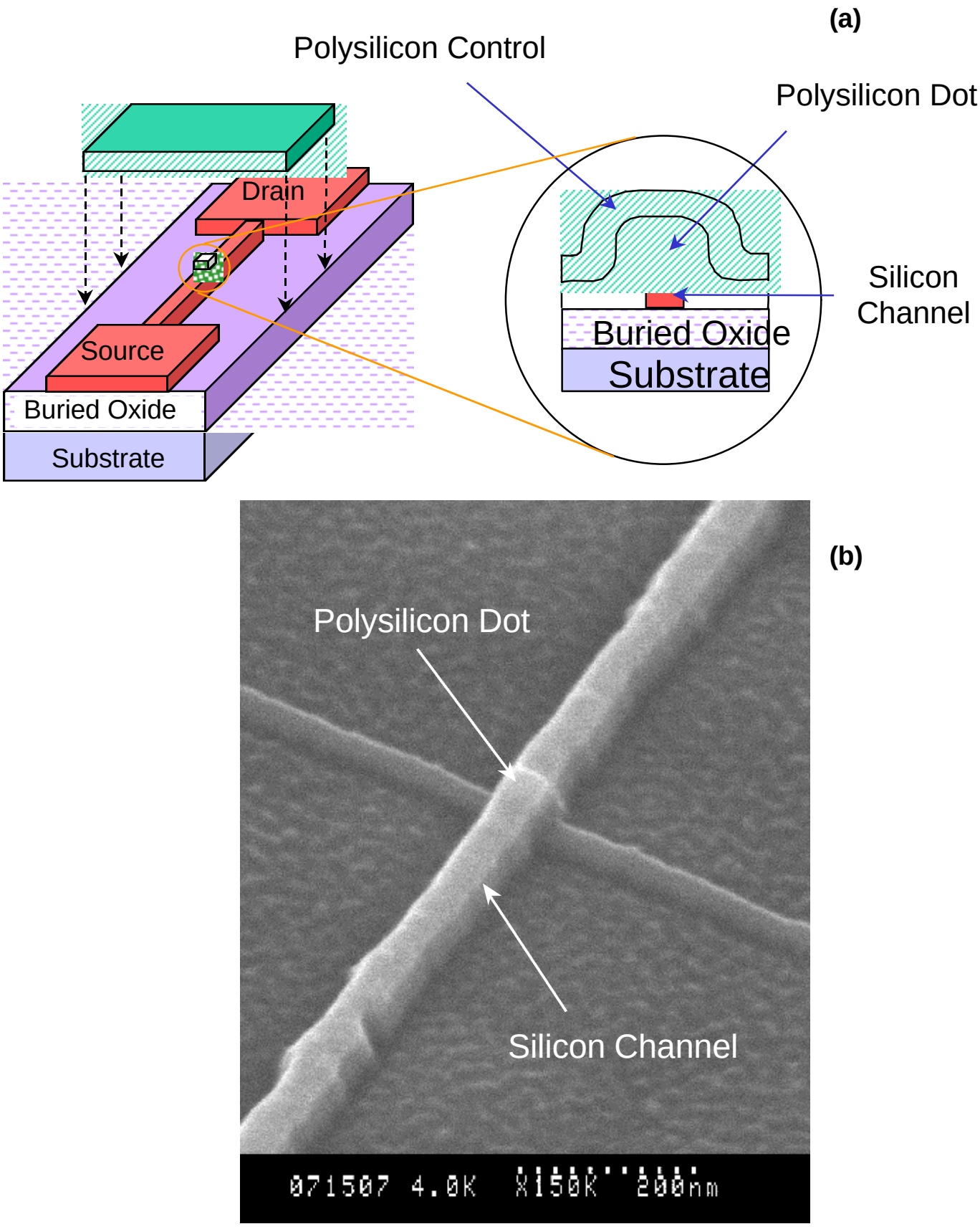


Fig. 19. Floating gate memory cell developed at the University of Minnesota: (a) schematics and (b) SEM picture taken before the control gate deposition. (After Ref. 175.)

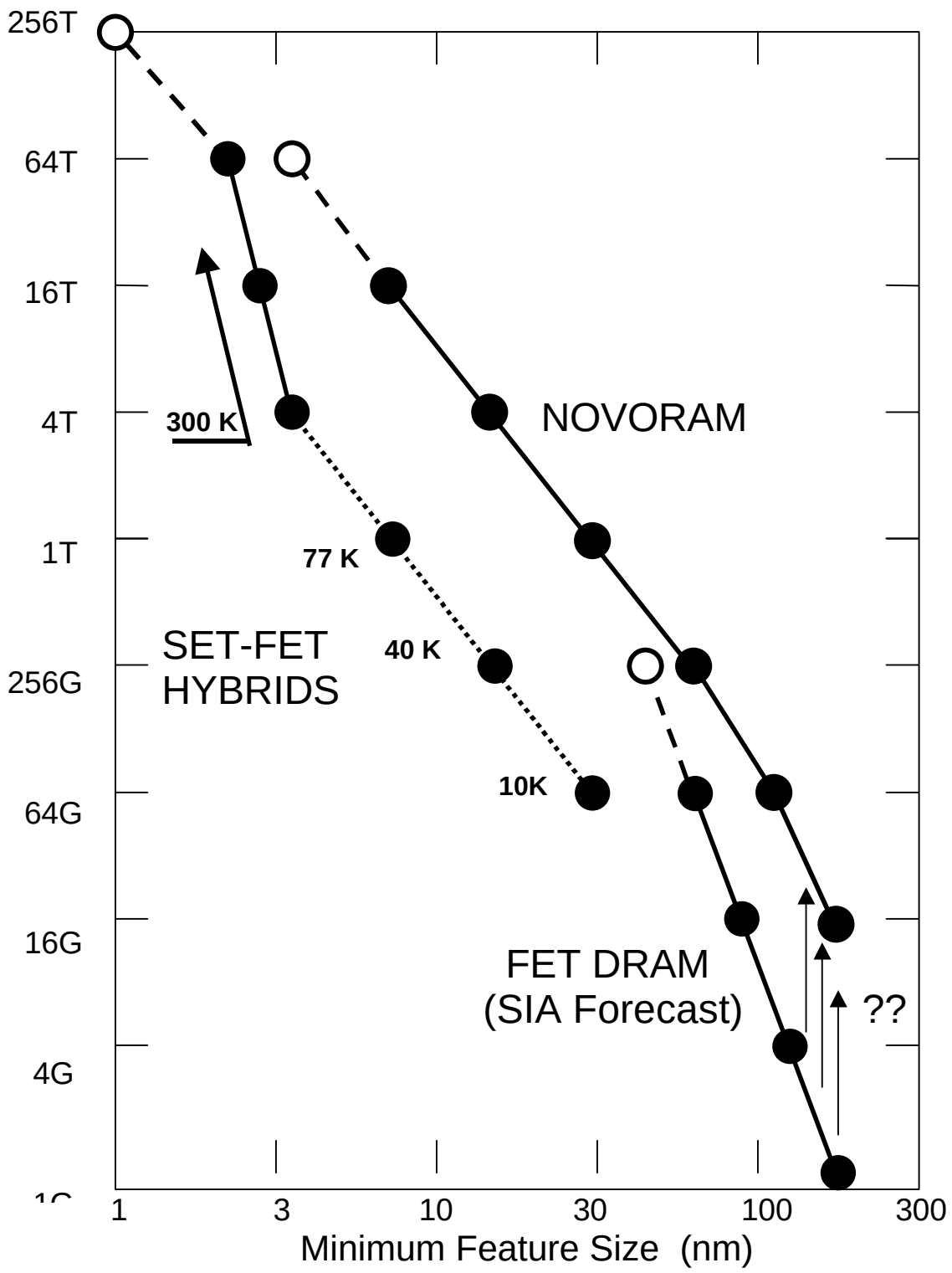


Fig. 20. Scaling prospects for various bit-addressable memories. Solid lines show the estimated relation between the minimum feature size and integration scale. The bit density is recalculated to the integration scale using the log-linear extrapolation of the chip size growth, similar to that accepted in the SIA forecast [177]. The DRAM projections (the lower right line) are also borrowed from that forecast. Dashed lines shows the regions where I anticipate major problems to occur (on the top of fabrication challenges). Dotted line shows the range where the operation of the SET/FET hybrid memory is possible at low temperatures (indicated with numbers at the dots).

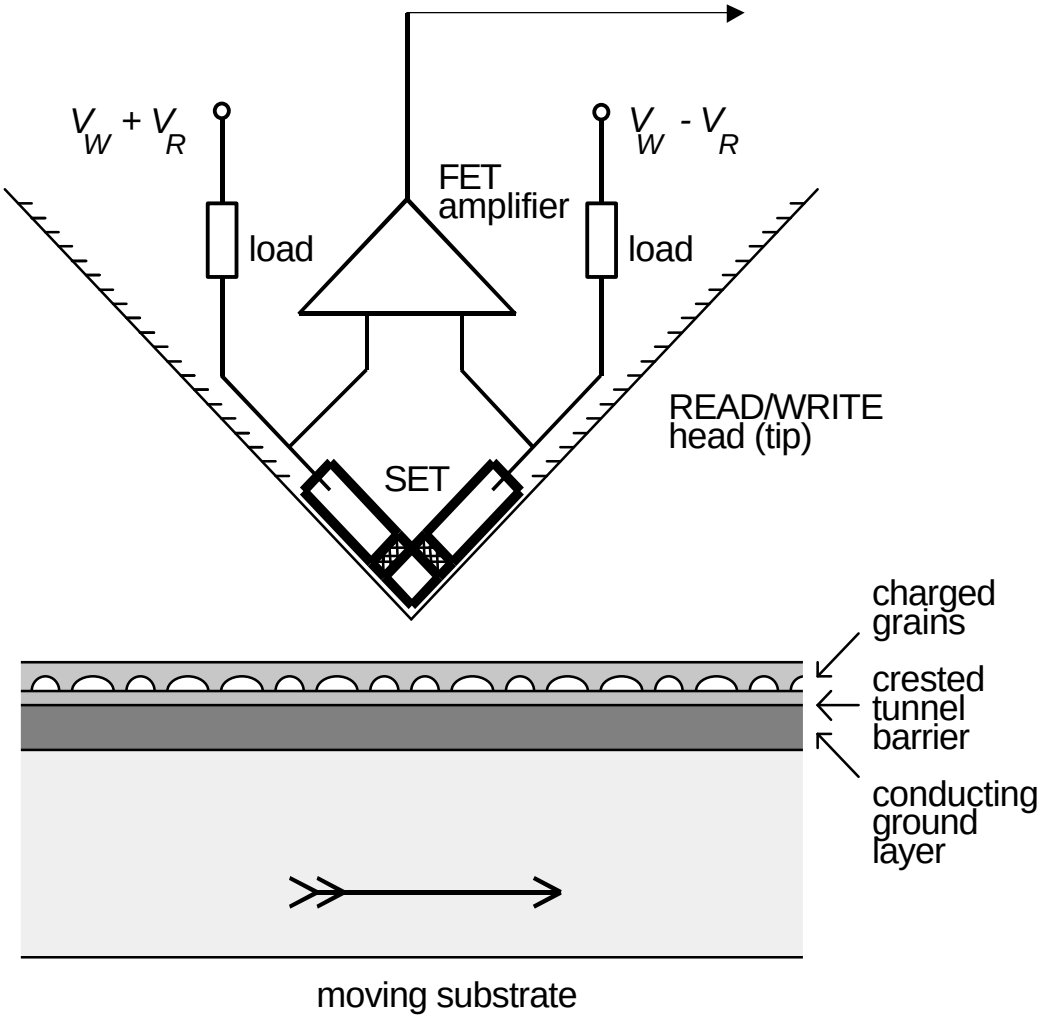


Fig. 21. Proposed electrostatic data storage system with hybrid SET/FET readout. (After Ref. 178.)