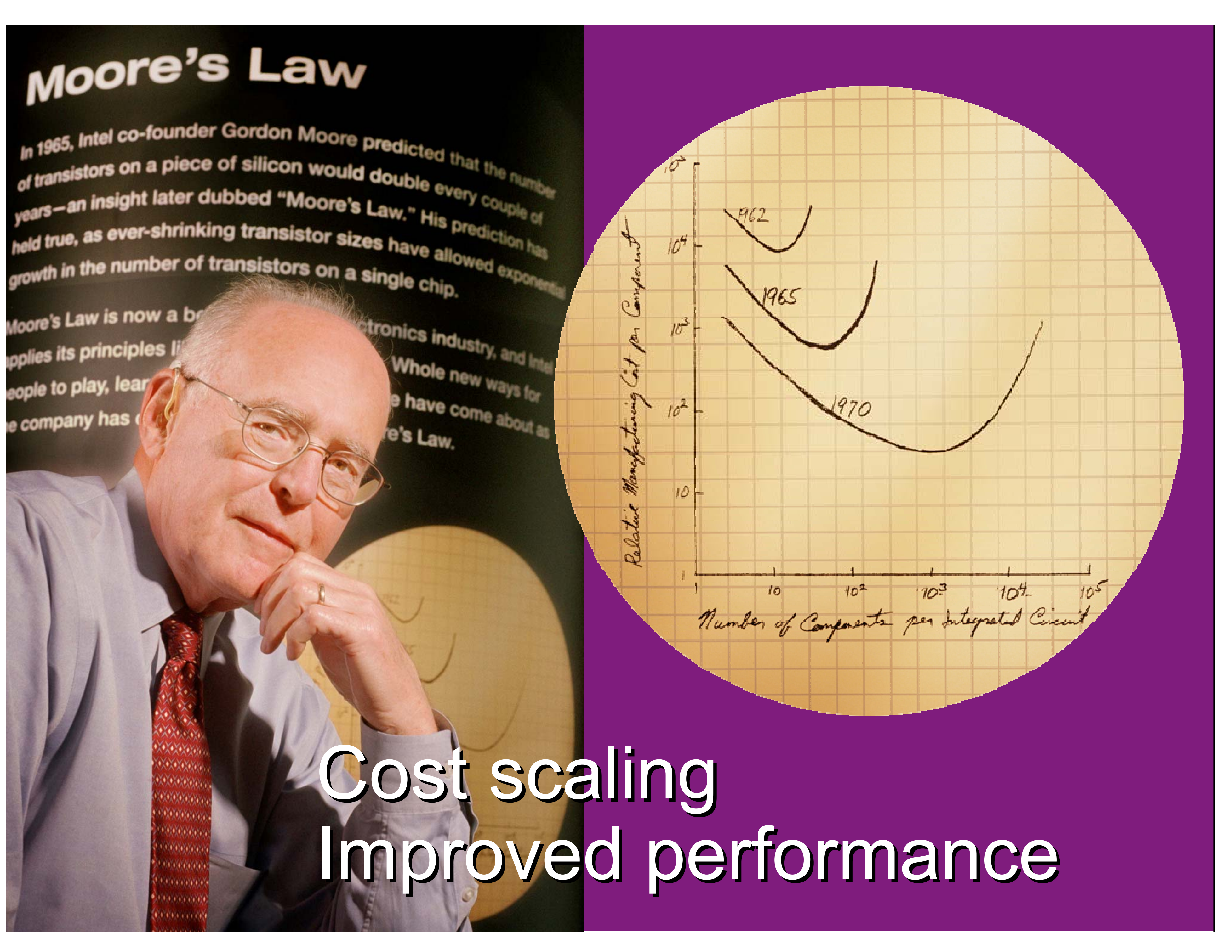
MARC HEYNS

IMEC
Kapeldreef 75, B-3001 Leuven, Belgium
also at MTM, KULeuven, Belgium

Innovation in nanoelectronics
for a sustainable future


Moore's Law
In 1965, Intel co-founder Gordon Moore predicted that the number
of transistors on a piece of silicon would double every couple of
years—an insight later dubbed "Moore's Law." His prediction has
held true, as ever-shrinking transistor sizes have allowed exponential
growth in the number of transistors on a single chip.
Relative Manufacturing Cost per Component
Number of Components per Integrated Circuit
1962
1965
1970
Cost scaling
Improved performance

Nanoscale dimensions by lithography

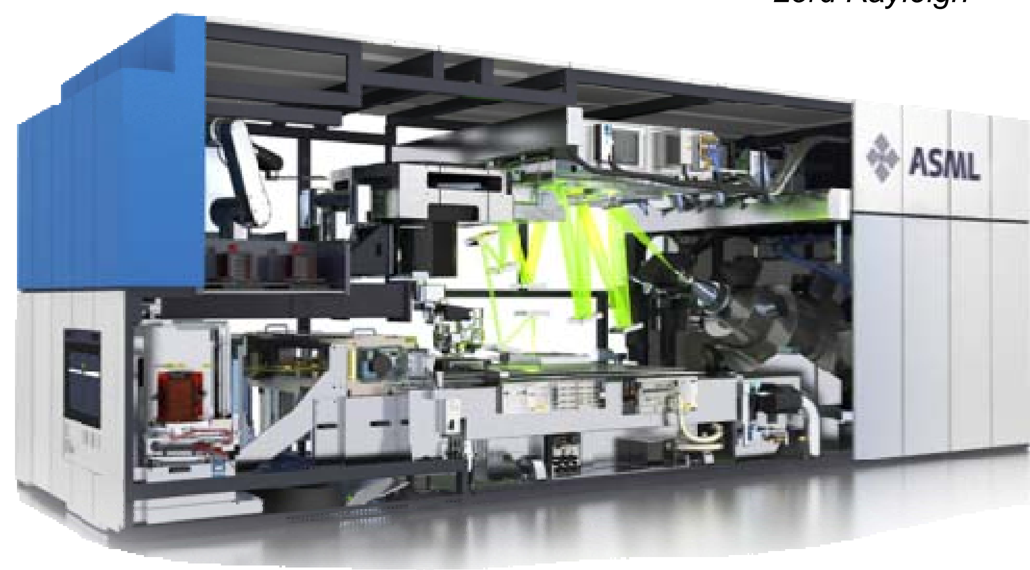
Exposure wavelength (λ)

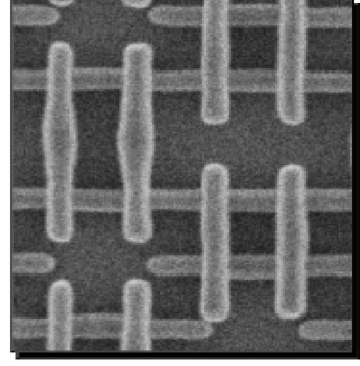
436nm : g-line
365nm : i-line
248nm : Deep-UV (KrF)
193nm : Deep-UV (ArF)
157nm : Vacuum UV (F2)
13.5nm: Extreme UV (EUV)

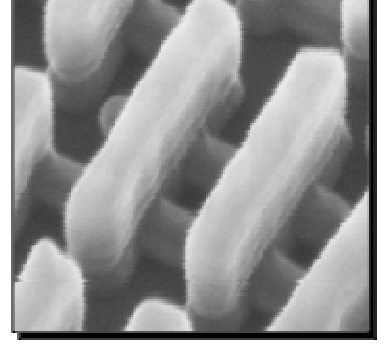
Lord Rayleigh

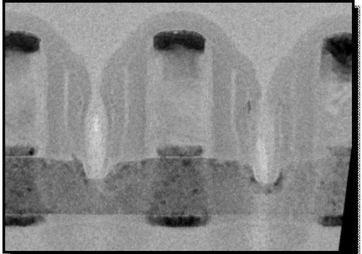
Rayleigh equation defines litho roadmap

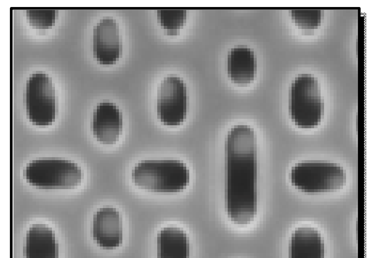
$$resolution = k_1 . \frac{\lambda}{NA}$$







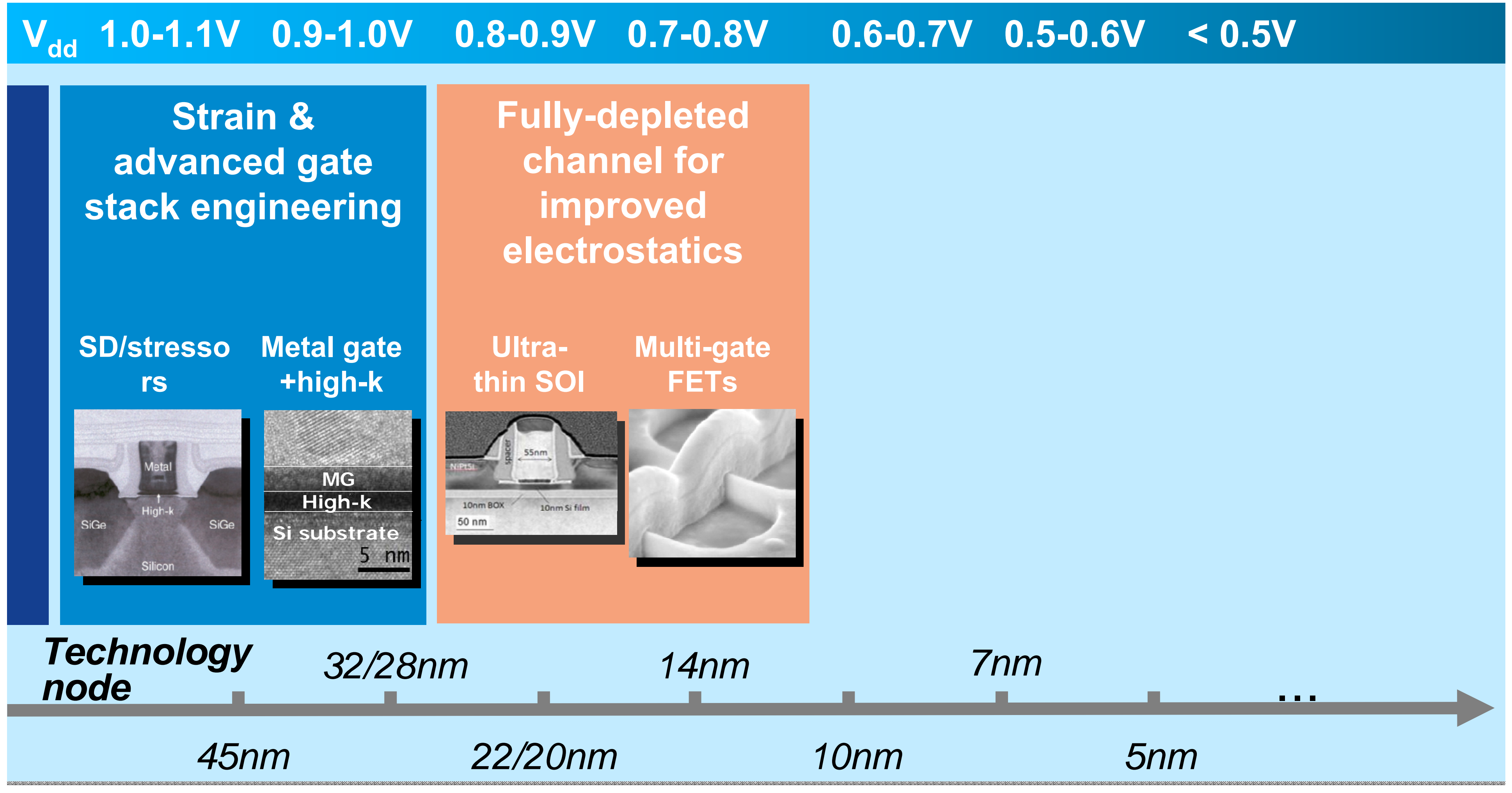




22-16nm SRAM fabricated with EUV

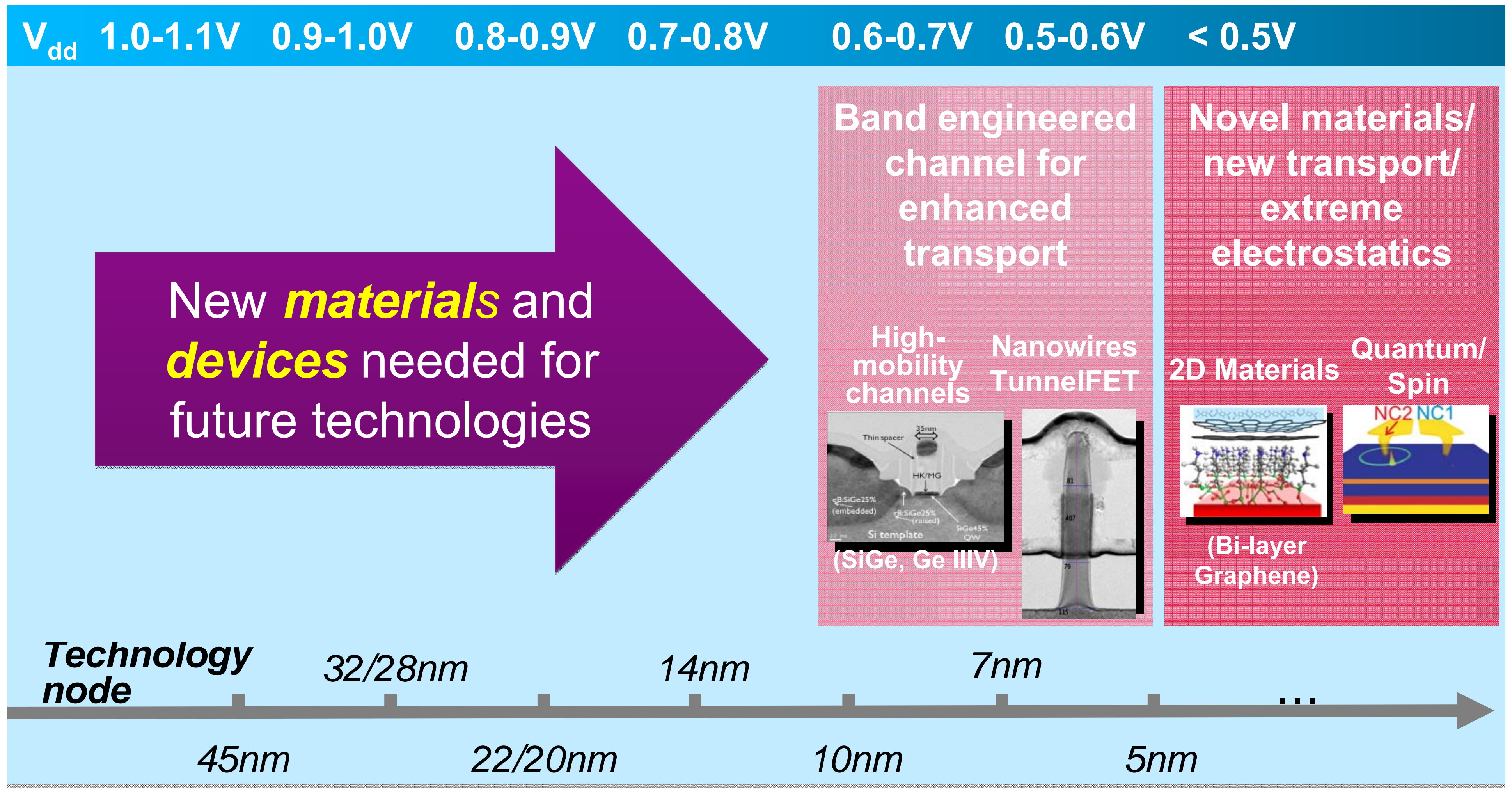
© IMEC 2013

Logic scaling trend and roadmap



➢ Feature dimension & voltage scaling are concurrent drivers

Logic scaling trend and roadmap

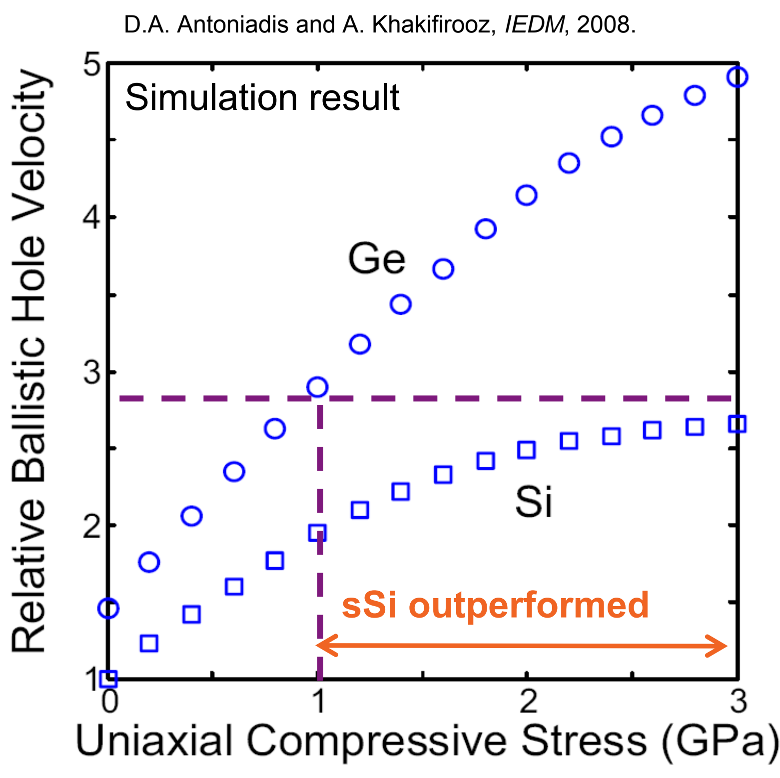


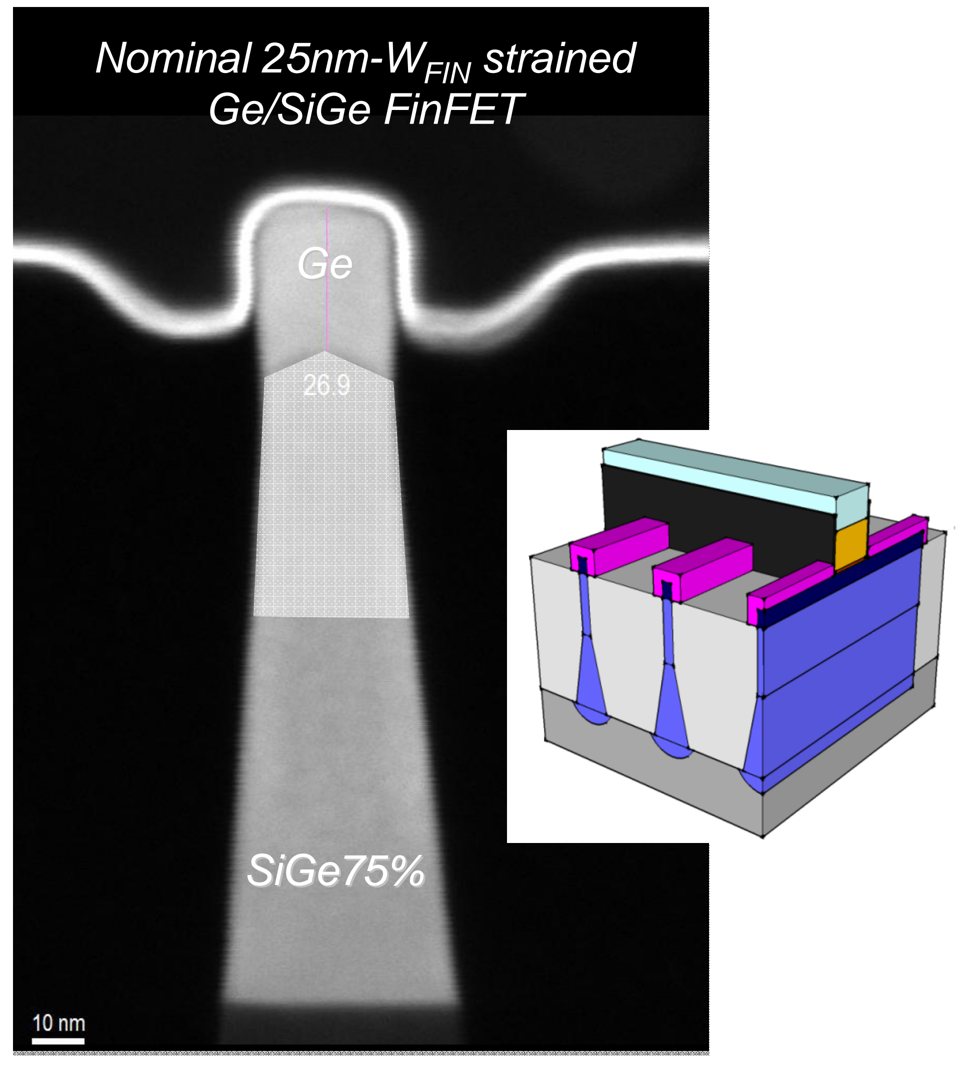
- Feature dimension & voltage scaling are concurrent drivers
- Material & device architecture innovations enablers of continual scaling

© IMEC 2013

Strained Ge pMOS devices

➢ Compressively strained Ge can outperform sSi pMOS



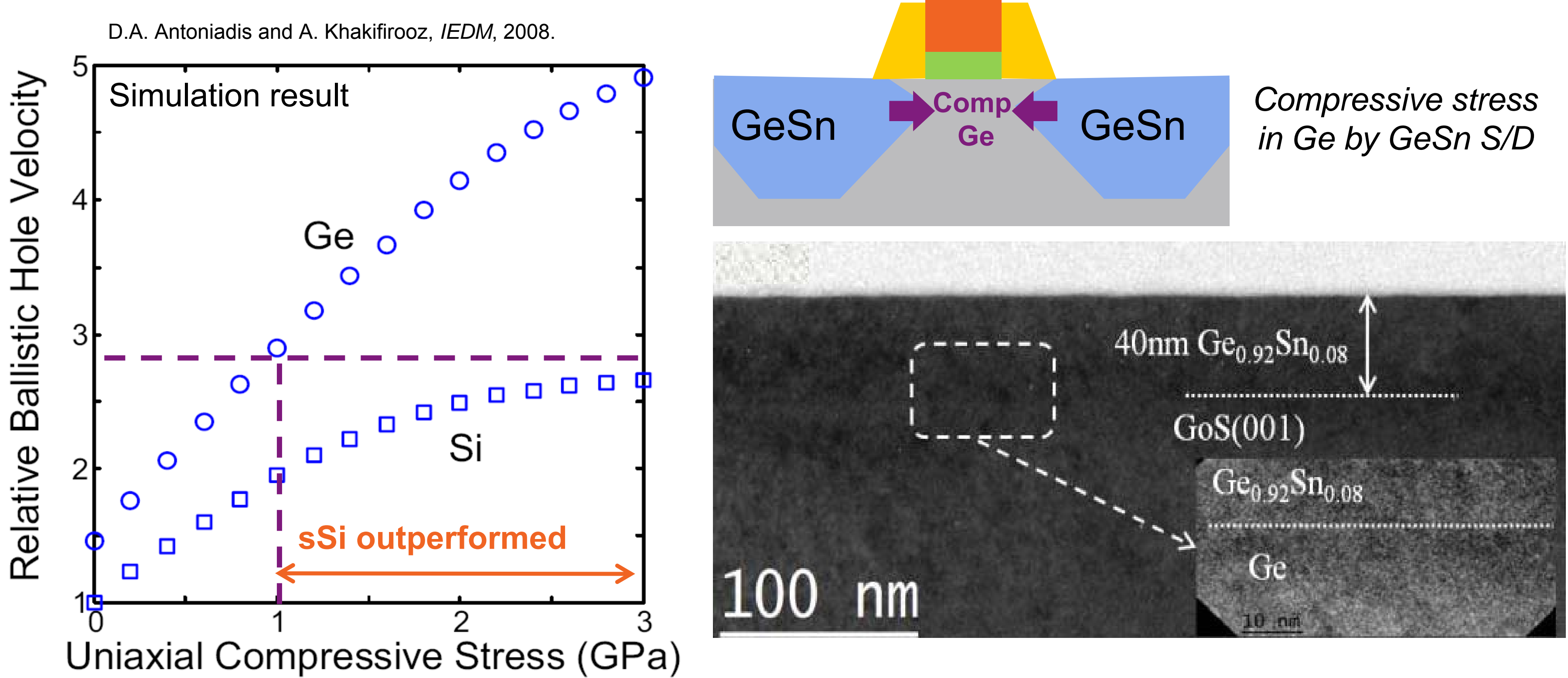


- Demonstration of strained Ge/SiGe FinFETs shows promising electrical results

© IMEC 2013

Strained Ge pMOS devices

➢ Compressively strained Ge can outperform sSi pMOS

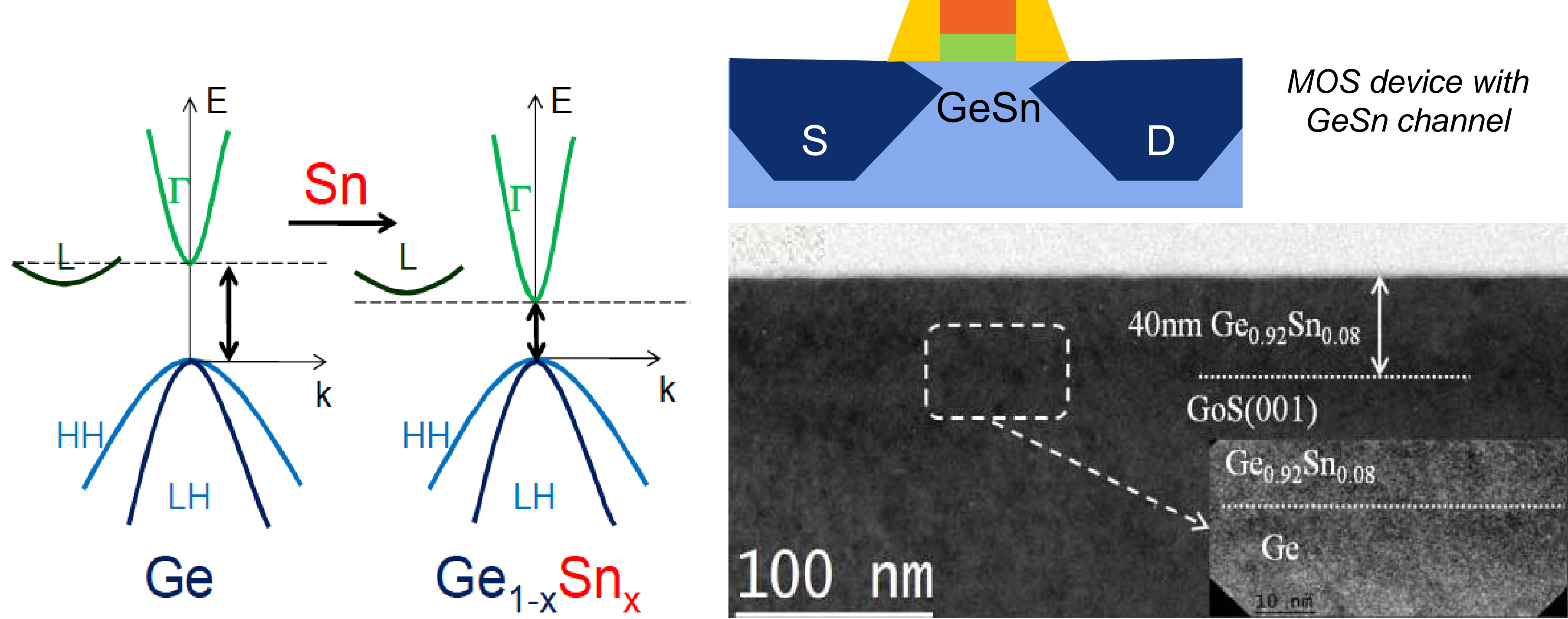


- Compressively strained Ge channels using GeSn requires strained GeSn with Sn content higher than Sn solubility in Ge (<1%)
- Defect free, fully strained GeSn grown on Ge with 8% Sn demonstrated by Atmospheric Pressure –CVD of GeSn at 320ºC

© IMEC 2013

$Ge_{1-x}Sn_x$ devices

- Semiconducting GeSn alloy has tunable bandgap and the possibility of high electron and hole mobility.



- $Ge_{1-x}Sn_x$ is an interesting material for electronic and optical applications
- The extremely low (<1%) solid solubility of Sn in Ge presents considerable difficulties in synthesizing GeSn alloys with good crystallinity.

© IMEC 2013

Alternative materials for CMOS

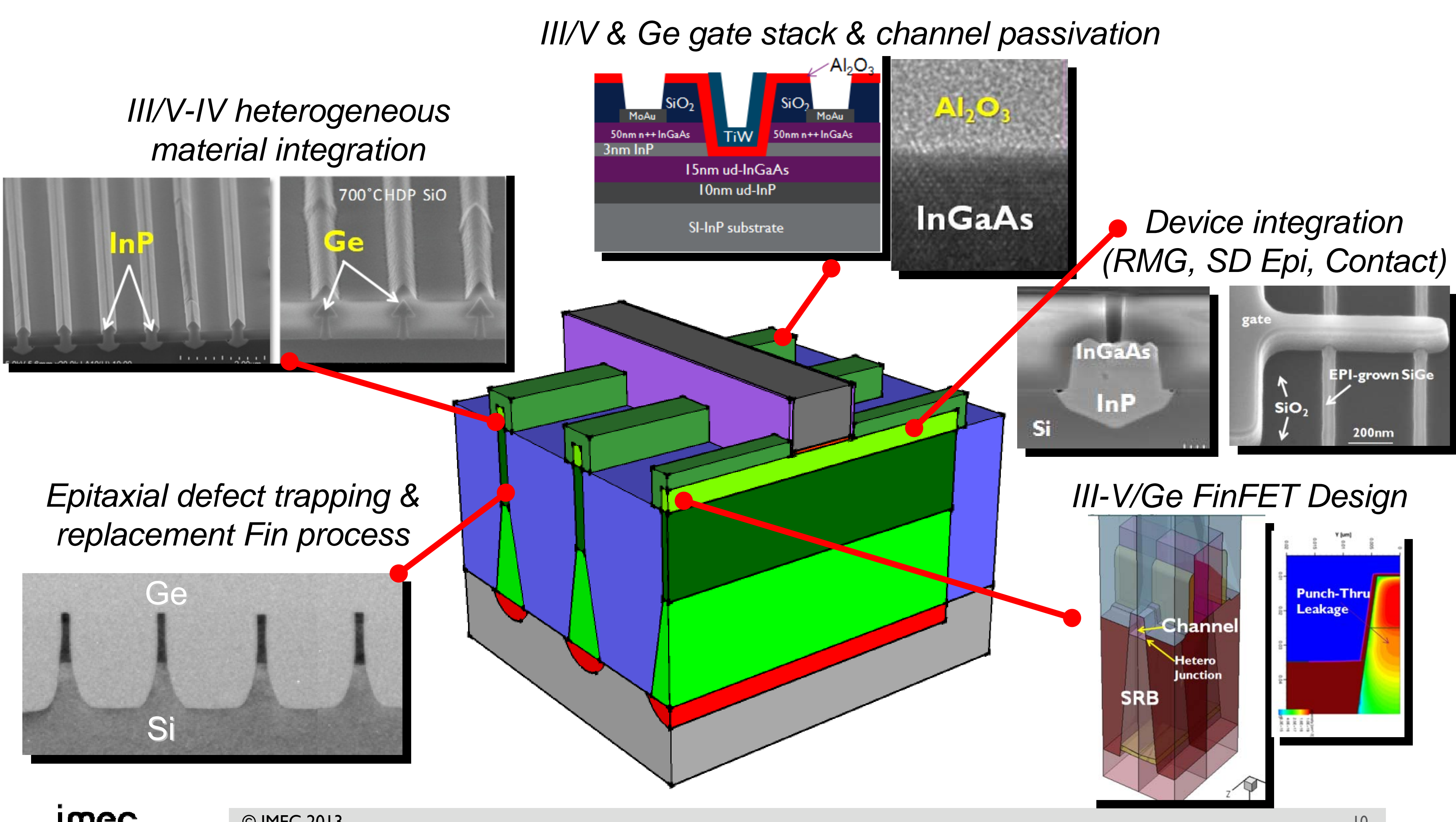
Material / Property	IV – IV		III - V					
	Si	Ge	InP	GaAs	$In_{0.5}Ga_{0.5}As$	GaSb	InAs	InSb
Elec. mobility (cm^2 / V·sec)	1 400	3 900	5400	8 500	12 000	3000	40 000	77 000
Electron effective mass ($/m_0$)	m_t: 0.19 m_l: 0.98	m_t: 0.082 m_l: 1.6	0.082	0.067	0.041	0.041	0.023	0.014
Hole mobility (cm^2 / V·sec)	450	1 900	200	400	450	1000	500	850
Hole effective mass ($/m_0$)	m_{HH}: 0.49 m_{LH}: 0.16	m_{HH}: 0.33 m_{LH}: 0.043	m_{HH}: 0.6 m_{LH}: 0.089	m_{HH}: 0.51 m_{LH}: 0.082	m_{HH}: 0.45 m_{LH}: 0.052	m_{HH}: 0.4 m_{LH}: 0.05	m_{HH}: 0.41 m_{LH}: 0.026	m_{HH}: 0.43 m_{LH}: 0.015
Bandgap (eV)	1.11	0.67	1.34	1.42	0.74	0.72	0.36	0.17
Lattice parameter (A)	5.431	5.658	5.868	5.653	5.868	6.095	6.058	6.479

- Low effective mass ➔ high source injection velocity and drive currents.
- Smaller bandgap materials ➔ low V_t possible with 'reasonable' work-function metals, allowing to reduce V_{dd}

© IMEC 2013

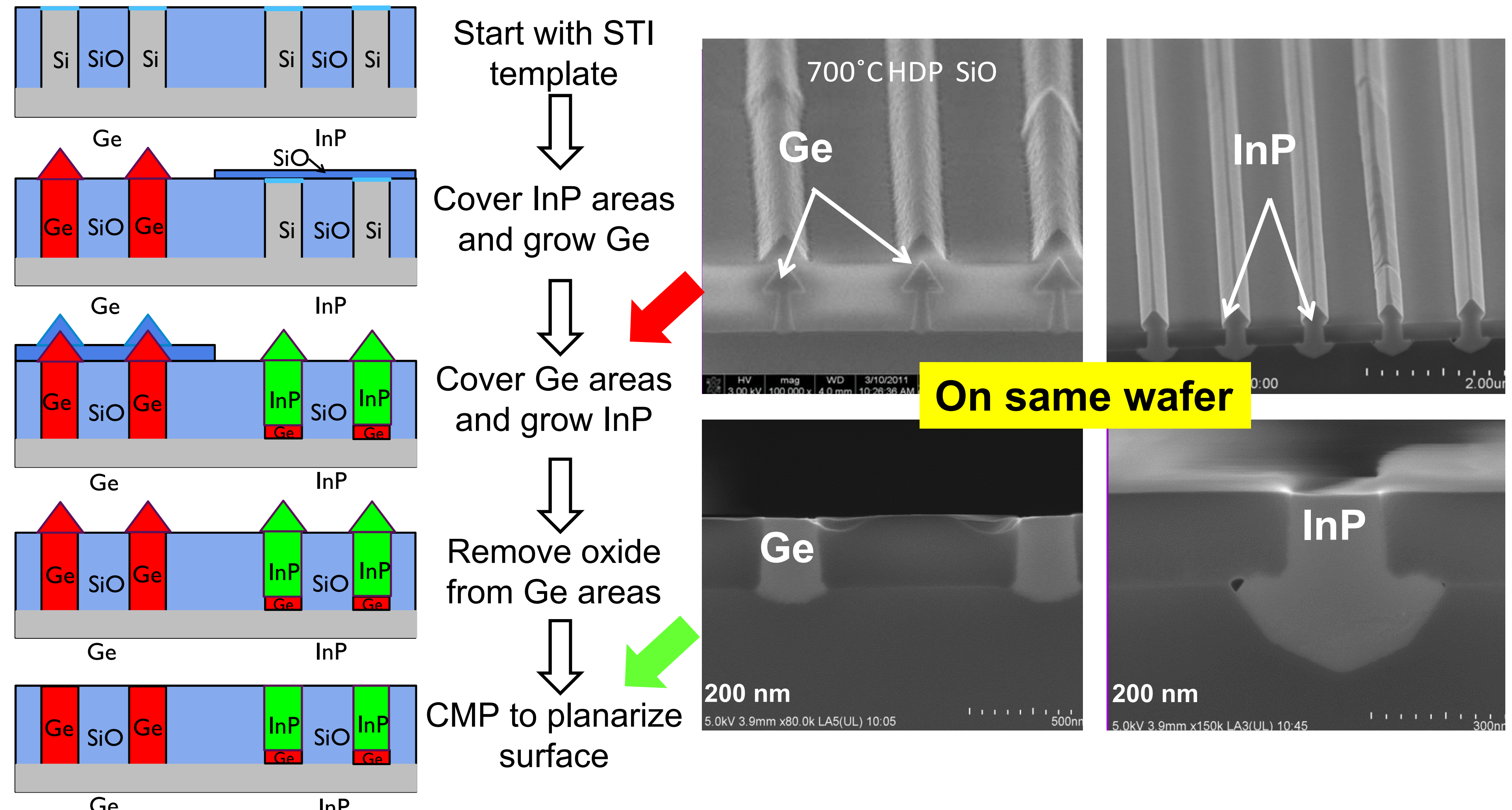
Heterogeneous CMOS integration

- Heterogeneous integration of high-mobility channel materials (Ge and III/V) in FinFETs for next-generation CMOS technology



© IMEC 2013

CMOS Ge and III/V virtual substrate

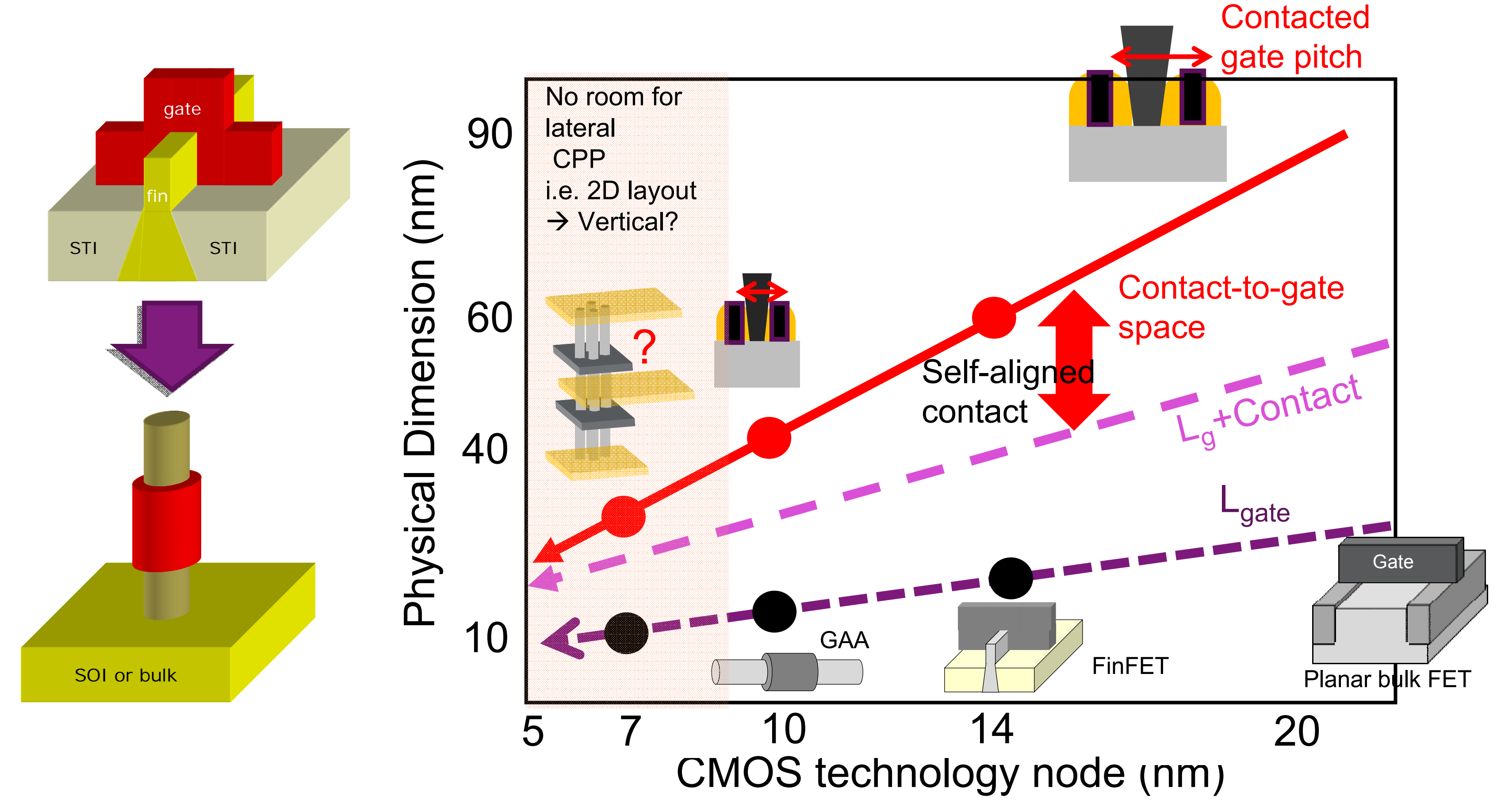


➤ Demonstration of CMOS Ge/InP virtual substrate by ART (Aspect Ratio Trapping)

© IMEC 2013

Density scaling for sub 7nm CMOS

➢ Vertical nanowires will be needed to maintain the density scaling below 7nm.

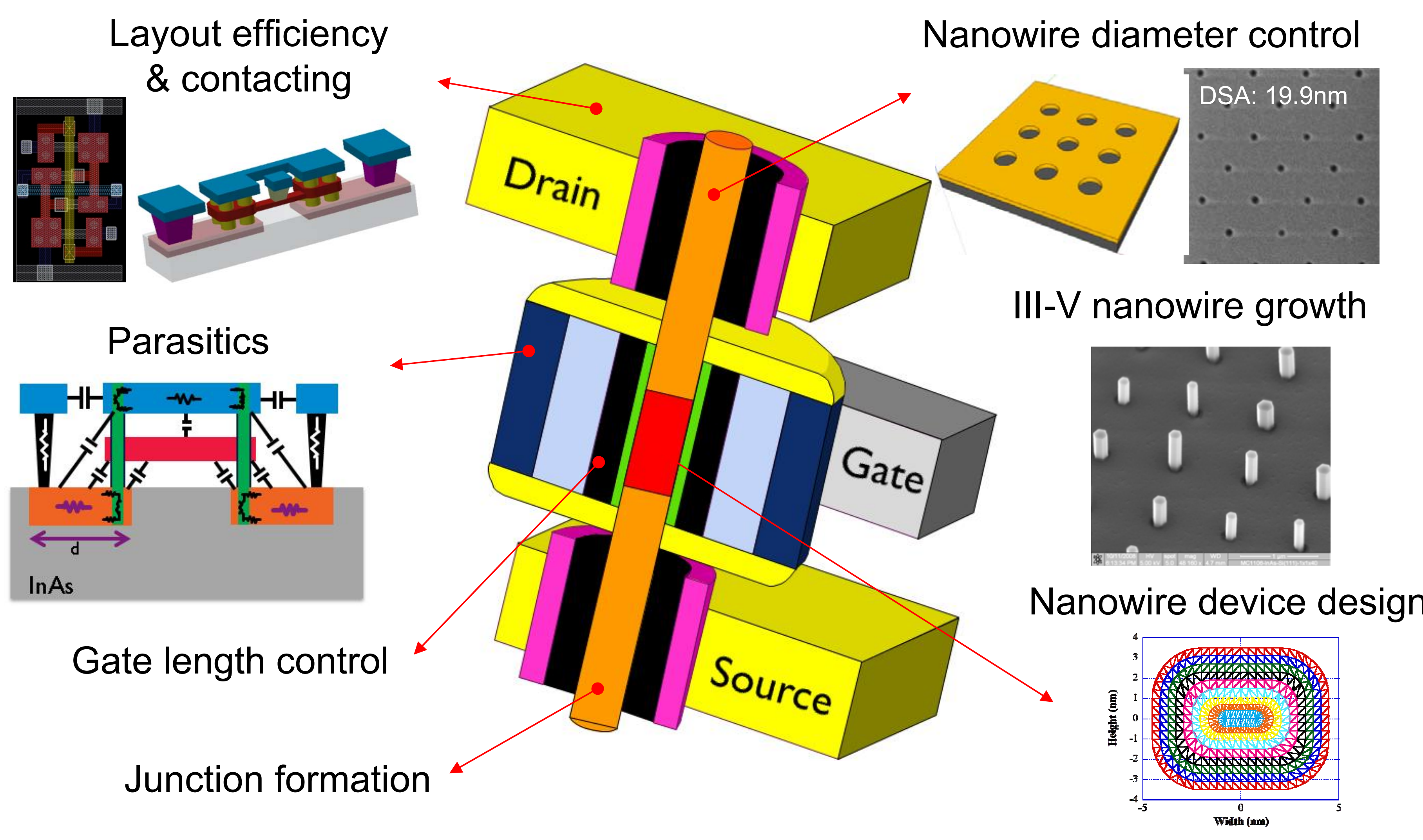


- Contacted gate pitch reduction necessary for continual density scaling
- L_{gate} scaling limited by device electrostatics - out of space for contact and gate

© IMEC 2013

III-V nanowires

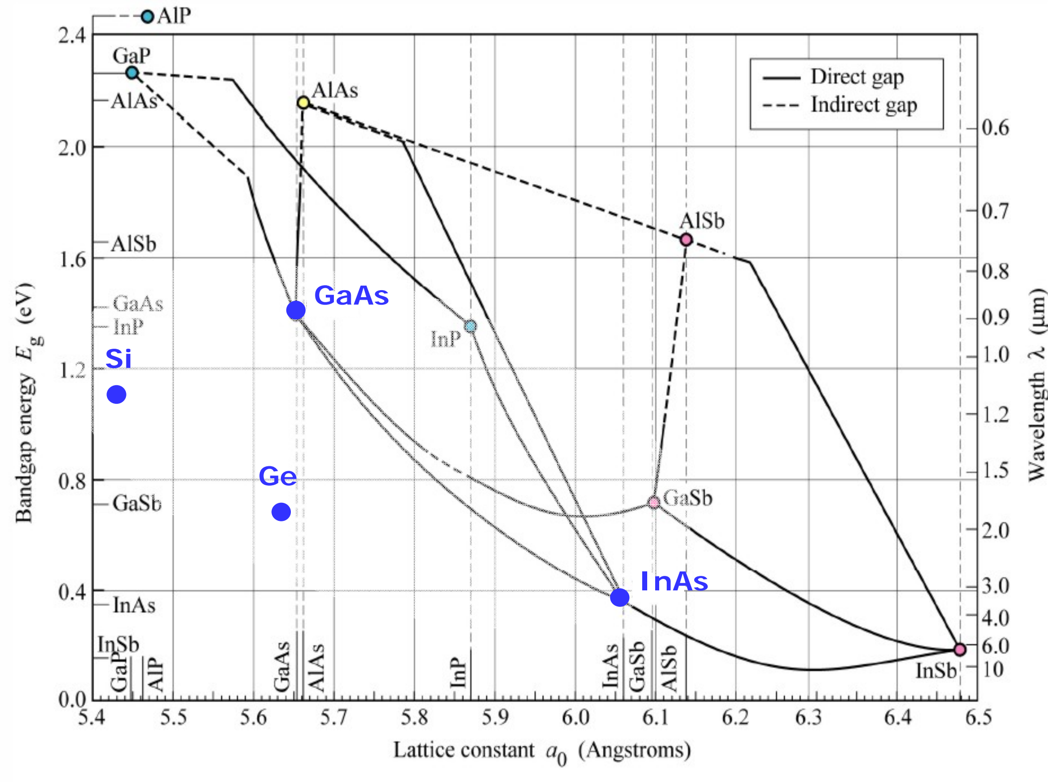
➢ Vertical nanowires will be needed to maintain the density scaling below 7nm.



© IMEC 2013

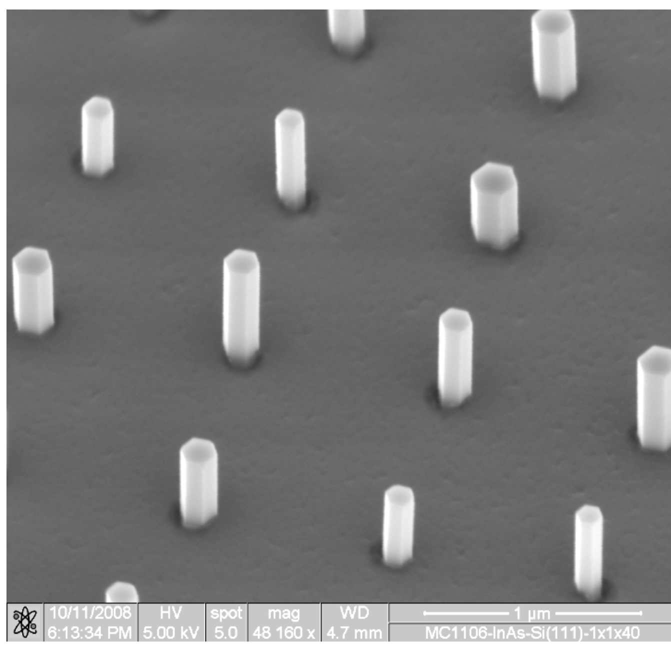
III-V nanowires

- Large lattice mismatch (eg InAs on Si) can be covered by nanowires
- Very interesting technique to introduce various III/V materials on Si



Mismatch w/Si	Ge	InAs	$In_{0.6}Ga_{0.4}As$
Lattice	4.2%	11.6%	8.6%
Thermal	127%	74%	120%

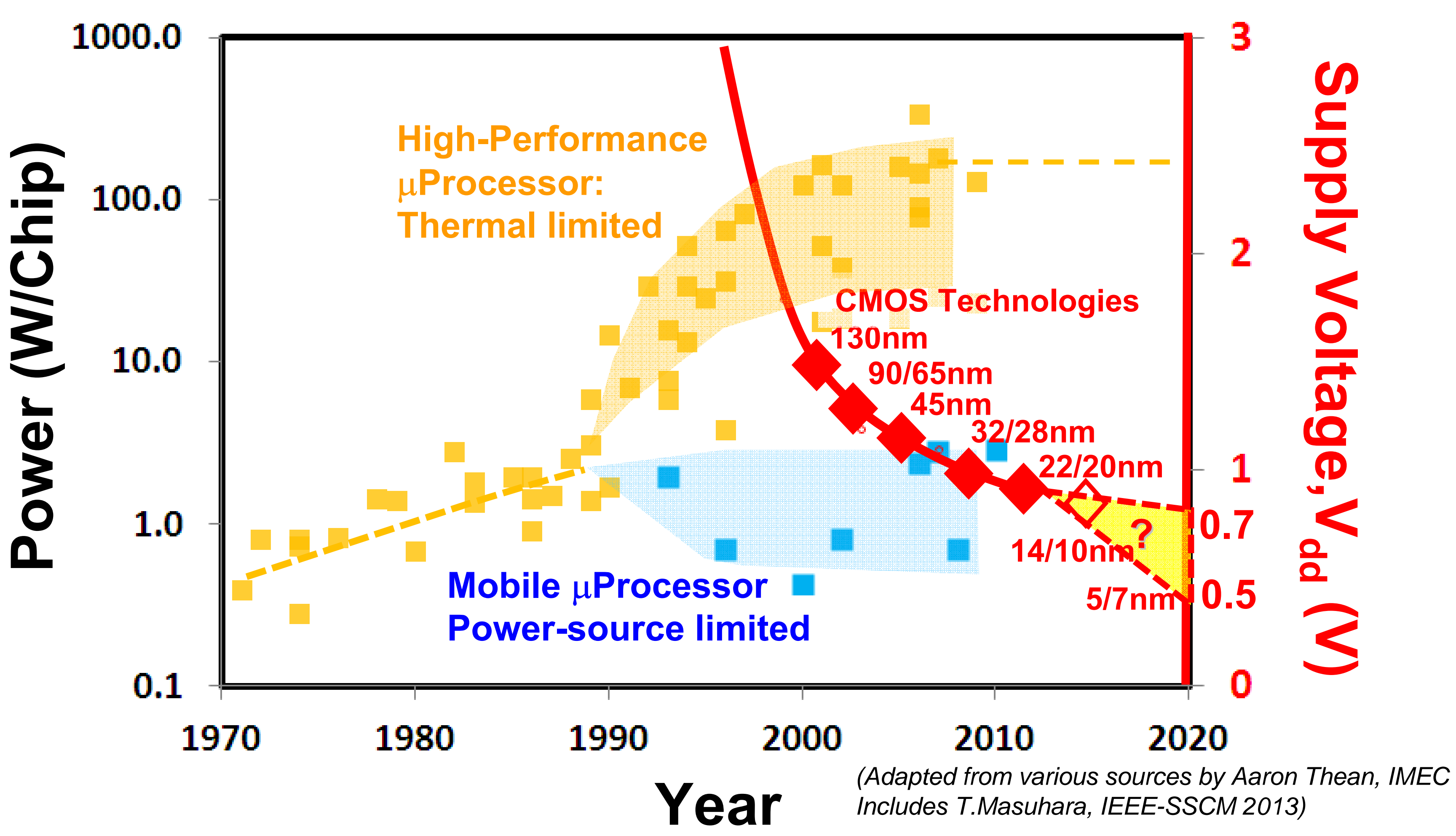
InAs NW growth on patterned Si(111)



- (111) nanowire growth direction
- High growth selectivity
- Desired crystallisation/faceting
- ~0.5 nm/s growth rate
- ~100-200 nm diameter

© IMEC 2013

Power crisis: the need for V_{DD} scaling



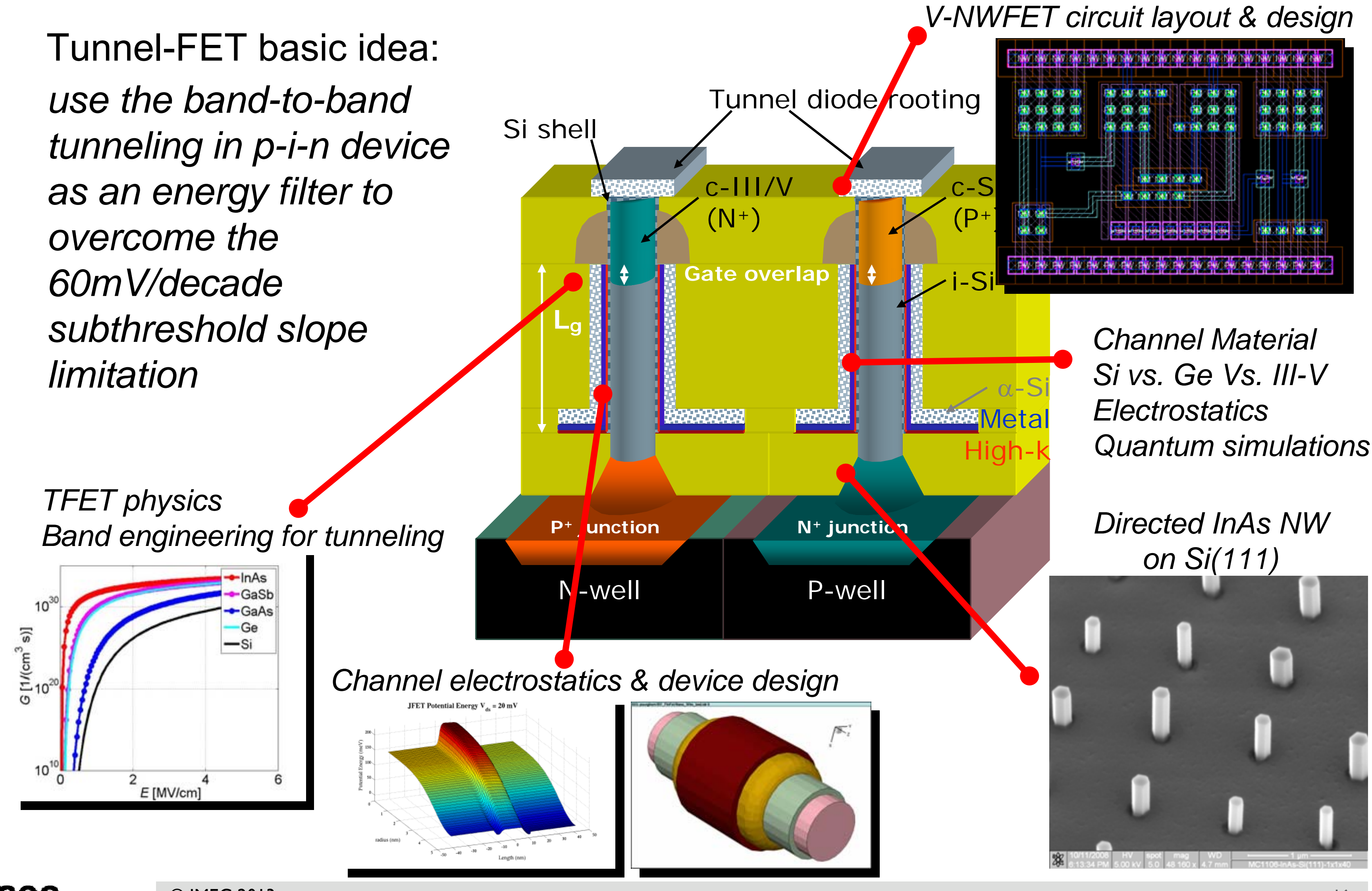
(Adapted from various sources by Aaron Thean, IMEC
Includes T.Masuhara, IEEE-SSCM 2013)

- Higher performance and mobile processors are power limited
- V_{dd} scaling is slowing down

© IMEC 2013

Nanowire / TunnelFETs

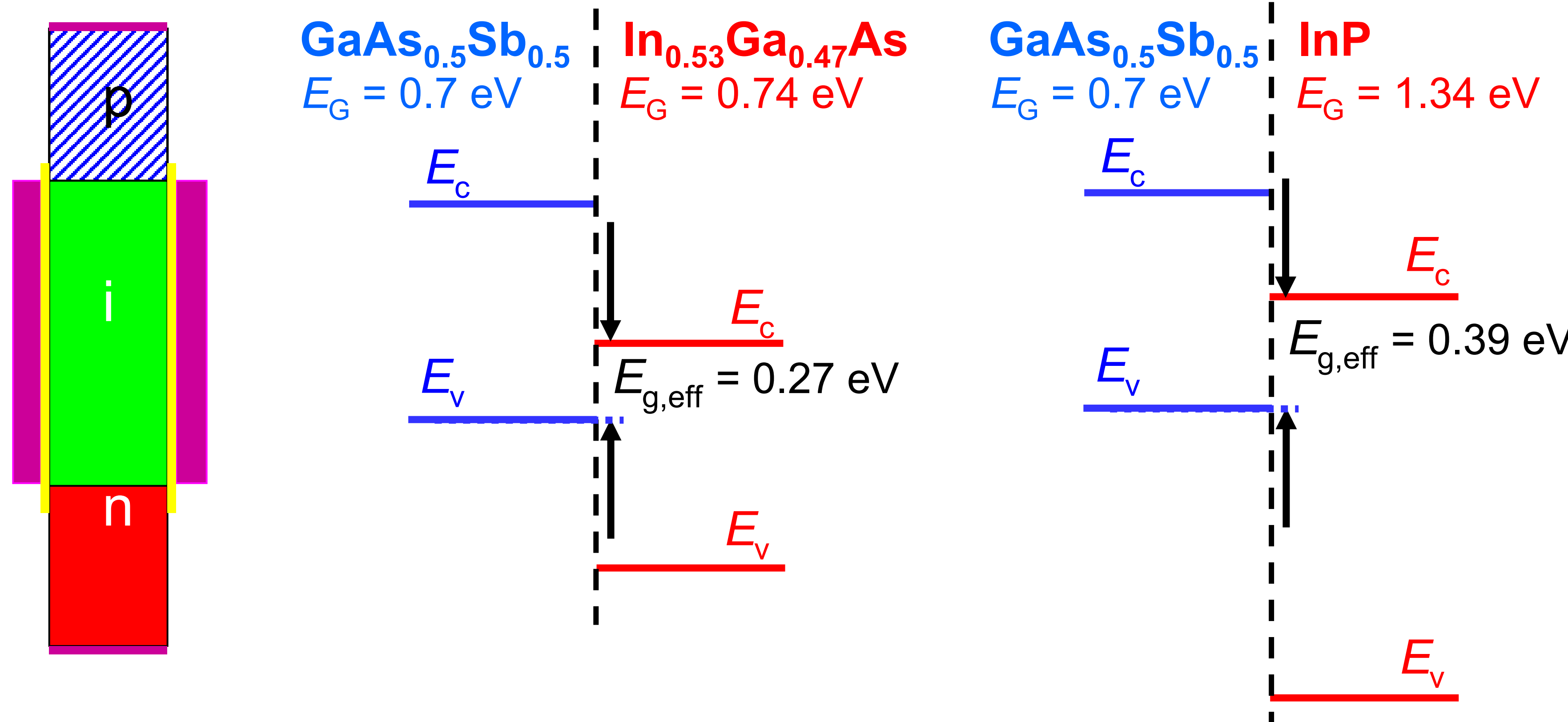
- New devices for reduced power consumption



© IMEC 2013

Heterojunction TunnelFET

- New devices for reduced power consumption

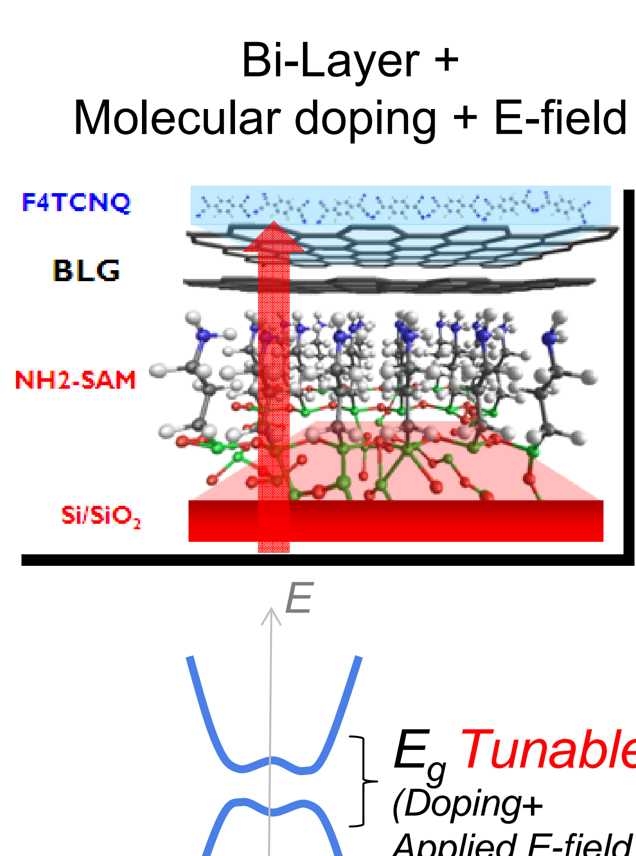


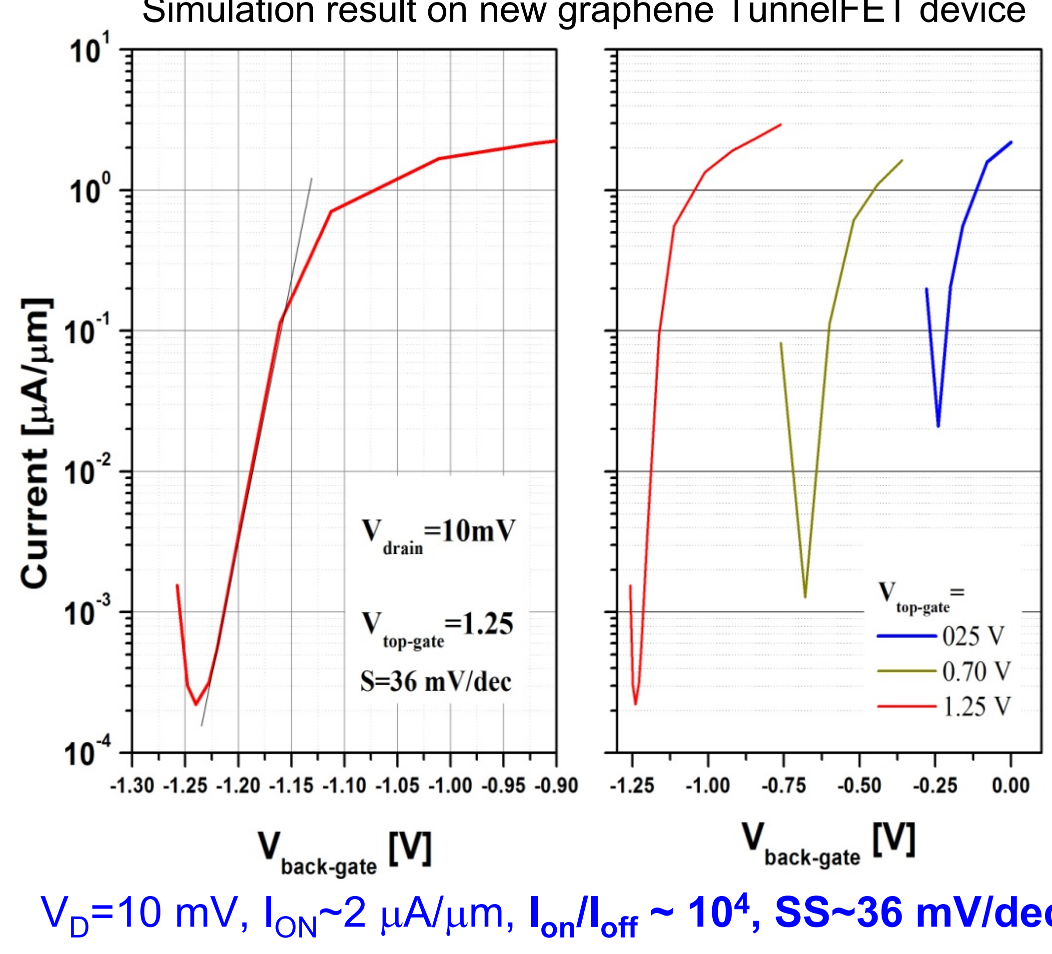
- Both configurations are lattice matched:
  - $GaAs_{0.5}Sb_{0.5}$ – $In_{0.53}Ga_{0.47}As$: for highest I_{on}
  - $GaAs_{0.5}Sb_{0.5}$ – InP: for lowest I_{off}

© IMEC 2013

Graphene beyond CMOS devices

- In bi-layer graphene the effective band-gap can be "tuned" electrostatically
- TunnelFET devices in graphene should provide good I_{on}/I_{off} and steep subthreshold for low power



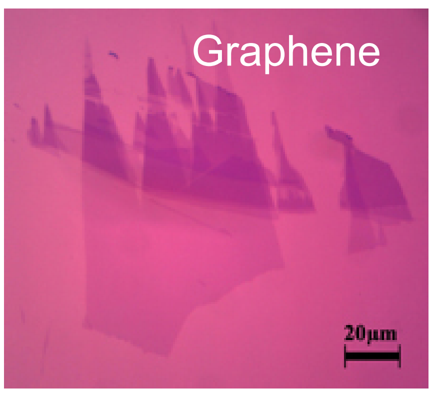


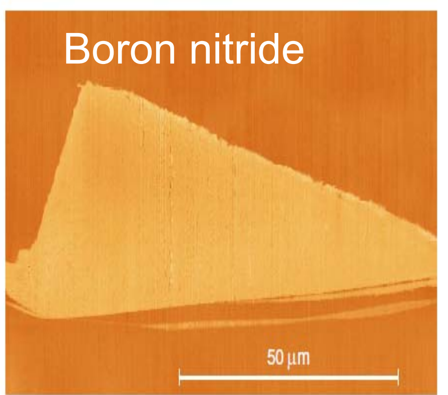
V_D=10 mV, I_{ON}~2 μA/μm, **I_{on}/I_{off} ~ 10^4, SS~36 mV/dec**

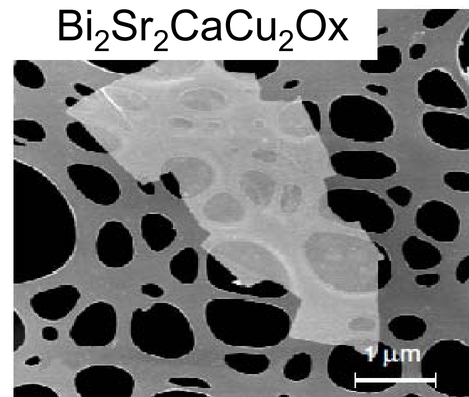
© IMEC 2013

Many other 2D materials possible

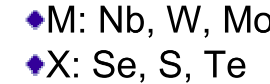
Obtained by exfoliation ("scotch tape") from bulk crystals!



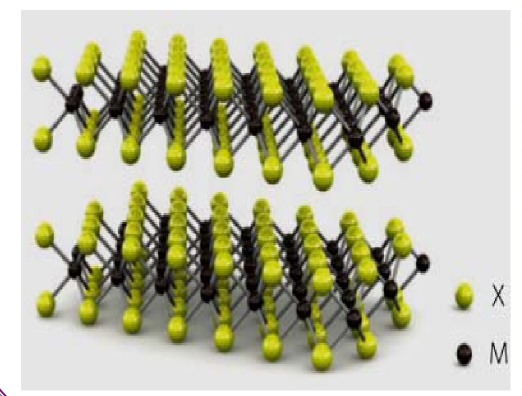


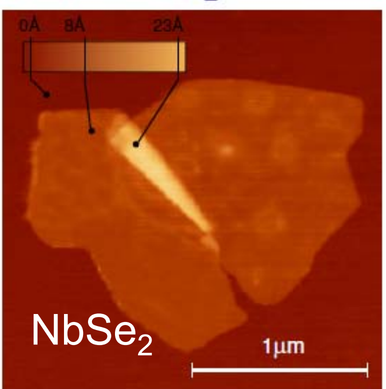


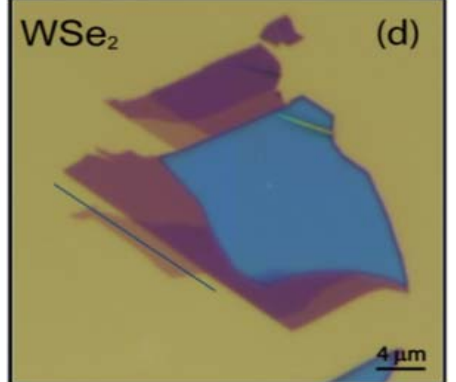
Layered metal dichalcogenides (MX_2)

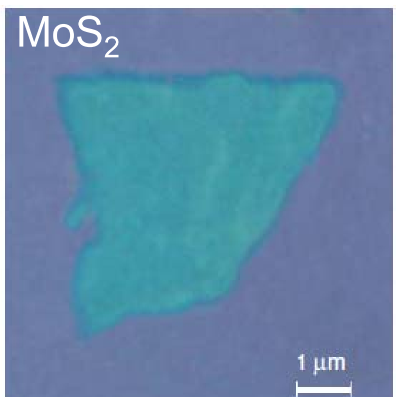


- M: Nb, W, Mo
- X: Se, S, Te





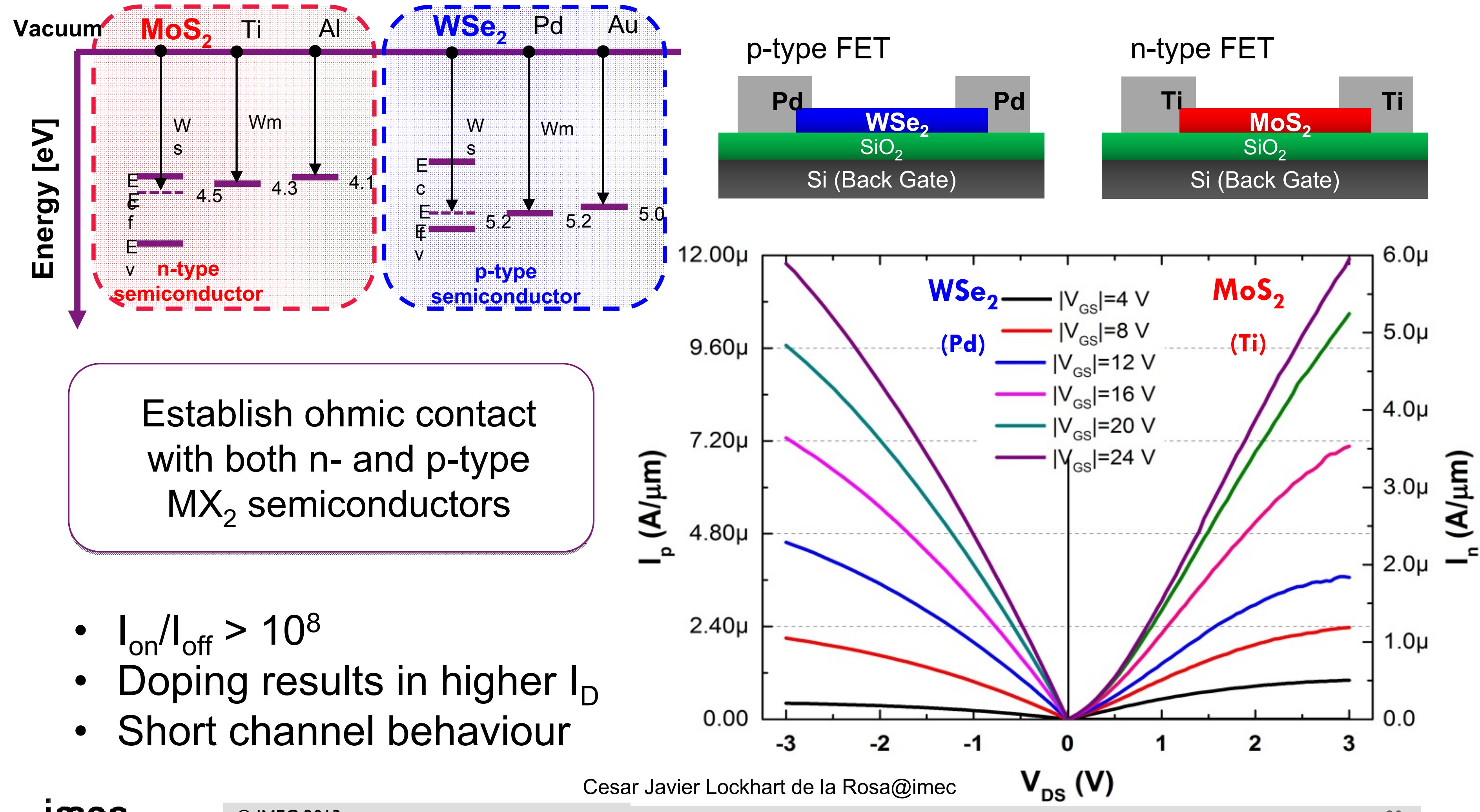




Geim *et al*, Manchester PNAS 2005

p- and n-MOS monolayer MX_2 FETs

- 2D materials can be used to produce CMOS
- These materials can also be used on flexible substrates



Establish ohmic contact with both n- and p-type MX_2 semiconductors

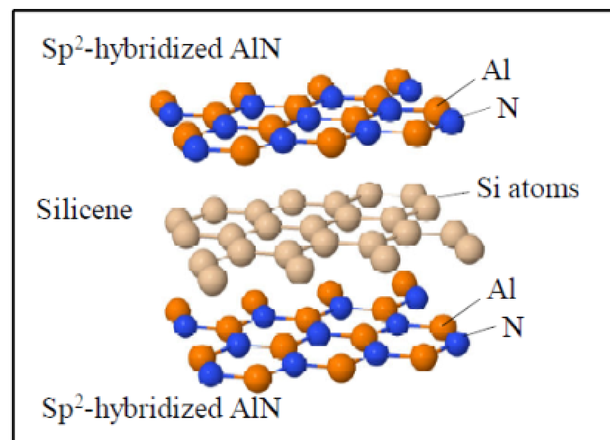
- $I_{on}/I_{off} > 10^8$
- Doping results in higher I_D
- Short channel behaviour

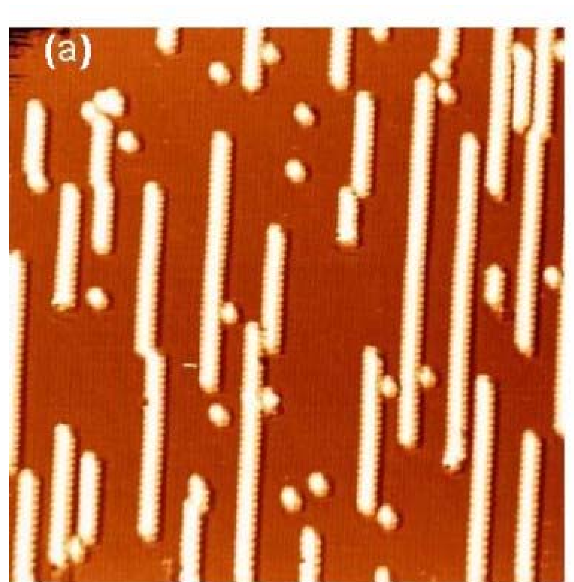
Cesar Javier Lockhart de la Rosa@imec

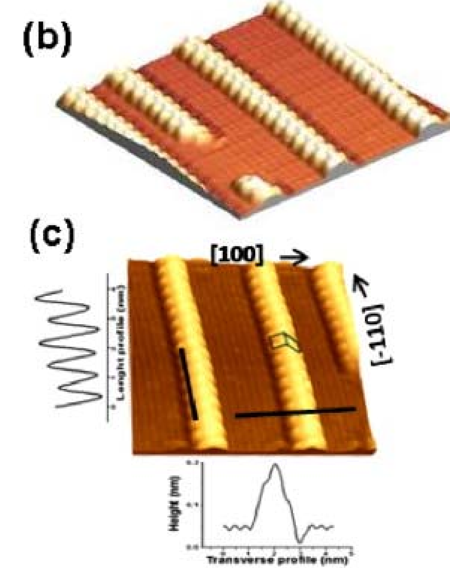
© IMEC 2013

2D materials: Silicene

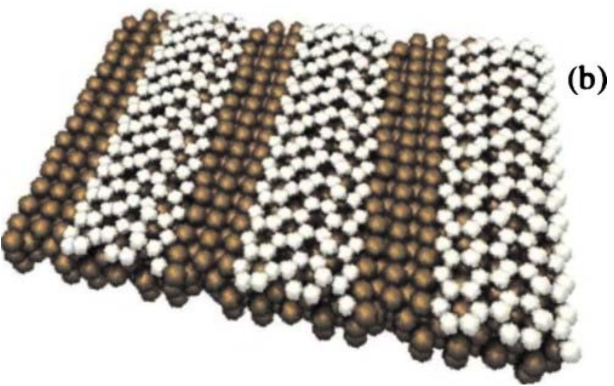
- Silicene is the Si equivalent of graphene.
- Promising results have been obtained on silicene nanoribbon fabrication on Ag surfaces.
- Can also be made on AlN







STM images of straight, parallel 1D silicon nanostructures grown on a Ag(110) surface. (a) Large view (42×42 nm2, filled states); (b) 3D view (12×12 nm2, filled states); and (c) detailed view (6.22×6.22 nm2, filled states).



Filled-states STM image, 11×10 nm2 (V = −3.3 V, I = 1.90 nA) of the dense array of SiNRs forming a 1D grating with a pitch of ~ 2 nm (a); ball model of the corresponding calculated atomic structure (b).

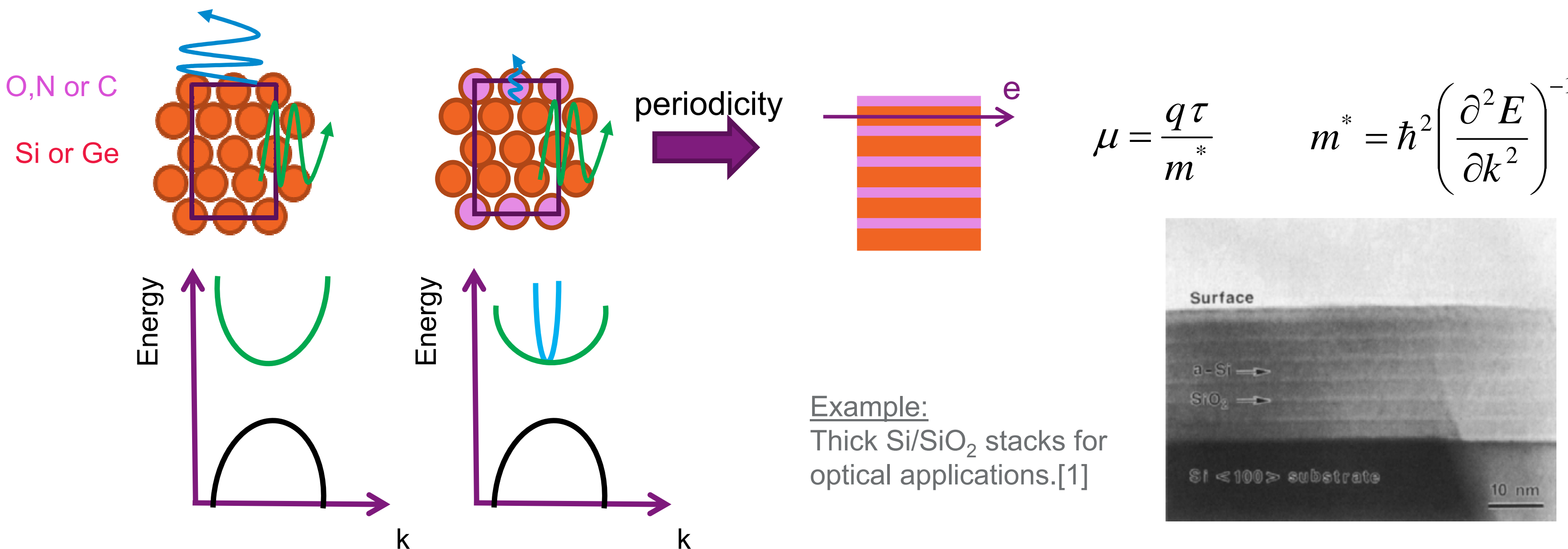
P. De Padova et al, Appl. Phys. Lett. 96, 261905 (2010), B. Aufray et al, Appl. Phys. Lett. 96, 183102 (2010)

© IMEC 2013

Bulk quasi-2D superlattices

Generating anisotropic band structures

- Lower effective mass in transport direction: higher mobility
- Enhanced effective mass in perpendicular direction: (➔lower leakage and less interaction with insulator defects)



➢ EPI growth of Si/Ge stacks with a (sub)-monolayer thick interspersing species to tune the band structure.

➢ Modeling of the electronic properties and of transport combined with material growth and experimental characterization.

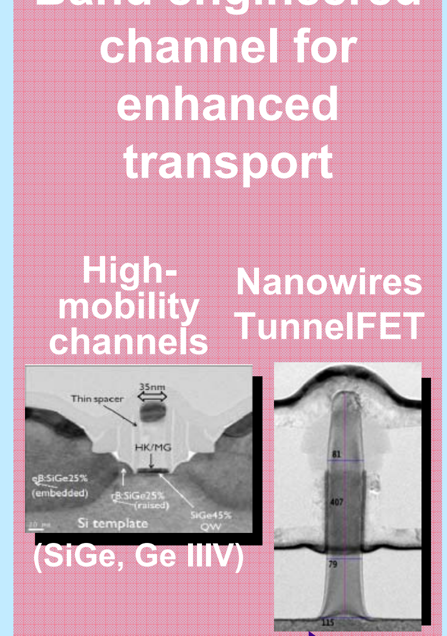
[1] Lu *et al*, nature, 378, p. 258 (1995)

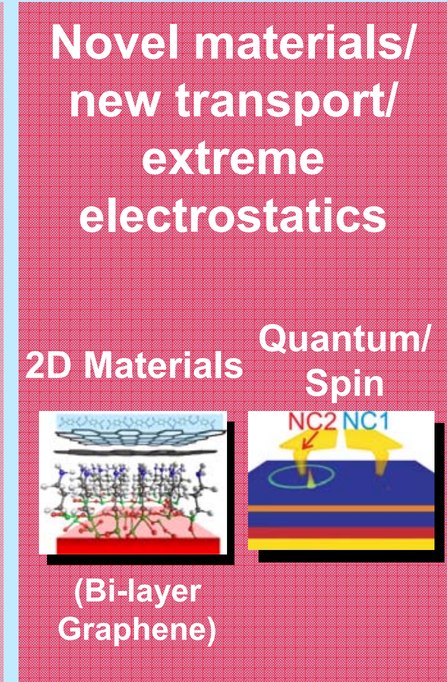
© IMEC 2013

Logic scaling trend and roadmap

V_{dd} 1.0-1.1V 0.9-1.0V 0.8-0.9V 0.7-0.8V 0.6-0.7V 0.5-0.6V < 0.5V

- **CMOS with high mobility channel materials**
  - Ge and III/V CMOS
- **Steep subthreshold devices**
  - Nanowires for improved electrostatics
  - Steep subthreshold devices (e.g. TunnelFETs) for reduced power
- **2D(-like) materials**
  - Graphene, silicene, MoS_2, nanolattices, …
- **Novel devices and logic concepts**
  - Spin-based devices, topological insulators, non-Boolean logic, MTJ logic, memristors,





Power reduction is the major challenge

Many new materials and devices will be implemented in future CMOS to maintain the performance scaling

© IMEC 2013

Global collaboration including entire value chain is required to address the huge R&D challenges.

Uachtaránacht na hÉireann ar Chomhairle an Aontais Eorpaigh
Irish Presidency of the Council of the European Union
eu2013.ie

JOINT MULTI-DISCIPLINARY R&D

…THE KEY TO INNOVATION

Thank you for your attention

MARC HEYNS

IMEC
Kapeldreef 75, B-3001 Leuven, Belgium
also at MTM, KULeuven, Belgium

KU LEUVEN