Computing with Nanoelectronic Devices

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Outline

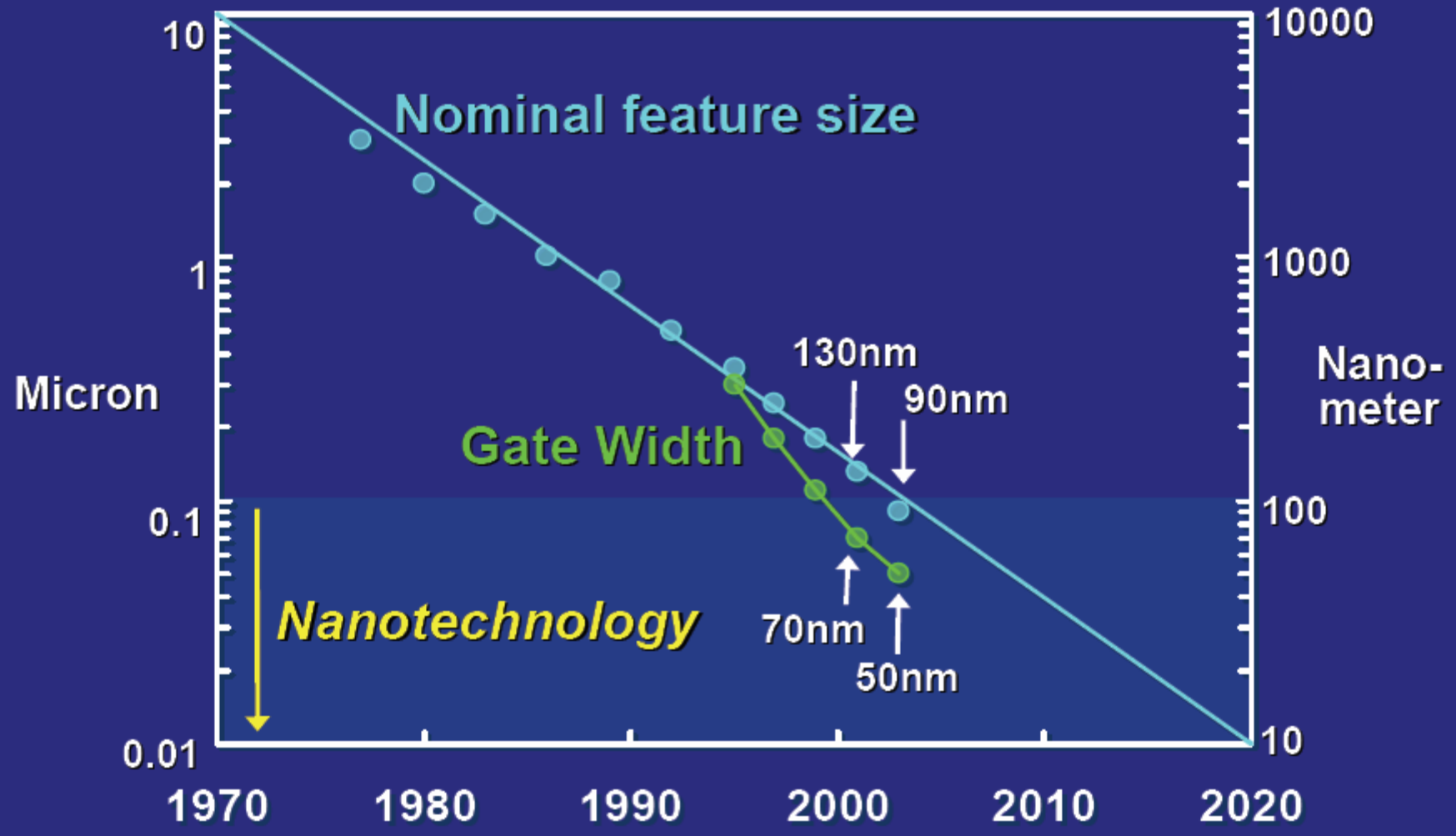
- Applications challenges for computing and communications
- Semiconductor capabilities and limitations to meet these challenges
- Current nanoelectronics device capabilities and limitations
- Infrastructure needs for future nanoscale electronics – technology integration, circuit design, and architecture

Inputs from the 2005 Revision of the Emerging Research Devices section of the International Technology Roadmap for Semiconductors and Dr. George Bourianoff, Intel

Applications Challenges for Computing and Communications

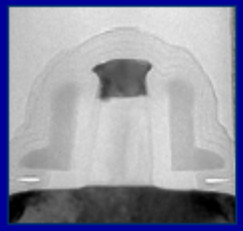
- Current architecture improvements are limited by slow down in density and clock speed increases
- Multiple core approaches increase already strained demands on memory latency, access time, and bandwidth to feed processors
- Memory hierarchies are still limited by magnetic and optical data storage millisecond seek times as well as by flash end-of-scaling
- Many important applications do not benefit from improvements in existing architectures – e.g. data streaming, graphics, video, deep searching, secure communications, remote sensing, self configuring and repairing networks – for mostly portable/mobile applications
- Most new portable/mobile applications will require online reconfigurability to accommodate multiple and changing standards as well as updates for security and search engine improvements

Silicon Nanotechnology is Here!



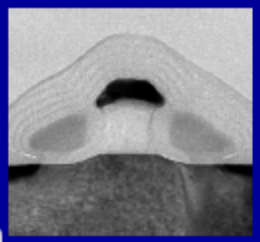
Nanotechnology will extend CMOS scaling

90nm Node
2003



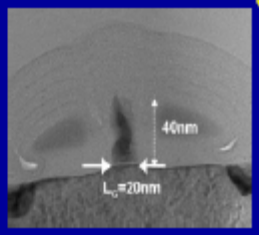
50nm Length
(IEDM2002)

65nm Node
2005



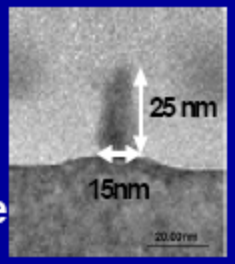
30nm
Prototype
(IEDM2000)

45nm Node
2007



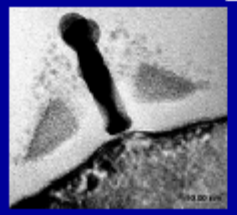
20nm Prototype
(VLSI2001)

32nm Node
2009



15nm Prototype
(IEDM2001)

22nm Node
2011



10nm Prototype
(DRC 2003)

2003

2012

Nanotubes, nanowires

1-3nm

2013 – 2017

16 nm node
2013

7nm

11nm node
2015

5nm

8 nm node
2017

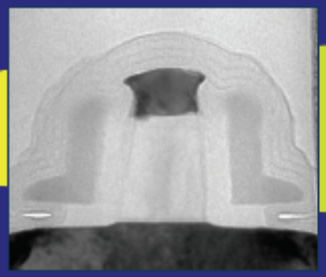
3nm

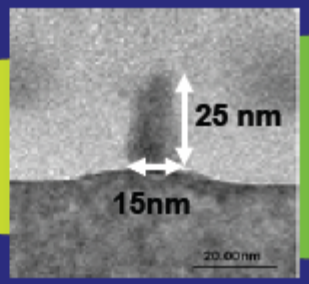
Innovations like quantum dots,
Nanowires, Naotubes, etc.

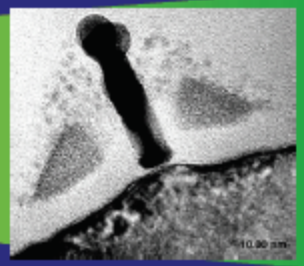
Semiconductor Capabilities and Limitations to Meet Future application Challenges

- Future FET designs will scale to the 11nm node slated for production in the 2012-2015 timeframe
- On-chip interconnects are “reverse” scaling – requiring larger dimensions for the higher densities and clock speeds
- Major limitations occur due to power dissipation (fixed at 1E-21J per switching gate) and current leakage (both on-state and off-state) due to tunneling through the thinner gate dielectric and lower operating voltages
- So overall raw performance for existing architectures will not improve significantly for future technology generations
- The real performance gains must be achieved by integrating new technologies onto CMOS – i.e. increasing the functionality of basic CMOS for new applications

Expanding Moore's Law







50nm Prototype (IEDM2002)

15nm Prototype (IEDM2001)

10nm Prototype (DRC 2003)

EXPANDING

Sensors

Photonics

Biological

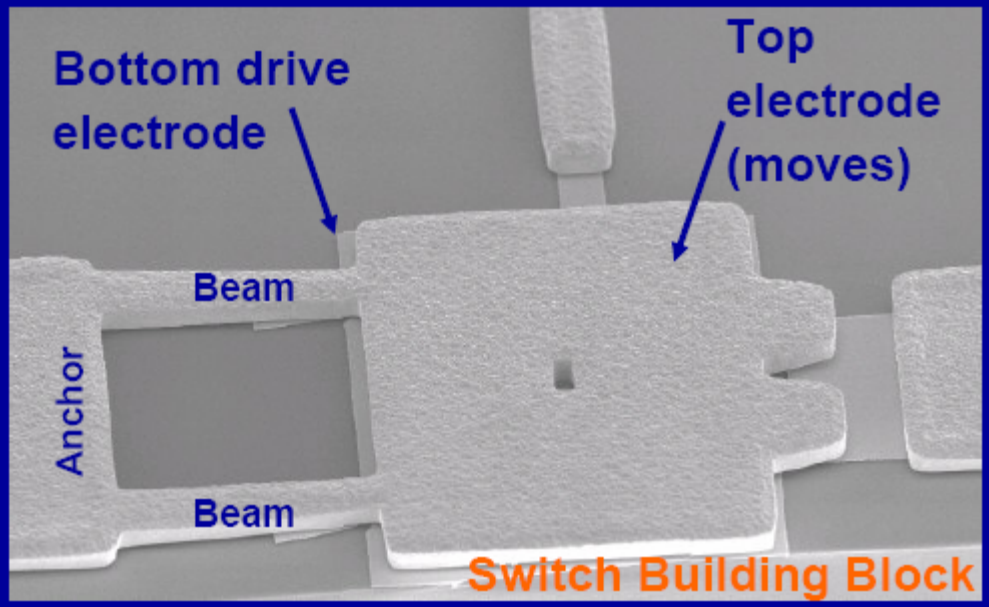
Nano

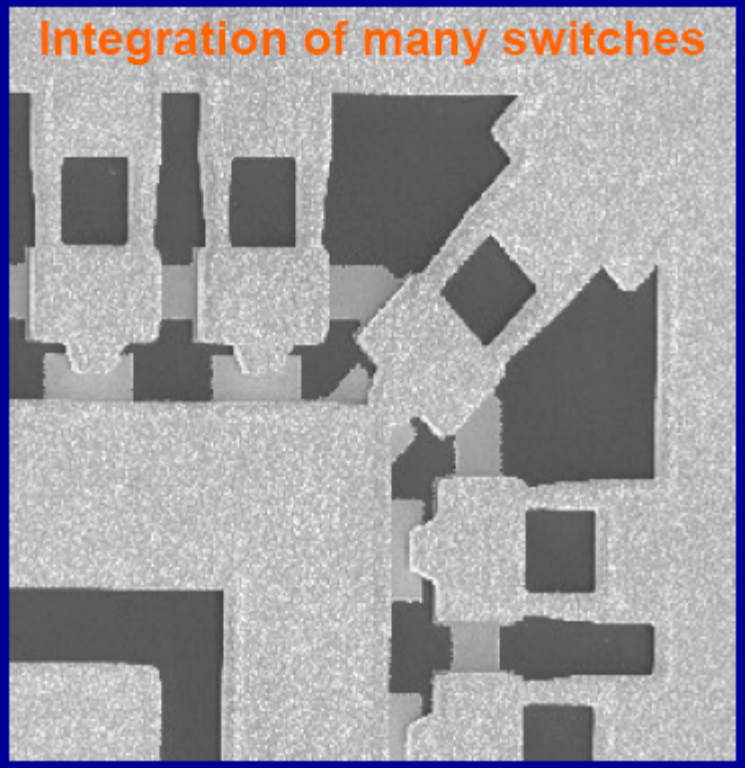
Fluidics

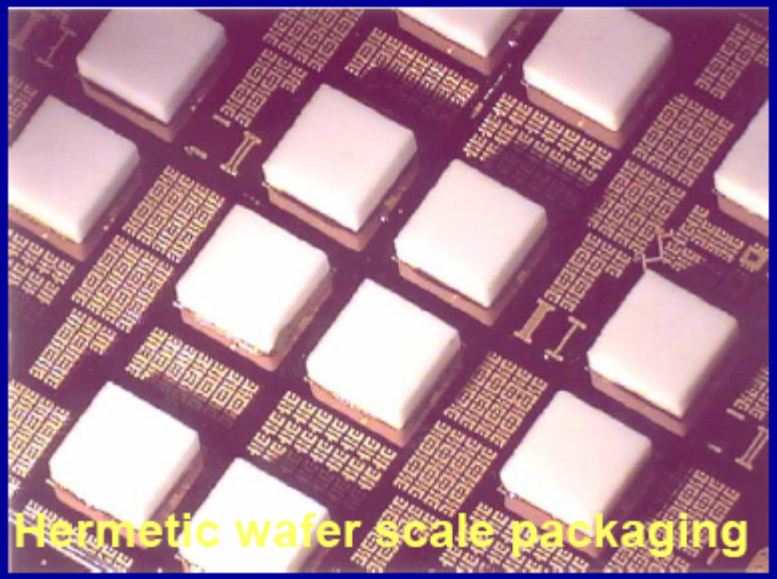
Wireless

Mechanical

MEMS for RF switching





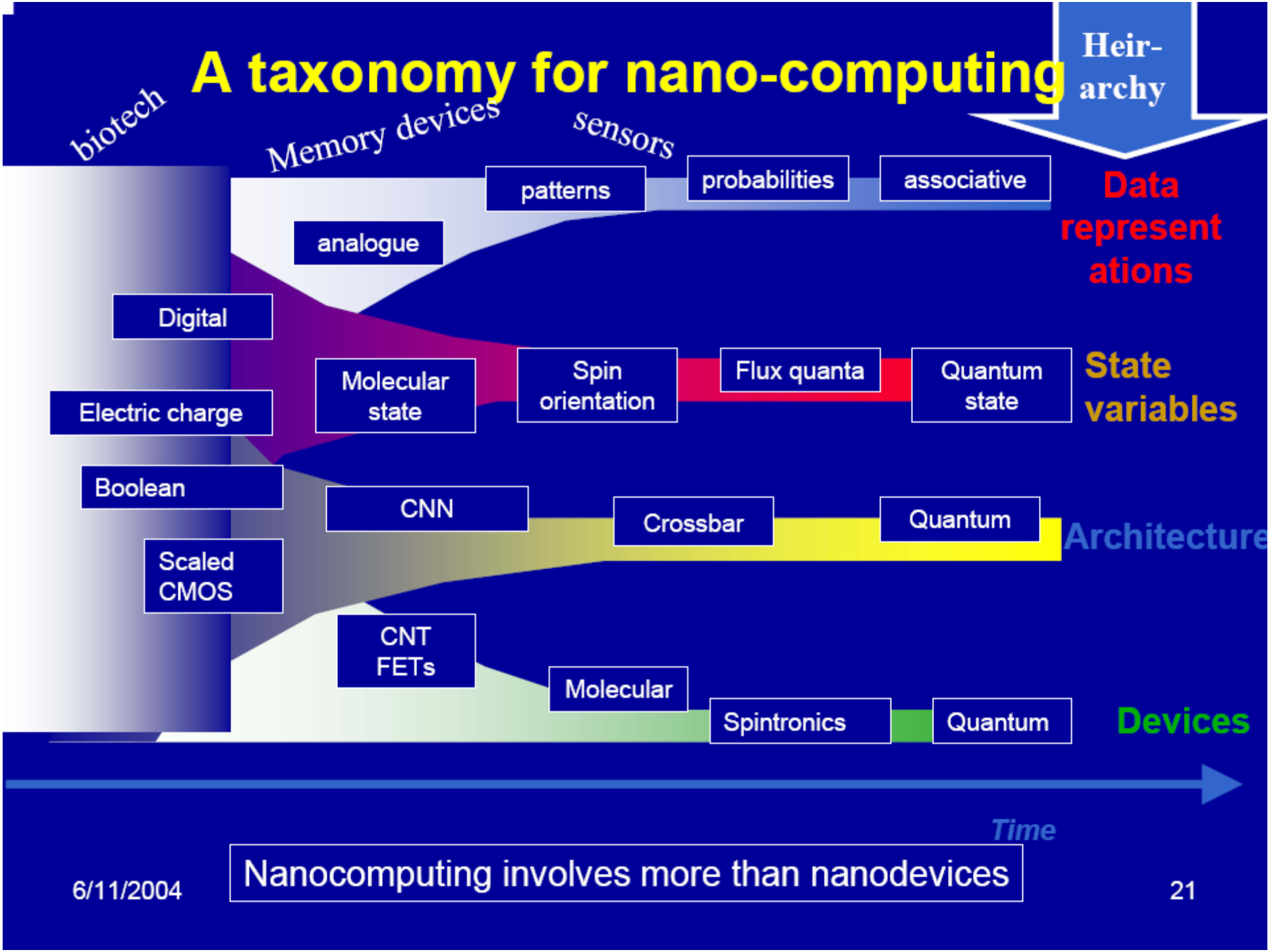


- Laterally lithography requirements are only n-5:
  - Mechanical devices are large10 µm -100 µm
- Vertically:
  - Layer thickness control requirement are extremely stringent: **"Nanometer sized gaps"**
  - Advanced materials with excellent mechanical and electrical properties are needed

Current Nanoelectronics Device Capabilities and Limitations

- New nanoscale electronic devices offer some new capabilities
  - Increased densities – potentially to 1e12 cm^{-2}
  - New bandgap engineered structures such a silicon nanowire nanolasers and Si – compound semiconductor heterostructures for increased mobility and reduced power.
  - Improved carrier mobility due to decreased scattering and quantum confinement
- But nanoscale electronic devices also present some new limitations
  - Increased property variability due to intrinsic process variations
  - Increased defect levels due to increased demands for lower particulates, contamination levels, and heterointegration
  - Unknown reliability failure modes due to high electric fields, unstable contacts, and non-equilibrium metamaterials
  - Inability to manufacture monolithically with needed registration and alignment over large dimensions
  - Poor integration technology to basic CMOS
  - Decreased feature sizes do not address important analog device and circuit needs

A taxonomy for nano-computing

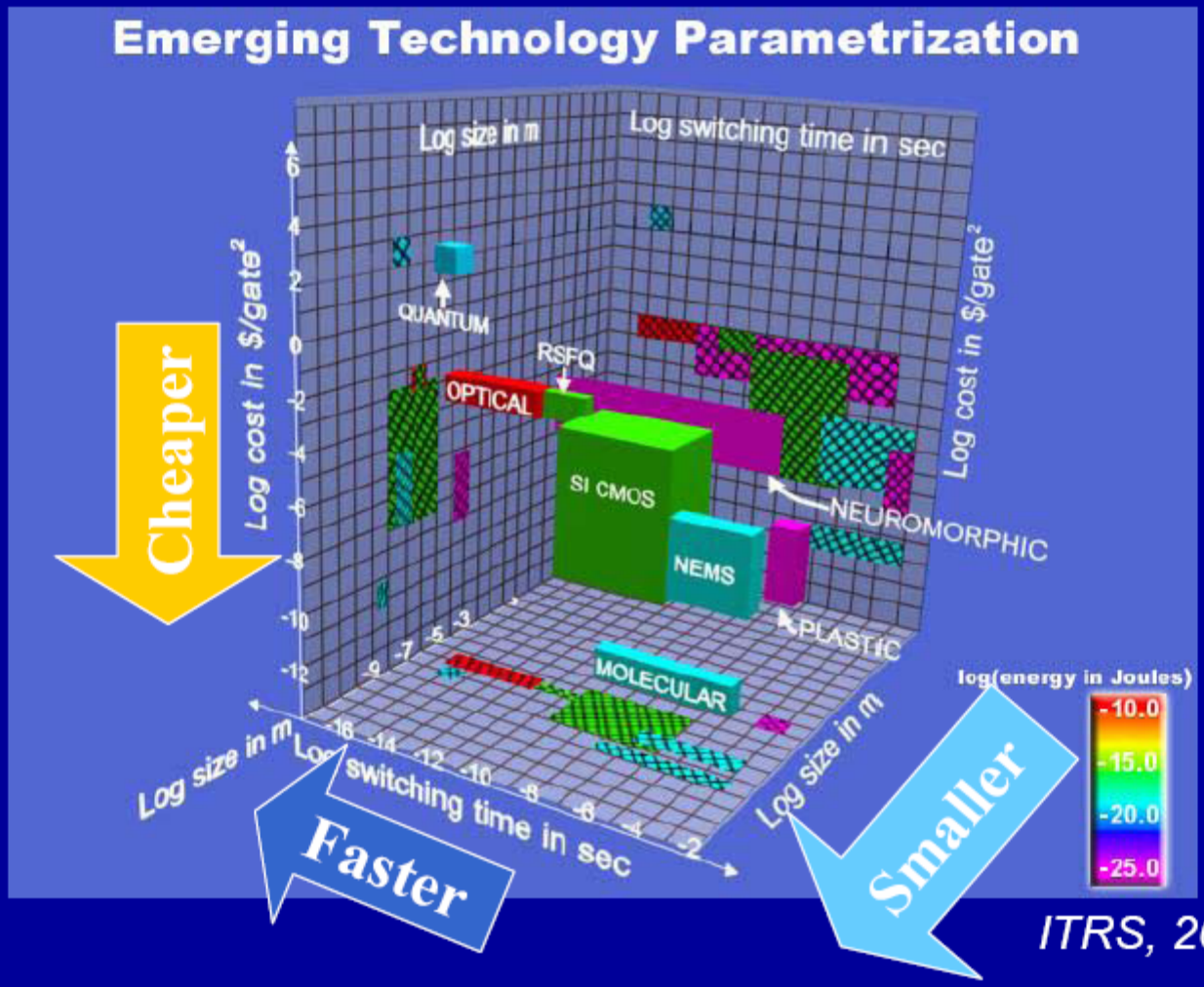


Nanocomputing involves more than nanodevices

Implications of Nanoelectronics Device Limitations

- Schemes to manage variability and defects will reduce the number of devices available for useful computing and communications (by some estimates to 1E9 from 1E12 cm^{-2} for expected defect levels of 5-10%)
- Logic applications will require 3-D structures and non-Manhattan layouts not favored by “bottoms-up” processing schemes
- Multiplexing schemes to manage the interconnect pitch transformation from nano- to microscale will require additional real estate
- Charge-based devices will still dissipate unacceptable power
- Spin-based devices still need to demonstrate gain and to transform spin to charge and vice versa for connection to the external world

Radical technologies beyond CMOS



ITRS, 2001

Nothing beats scaled silicon but nanotechnology can complement

Synergy Between Nanoscale Devices and Architectures for Nanoscale Electronics

- Today's nanoscale charge-based devices are switches with voltage and current gain so that large fanout and circuits can be sustained
- Nanoscale spin based devices have not demonstrated gain so far
- However if individual devices posses more complex, nonlinear input-output functions, then logic functions could be subsumed into individual devices and result in circuit and interconnect simplification
- One example is neuromorphic computing where thresholding of accumulated charge determines the transmission properties of neurons
- New architecture concepts may be stimulated by the availability of such functional nanodevices
- Also new device concepts may be stimulated by new architectures that meet requirements of applications such as data streaming

Infrastructure Needs for Future Nanoscale Electronics

- Technology Integration
  - Process control – low temperature, reduced statistically variability
  - Device structures – multiple technology devices (Si/III-V)
  - Package including MEMS structures – integrated interconnect transformations to the external world
- Circuit Design
  - New device characteristics – multiple functional device concepts
  - Device variability – manage low signal/noise, low gain, high fan-out
  - Mixed signal models – integrate analog and digital functions
  - Design tools – integrated across multiple technologies
- Architecture
  - New memory hierarchy – on chip cache integrated vertically in interconnect stack
  - Hardware functions -> software (such as software radio)
  - “Pixel” management – smart pixels with embedded computation nodes for pattern recognition and transfer
  - Self configuring, neuromorphic organizations based on highly parallel and slower applications that integrate to faster CMOS for supporting algorithm execution