Dual Work Function Metal Gate CMOS Technology Using Metal Interdiffusion

Igor Polishchuk, *Student Member, IEEE*, Pushkar Ranade, *Student Member, IEEE*, Tsu-Jae King, *Senior Member, IEEE*, and Chenming Hu, *Fellow, IEEE*

***Abstract*—In this letter, we propose a new metal-gate CMOS technology that uses a combination of two metals to achieve low threshold voltages for both n- and p-MOSFET's. One of the gate electrodes is formed by metal interdiffusion so that no metal has to be etched away from the gate dielectric surface. Consequently, this process does not disturb the delicate thin gate dielectric and preserves its uniformity and integrity. This new technology is demonstrated for the Ti–Ni metal combination that produces gate electrodes with 3.9 eV and 5.3 eV work functions for n-MOS and p-MOS devices respectively.**

***Index Terms*—Interdiffusion, metal gate CMOS, nickel, titanium, work function, x-ray photoelectron spectroscopy.**

I. Introduction

REDUCTION of the capacitance-equivalent thickness (CET) of the gate dielectric remains a major challenge for scaling CMOS technology beyond the 100-nm node. The use of high-K dielectrics will allow a significant reduction of the equivalent oxide thickness of the gate dielectric itself. However, there are additional factors such as polysilicon-depletion effect (PDE) contributing to the total CET of gate dielectrics[1]. Replacing the polysilicon gate with a metal gate will essentially eliminate gate depletion and consequently reduce the CET by several angstroms. In addition, polysilicon gates are thermodynamically unstable on many high-K materials, such as Ta_2O_5 [2] and ZrO_2 [3], while many metals are expected to be stable on advanced gate dielectrics.

A major advantage of polysilicon gates is that by doping polysilicon with either acceptor or donor atoms one can change the work function of the gate electrode and thus achieve surface-channel bulk-Si p-MOSFET and n-MOSFET devices with the desirable threshold voltages. Since there is no well-established way to modify the work function of a metal, two different metals (one with a high work function of around 5 eV and the other with a low work function of around 4 eV) will likely be needed for future bulk CMOS devices. A straightforward way to implement a dual-work-function metal gate CMOS technology [4] is as follows. After blanket deposition, the first metal is removed from either the p-MOS or n-MOS regions, and then a second metal with a different work function is deposited. Unfortunately, this entails exposing the gate dielectric to the metal etchant, which causes undesirable thinning and potential dielectric reliability problems.

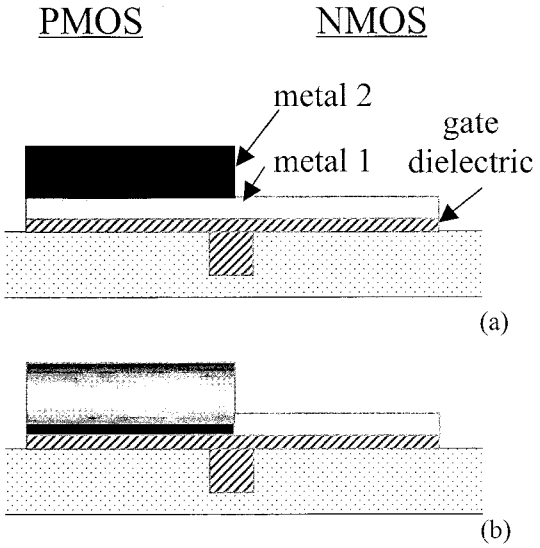

Fig. 1. Schematic illustration of the process flow. (a) CMOS structure after second metal has been removed from the n-MOS side. (b) CMOS structure after annealing shows that the metals on the p-MOS side have interdiffused, and second metal has segregated to the dielectric interface.

We propose an alternative approach in which dual work function gates can be fabricated without exposing the gate dielectric to the etchant. First, deposit a thin layer of one of the metals over the entire wafer. For the sake of discussion, let us assume this first metal is the one with the low work function. Then deposit the second (high work function) metal over the entire wafer (Fig. 1(a)). Next, selectively remove the high work function metal from the n-MOS regions while the p-MOS regions are protected by photoresist. Since the low work function metal is the only metal remaining on top of the n-MOS dielectric, it will clearly determine the n-MOSFET threshold voltage (V_T). The two remaining metals on the p-MOS side are subsequently allowed to interdiffuse. In some cases, the two metals will mix, yielding an intermediate gate work function. By choosing a suitable thickness combination for the metal layers, the composition of the mixture and thus the gate work function can be controlled. This approach would allow for a continuous tuning of transistor threshold voltages independent of substrate doping concentration. This can be especially important for ultra-thin body MOS transistors [5], where adjustment of the substrate doping is not an effective way of V_T-control. In other cases, one of which we

Manuscript received May 29, 2001; revised June 19, 2001. The work of I. Polishchuk was supported by a fellowship from NIST/SRC. The review of this letter was arranged by Editor C.-P. Chang.

I. Polishchuk, T.-J. King and C. Hu are with the Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720 USA (e-mail: pranade@eecs.berkeley.edu).

P. Ranade is with the Department of Materials Science and Engineering, University of California, Berkeley, CA 94720 USA (e-mail: igorp@eecs.berkeley.edu).

Publisher Item Identifier S 0741-3106(01)07739-4.

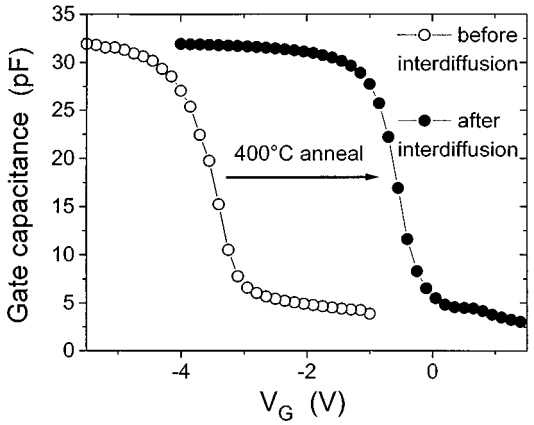

Fig. 2. Capacitance versus voltage characteristics of a fabricated MOS capacitor with Ti/Ni gate. ($t_{ox} = 35$ nm) A large (3 V) shift in the flat-band voltage is due in part to the change in the work function, and in part to the reduction in fixed charge.

explore in this letter, the top-layer metal may have a propensity to segregate at the dielectric interface (Fig. 1(b)). Consequently, this metal will solely determine the work function of the p-MOS gate electrode.

II. Device Fabrication and Characterization

To demonstrate the proposed metal interdiffusion gate (MIG) technology, we chose Ti as a low work function metal and Ni as a high work function metal. We first sputter-deposited an ultrathin (100 Å) layer of Ti on top of the SiO_2 gate dielectric followed by 200 Å of Ni. The sample was then annealed in forming gas $(N_2 + H_2)$ at 400 °C for 30 min. Due to the high diffusivity of Ni in Ti [5], this low thermal budget is sufficient to ensure that Ni diffuses through the Ti layer to the dielectric interface. The work function of this MIG electrode was measured both before and after anneal. These measured values were compared to the work functions of the Ti-gated and Ni-gated control samples.

A large shift in the flat-band voltage (V_{FB}) of a p-MOS capacitor with Ti/Ni MIG gate resulting from metal interdiffusion was observed (Fig. 2). The work functions of the metal gates can be determined by measuring and plotting V_{FB} as a function of oxide thickness [7]; the intercept of the plot gives the gate work function relative to the Si substrate's Fermi level (Fig. 3). Fig. 3 shows that before interdiffusion the work function of the MIG electrode corresponds to that of Ti-gate control sample, while its work function after the 400 °C anneal corresponds precisely to the Ni-gate control sample annealed under the same conditions. This observation indicates that, as the result of the 400 °C anneal, Ni has diffused to the SiO_2 interface and now determines the gate work function.

We further confirm the interdiffusion of titanium and nickel by X-ray photoelectron spectroscopy (XPS) analysis. The depth profile for the annealed Ti/Ni MIG sample [Fig. 4(a)] indicates that Ni, which originally was on top of the Ti layer, has diffused to the SiO_2 interface. The fact that Ni has segregated to the dielectric interface explains why the Ti/Ni gate electrode has a high work function after the anneal. The detailed photoelectron spectrum for Ni at the dielectric interface [Fig. 4(b)] shows that only elemental Ni is at the SiO_2 interface. The absence of nickel

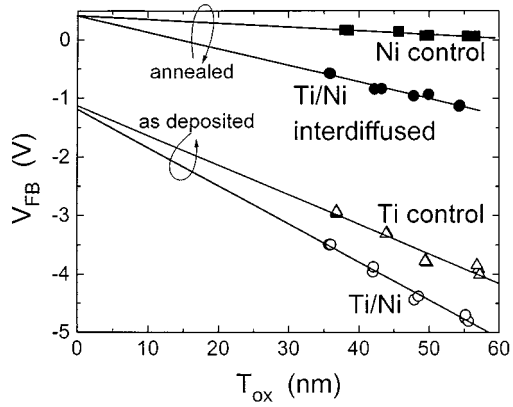

Fig. 3. Before annealing, the work function of the Ti/Ni gate is the same as that of the Ti-control gate; after annealing, it is the same as the work function of the Ni-control gate. As a result of Ni diffusing through Ti to the SiO_2 interface, the work function of the Ti/Ni gate changes by 1.6 eV.

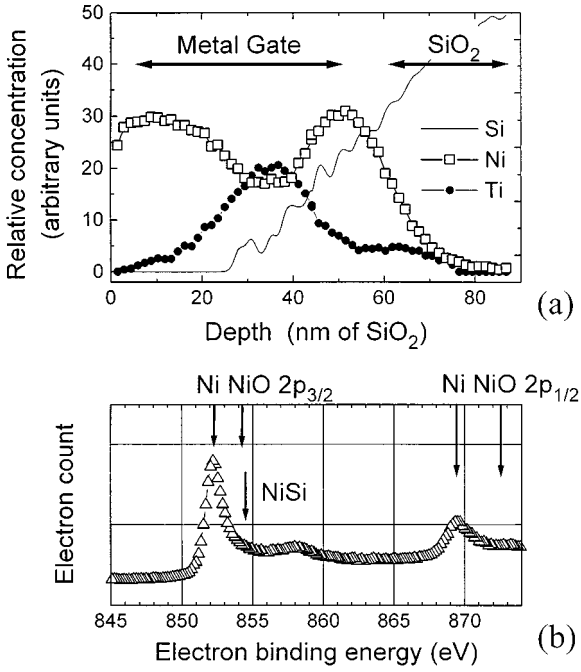

Fig. 4. (a) XPS depth profile for Ti/Ni gate electrode after the 400 °C, 30 min interdiffusion anneal. A large concentration of Ni is present at the SiO_2 interface, thus Ni determines the gate work function. (b) The photoelectron spectrum taken at the bottom of the MIG electrode shows that only elemental Ni is present at the dielectric interface. This indicates that Ni is thermally stable on SiO_2.

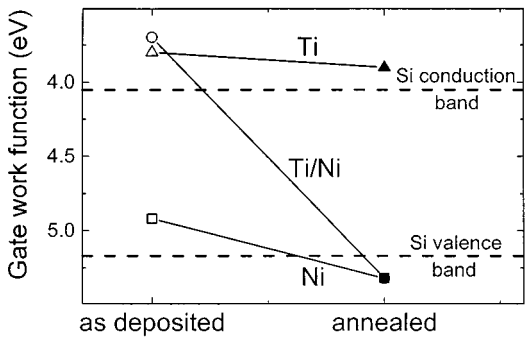

Fig. 5. Work function of Ti is 3.9 ± 0.08 eV and is appropriate for n-MOS gate application. The work function of the Ti/Ni gate after interdiffusion corresponds to that of Ni $(5.32 \pm 0.04$ eV) and is appropriate for p-MOS gate application.

oxide or nickel silicide indicates that Ni electrode is stable on SiO_2 for the process conditions used in this MIG technology.

III. Summary and Conclusion

We have demonstrated an advantageous dual work function metal gate fabrication process. This process relies on metal interdiffusion to achieve the desirable work functions for n-MOS and p-MOS gate electrodes, and thus the gate dielectric is always protected from etchants. The measured Ti work function is 3.9 eV and corresponds to the silicon conduction band (Fig. 5), therefore Ti is a good choice for the n-MOS gate electrode. Ni diffuses easily through Ti and segregates to the dielectric interface. Since Ni has a work function of 5.3 eV (corresponding closely to the silicon valence band) it can be used to make p-MOSFET's with a low threshold voltage. One should note that since Ti is not stable on SiO_2 at elevated temperatures, it cannot be used in a standard self-aligned SiO_2 CMOS process. Nevertheless, the proposed Ti-Ni combination can be used in a gate-last SiO_2 CMOS process [8] and potentially in a standard gate-first CMOS process with high-K gate dielectrics.

Acknowledgment

Devices were made in the Microfabrication Laboratory, University of California, Berkeley. The authors wish to thank T. Westmore from Accurel Systems for performing the XPS analysis.

References

[1] K. F. Schuegraf, C. C. King, and C. Hu, "Impact of polysilicon depletion in thin oxide MOS technology," in *Proc. Tech. Papers 1993 Int. Symp. VLSI Technology, Systems, and Applications*, 1993, pp. 86–90.

[2] H. F. Luan, B. Z. Wu, L. G. Kang, R. Vrtis, D. Roberts, and D. L. Kwong, "Ultra thin high quality Ta_2O_5 gate dielectric prepared by in-situ rapid thermal processing," in *IEDM Tech. Dig.*, 1998, pp. 609–612.

[3] C. H. Lee, H. F. Luan, W. P. Bai, S. J. Lee, T. S. Jeon, Y. Senzaki, D. Roberts, and D. L. Kwong, "MOS characteristics of ultra thin rapid thermal CVD ZrO_2 and Zr silicate gate dielectrics," in *IEDM Tech. Dig.*, 2000, pp. 27–30.

[4] Y. C. Yeo, Q. Lu, P. Ranade, H. Takeuchi, K. J. Yang, I. Polishchuk, T.-J. King, C. Hu, S. C. Song, H. F. Luan, and D.-L. Kwong, "Dual-metal gate CMOS technology with ultra-thin silicon nitride gate dielectric," *IEEE Electron Device Lett.*, vol. 22, pp. 227–229, May 2001.

[5] L. Chang, S. Tang, T.-J. King, J. Bokor, and C. Hu, "Gate length scaling and threshold voltage control of double-gate MOSFET's," in *IEDM Tech. Dig.*, 2000, pp. 719–722.

[6] G. B. Gibbs, D. Graham, and D. H. Tomlin, *Philos. Mag.*, vol. 8, p. 1269, 1963.

[7] E. H. Nicollian and J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*. New York: Wiley, 1982, p. 467.

[8] A. Yagishita, T. Saito, K. Nakajima, S. Inumiya, Y. Akasaka, Y. Ozawa, K. Hieda, Y. Tsunashima, K. Suguro, T. Arikado, and K. Okumura, "High performance damascene metal gate MOSFET's for 0.1 μm regime," *IEEE Trans. Electron Devices*, vol. 47, pp. 1028–1034, May 2000.