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How do carbon nanotubes fit into the semiconductor roadmap?

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ABSTRACT This paper presents an overview of the issues related to the integration of carbon nanotubes into microelectronics systems. Particular emphasis is placed on the use of carbon nanotubes as on-chip wiring (interconnects) and active devices (transistors), the two main building blocks of current semiconductor circuits. The properties of state-of-the art devices are compared in order to test the viability of replacing silicon-based components with carbon nanotubes. Further, the problems associated with the construction of nanotube-based devices are discussed.

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1 Introduction

A quick glance at the current version of the international technology roadmap for semiconductors (ITRS) [1] shows that the continued down-scaling of the features on semiconductor chips is expected to reach 15 nm by 2020. Already by 2010 the smallest wiring on a chip should be narrower than 50 nm. This means that the already high demands placed on state-of-the-art circuits with features of around 90–100 nm will increase considerably, creating a number of critical bottlenecks related to properties of the materials currently used. Thus, the search is on for new materials to relax these constraints, enabling downscaling to take place at the current level.

Several options have been considered to replace the tried-and-tested silicon at the centre of the devices. Other materials such as germanium and gallium arsenide have superior semiconducting properties, but are much more difficult to integrate due to several problems including the deposition of gate oxides and device etching. These problems increase the cost per device considerably with the result that silicon has remained on top, providing the standard to which all alternative technologies must be measured.

The manufacture of silicon based chips is based on a, so-called, "top down" approach whereby the materials used to make the devices are first deposited on the chip and then structured using optical lithography and etching. In this way a large number of layers can be built up to connect the transistors that are constructed from the topmost part of the single crystal silicon wafer. Since crystalline silicon cannot be grown on silicon dioxide or other dielectric materials, the transistors in a chip are restricted to the two-dimensional silicon substrate surface, and cannot be distributed within the interconnect wiring network. However, this limitation is not as significant as it would appear for silicon substrates because the transistor density is limited by the amount of heat that can be removed from the chip. It does restrict the choice of substrates to silicon for high performance chips. An alternative to the top down method is the use of self-organization in which large complex structures are constructed from smaller building blocks, e.g., molecules. This approach is referred to as "bottom up" and includes molecular self-assembly and the generation of extremely uniform crystalline structures such as nanowires and carbon nanotubes.

Carbon nanotubes (CNTs) were discovered by Iijima in 1991 while investigating the soot of an arc-discharge experiment used to create C_{60} buckyballs [2]. From transmission electron microscope (TEM) images of periodic structures in the soot he speculated that concentric, graphene-based tubes had formed in the discharge zone. The basic forms of single-walled and multi-walled CNTs are shown in Fig. 1 together with a planar graphene sheet. One year later Hamada et al. suggested that these tubes could be metallic or semiconducting from tight binding calculations [3]. In the same year Ebbesen and coworkers presented an optimization of the arc-discharge method that yielded large quantities of CNTs [4]. Despite this initial success, it took a further four years to pu-

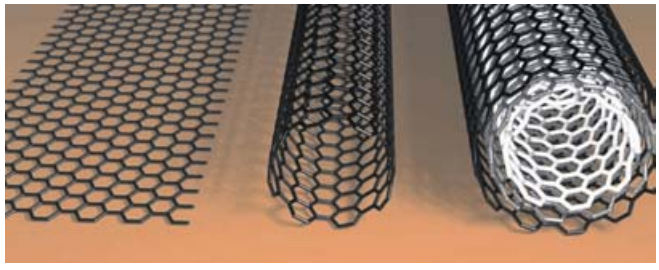

FIGURE 1 Illustration of the form of a graphene sheet (*left*), single-walled carbon nanotube (*middle*) and a multi-walled carbon nanotube with three shells (*right*)

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rify the arc-discharge material sufficiently to enable devices to be created, starting with the first measurement by Ebbesen et al. on the resistance of multi-walled carbon nanotubes [5]. Two years later the first transistor was made [6] and ballistic transport in multi-walled CNTs was established [7].

The creation of a complete, functioning microelectronic system using only self-assembly and other nanotechnology methods is an enormous task requiring many different components to work together. Several important building blocks in this process have already been demonstrated, for instance selective bonding using DNA [8], but the ability to produce complex structures reliably seems a long way off. In particular, for microelectronics, it is important to reproduce the same device millions of times over almost flawlessly. For this reason a number of groups, including ourselves, are focusing on the selective integration of specific bottom up components into traditional top down microelectronics process flows to create hybrid systems with superior properties. In our work we have concentrated on the parallel production of carbon nanotubes at selected locations for on-chip interconnect and transistor applications.

2 Electronic properties of carbon nanotubes

The basic structure of CNTs is shown in Fig. 1. A single wall of a CNT can be thought of as a rolled up graphene sheet in which the edges of the sheet are joined together to form a tube (single-walled CNT (SWCNT)). By changing the degree of twist in the roll up different helicities or chiralities can be created. Further, several tubes of different diameter can be fitted into each other, rather like a Russian doll, to make a multi-walled CNT (MWCNT) [2].

The properties of CNTs are strongly dependent on the chirality and the tube diameter, as discussed by McEuen [9]. For single-walled CNTs about one third of the possible tube conformations are metallic whereas the remaining two thirds are semiconducting. The band gap of semiconducting SWCNTs is inversely proportional to the diameter and corresponds to 0.8 eV for a tube with a diameter of 1 nm. Single-walled tubes with diameters up to 5 nm and as small as 0.4 nm have been observed, but the diameter is typically between 0.7 nm and 2 nm providing band gaps in a range that is interesting for transistor and diode applications. Multi-walled nanotubes with diameters up to 100 nm have been observed although their diameters are usually around 10–20 nm. The separation of the layers in a MWCNT is about the same as in graphite and corresponds to 0.34 nm.

The interesting properties of carbon nanotubes are a result of their quasi-one-dimensional shape and the sp_2 and π-bonding between the carbon atoms. The carbon bond in graphene is very strong, even stronger than the sp_3 bond in diamond, leading to high mechanical strength and excellent thermal transport characteristics. The π-electrons above and below the hexagonal graphene layer are free to move and form an electron band, producing the semi-metal electrical properties of graphite. However, for the nanotubes, the finite tube circumference restricts the number of allowed electron states. Hence, the semi-metal state of graphene is altered and a band gap may open up at the Fermi energy. Figure 2 shows how the band gap is influenced by the CNT diameter and chirality.

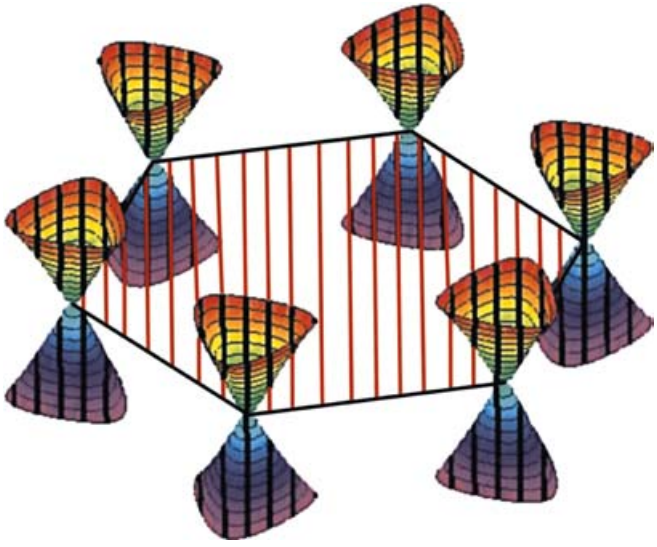

FIGURE 2 The first Brillouin zone of a nanotube showing how the periodicity around the circumference of a carbon nanotube influences its electrical properties. The *pyramidal cones* represent the electron energy dispersion of the nanotube surface close to the Fermi energy and the *parallel lines* show the periodicity around the circumference in reciprocal space. The spacing of the lines is inversely proportional to the CNT diameter and their angle depends on the nanotube chirality. For specific tube diameter and chirality the lines intersect with the apex of the cones and the nanotubes are metallic, i.e., there is an allowed state at the Fermi energy. If, as shown, the lines intersect elsewhere on the cones, there is a band gap around the Fermi energy and the tubes are semiconducting. For larger diameter CNTs the spacing between the lines is reduced and the maximum possible band gap decreases

The resistivity of a conducting material depends on the number of scatterers, number of carriers and the availability of states into which the electron or hole can be scattered. Hence, a further impact of the perfect structure of the CNTs and the limited number of states is their ability to transport electrical charge ballistically, i.e., without scattering, over distances of up to several micrometers depending on the quality of the tubes [10]. The downside is that it is more difficult to access these states due to their reduced number and specific configuration which leads to significant reflection at the contact-CNT interface. The number of transmitted electrons or holes depends on the number of states available; each conducting state can transport one spin up and one spin down electron (or hole) giving a quantum conduction $G_0 = 2e^2/h = 1/12.9\,\mathrm{k}\Omega$. Since each tube has two conduction states available at low bias voltage, the ideal resistance of a CNT is 6.45 kΩ. In this case the voltage drops across the contacts and not along the tube. This applies to conduction through both metallic and semiconducting CNTs. For MWCNTs, if all of the walls are directly connected to the contact material, the tubes conduct in parallel, and the resistance is reduced accordingly. Further, the ballistic transport and mechanical stability of the CNTs allow them to withstand high current densities up to $10^{10}\,\mathrm{A/cm^2}$, three to four orders of magnitude higher than most metals [11].

Other types of structures referred to as carbon nanotubes include “bamboo” tubes that resemble a stack of beakers and “lampshade” tubes that look the same except that the base of the beaker is missing. Both of these types of tubes are interesting for gas storage applications due to their high surface area, but are not relevant for microelectronic systems because

electronic conduction perpendicular to the graphene layers is much poorer than parallel to the layer. Some types of carbon fibres are also referred to as CNTs in the literature despite their very poor crystallinity. However, any degree of disorder helps to destroy the ballistic conduction, so these structures are also not suitable for microelectronic applications.

3 Producing carbon nanotubes

There are three main methods to produce carbon nanotubes; arc discharge, laser ablation and catalyst enhanced chemical vapour deposition (CCVD). Each of these techniques has its advantages and disadvantages, as discussed below.

Arc discharge and laser ablation rely on the evaporation of a graphite target to create gas-phase carbon fragments that recombine to form CNTs. The temperatures reached in these processes are in the range 2000–3000 °C, more than sufficient for the carbon atoms to rearrange into the tube structure. In order to increase the yield of nanotubes in the carbon material created, several different metals are incorporated into the target that are evaporated in concentrations of the order of 1%. The metals evaporate with the carbon and coalesce into clusters that form a base from which the nanotubes can grow.

Under optimum conditions both of these processes produce nanotubes with the highest crystallinity due to the high formation temperature. Unfortunately, a large amount of unwanted non-nanotube graphitic and amorphous carbon material is produced as well, and a cleaning process is necessary before the nanotubes can be used. Further, the purified nanotubes are dispersed in a solvent and are typically deposited in a random manner on the substrate by dipping, spraying or spin-on. This is useful for investigations of the physical properties of CNTs in individual "hand-crafted" devices, but is not suitable for the reproducible, parallel integration of CNTs into microelectronic systems. On the other hand, preparation of the nanotubes in solution enables the application of various processes to separate the semiconducting and metallic CNTs [12, 13] and chemically functionalize the CNTs [14].

Catalyst enhanced chemical vapour deposition utilizes small metal catalyst clusters in the gas phase or on surfaces to decompose a carbon containing feedstock gas, such as methane or acetylene. The resulting carbon dissolves in, or is adsorbed on, the catalyst particle and is released in the form of a nanotube starting with a bucky-ball type cap when the concentration exceeds the maximum solubility [15]. The nanotube continues to grow as long as carbon continues to be delivered at the right rate and the form of the catalyst does not change. The growth temperature depends on the type of nanotube to be grown and the catalyst composition and lies in the range from 400 °C to 1100 °C, lower than the temperatures in the arc discharge or laser ablation processes. For this reason it is believed that CCVD tubes have a higher density of defects.

The advantage of CCVD nanotube production is the possibility to structure the catalyst particles and, hence, selectively grow the nanotubes where they are required. Further, under the right conditions only nanotubes are produced and no unwanted graphitic material. Using this method we have produced 6″ wafers coated with a patterned layer of MWCNTs of uniform length and diameter in a quartz oven at 700 °C using acetylene as the carbon feedstock and a structured 5 nm thick iron layer [16].

4 Carbon nanotube interconnects

The ability of CNTs to carry high current densities with a fixed resistance over several micrometers makes them attractive for on-chip interconnect applications in microelectronics. As shown in Fig. 3, the current density that is anticipated in the interconnects is expected to increase dramatically to about 7 MA/cm^2 in the next 14 years when the wire width is below 20 nm [1]. Recent measurements on lateral copper wires down to 50 nm indicate that they can withstand such high current densities [17]. However, the most critical components are the vertical interconnects (vias) between the metal layers because they do not have the same near perfect structure of the wires. Higher contact resistances at the boundaries between the vias and the lower metal layer together with a narrowing of the vias at the base leads to an enhanced risk of local heating and electromigration. Current estimates [1] based on larger vias manufactured with current methods suggest a lower maximum current density of 2.5 MA/cm^2 for the vias which should be exceeded for vias with diameters below 50 nm. Carbon nanotubes can carry current densities of over ten times higher than those required by the ITRS roadmap for 2018 and are, therefore, an interesting alternative to the current copper wires.

The ITRS 2003 roadmap also sets a limit on the total via resistance of 20 Ω, independent of the diameter [1]. Figure 4 shows a calculation of the resistance of copper vias of different aspect ratios (AR: height to diameter ratio) based on the known surface and grain scattering (size effect) parameters [18]. The resistances increase almost linearly on the log-log plot and do not meet the ITRS requirement for diameters below 10 nm.

The resistance of CNT based wires depends on the number of shells that can be contacted in parallel since, at low biases, each shell has a fixed resistance of 6.45 kΩ. The lowest resistance can, therefore, be achieved using a bundle of metallic SWCNTs with the smallest possible diameter. The resistances of bundles of 0.7 nm and 1.4 nm metallic SWCNTs are also

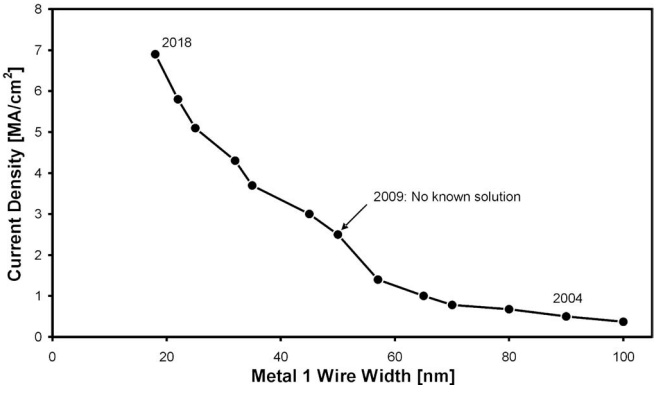

FIGURE 3 ITRS 2003 prediction of the current density increase in the lowest metal interconnect level (Metal 1) with decreasing interconnect width [1]. From 2009 (50 nm) onwards it is not known whether the current copper interconnects will be able to withstand the required current density of 2.5 MA/cm^2

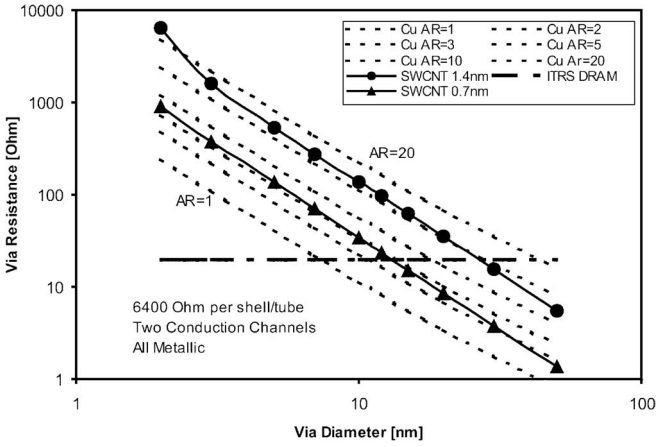

FIGURE 4 Calculated dependence of the via resistance on diameter and aspect ratio (AR). The *long dashed line* shows the ITRS 2003 requirement of 20 Ω per via, independent of the diameter. The *short dashed lines* indicate the anticipated resistance of copper vias taking into account surface and grain boundary scattering [18]. The *triangles* and *circles* show the resistances of vias filled with bundles of 0.7 nm and 1.4 nm diameter metallic SWCNTs, respectively. For ideal CNTs the aspect ratio of the via is not important because the voltage drops occur only at the contacts

shown in Fig. 4 for comparison with the copper vias. The resistances of the smallest diameter SWCNTs almost coincides with those of the copper vias with AR = 3 provided that they can be optimally contacted.

In order to test the properties of the CCVD CNTs, experiments were undertaken to disperse the CNTs in a solvent and deposit them on arrays of predefined electrodes for characterization. Dispersing the pristine MWCNTs directly in a solvent proved very difficult, and the CNTs had to be lightly oxidized in air or battered by ultrasonic agitation beforehand to make them acceptably soluble. Both of these methods introduce defects into the nanotube structure. Alternatively, surfactant based methods were also attempted, but in those cases it proved difficult to remove the unwanted surfactant after deposition. As a result, lightly oxidized CCVD MWCNTs were dispersed in dimethylformamide (DMF) and deposited on cobalt electrodes. In order to improve the contact, a structured layer of palladium was deposited on top using e-beam lithography (Fig. 5a).

Figure 5b shows the resistance of the MWCNTs as a function of their length between the contacts. Overall it can be seen that the resistance is higher for longer MWCNTs: Fitting the results delivers a resistance of about 40 kΩ/μm and a zero length extrapolation of almost zero, showing that the Pd contact is good. There is also a large amount of scatter, indicative of a statistical process, suggesting that the oxidation and dispersion preparation may have introduced defects into the CNT structure. Longer ultrasonic agitation, for instance, was found to increase the resistances, supporting this interpretation. As a result, we conclude that it is highly desirable to prepare the CNTs at the positions they are required to avoid any disruptive mechanical and chemical processing to place them on the surface.

At present no CCVD process has been presented for the structured creation of bundles of SWCNTs in vias. So, in order to demonstrate that CNTs can be selectively grown between two metal layers on a chip, we have chosen to use the well understood CCVD growth of MWCNTs from small iron clusters to selectively generate single CNT vias [19]. The process flow that we have used to generate CNT vias is shown in Fig. 6. A catalyst and support metal multilayer is deposited on the metal interconnect prior to deposition of the separating dielectric. A hole is then etched through the dielectric to stop in the catalyst metal multilayer (Fig. 6a). A catalyst particle is generated by annealing in a reducing atmosphere (Fig. 6b) from which the CNT can be grown using CCVD (Fig. 6c). The connection is completed by the structured deposition of a contact metal on top. The bottom contact is given by the catalyst particle and supporting metal layers which are automatically aligned. Thus, for the correct choice of catalyst and support metal, an optimum bottom contact is produced along with growth of the CNT.

An iron/tantalum catalyst and support multilayer was chosen because CNTs were found to grow well from Fe catalyst particles on Ta substrates [20]. For the first experiments the holes were produced using ion beam milling through a 150 nm thick silicon nitride coating over the multilayer. Subsequently the substrate was annealed in 2.5 Torr hydrogen in a quartz oven at 700 °C for 5 minutes prior to CNT growth at 700 °C in 2.5 Torr hydrogen and 5 Torr acetylene. Figure 7 shows an SEM image after the growth process demonstrating that CNTs of various lengths can be grown in almost every hole using this method [19]. We have also produced similar CNT filled vias using more conventional electron beam lithography and plasma dry etching to generate the holes [21].

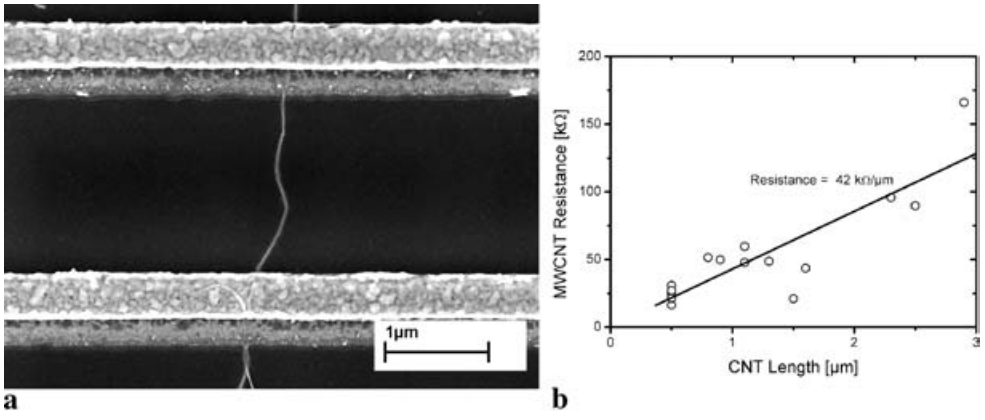

FIGURE 5 Length dependence of the resistance for dispersed and deposited MWCNTs contacted with palladium. In order to disperse the tubes, they were lightly oxidized in air. The resistance of longer MWCNTs is higher and indicates a resistance of about 42 kΩ/μm. This is probably due to the oxidation and dispersion process. The low zero-length resistance indicates that Pd forms a good contact to the CNTs

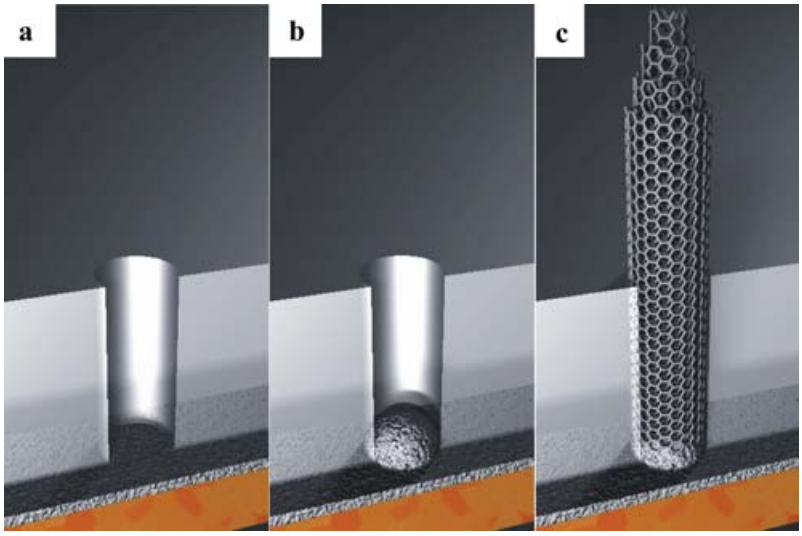

FIGURE 6 Production of a CNT via: (**a**) a hole is made in the dielectric above the metal layer to be contacted. (**b**) a catalyst particle is deposited or generated at the bottom of the via from which the CNT can be grown (**c**)

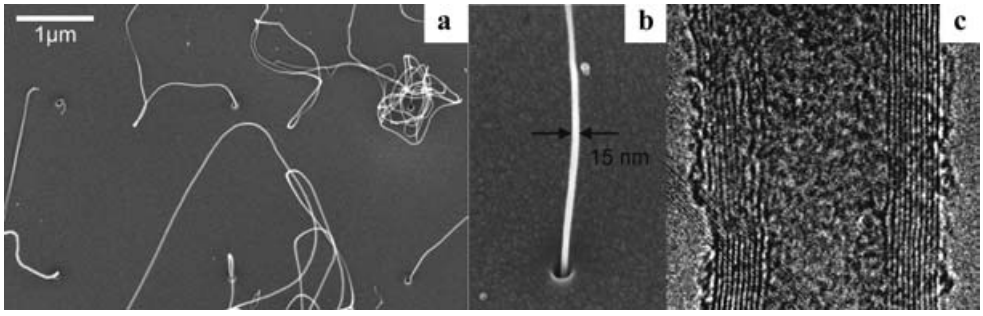

FIGURE 7 (**a**) Growth of an array of MWCNTs in 30 nm diameter vias from a buried Fe/Ta multilayer. The vias were defined using Ga^+ ion beam lithography. (**b**) Highlights one via hole in which a relatively straight 15 nm diameter MWCNT has been grown. (**c**) Shows a TEM image of a 12 nm diameter MWCNT grown under the same conditions

Tungsten contacts were selectively deposited using ion beam deposition in order to electrically characterize the CNT vias shown in Fig. 7. An image of the two contacts to one CNT via is shown in Fig. 8a. Using this method it is expected that the top electrode contacts only the outermost shell or wall of the MWNCNT, whereas the catalyst particle at the base of the via should contact all shells together. The two contacts to the top of the via and two to the substrate enabled a four-point measurement of the total via resistance including the contact resistances to the nanotube.

Figure 8b shows the results of the resistance measurements as a function of the annealing temperature; initially the via displays a poor resistance in excess of 1 MΩ, but on annealing to 850 °C this value drops sharply to under 8 kΩ. This decrease is attributed to an improvement in the bottom contact through the catalyst particle and a better attachment of

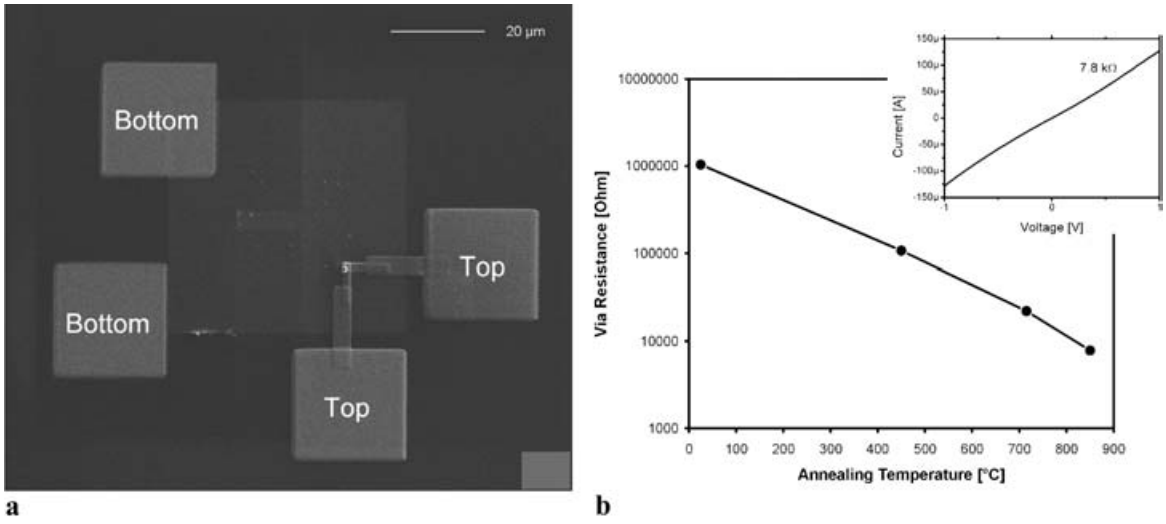

FIGURE 8 (**a**) SEM image of the tungsten top contacts to an individual CNT via grown from a buried catalyst layer. (**b**) The via resistance as a function of annealing temperature. The *inset* shows the nearly ohmic behaviour of the CNT up to currents in excess of 130 µA. This nanotube carried a current of 750 µA before breakdown ($J_{max} = 4.10^8$ A/cm^2)

the W top-contact to the MWCNT. More importantly, this 15 nm diameter MWCNT could transport currents of up to 750 μA before breakdown, corresponding to a current density of 4.10^8 A/cm^2, well above the ITRS 2003 requirements.

Similar values have been obtained for CNT vias made using e-beam lithography and standard dry etching processes [21]. In this case it is more difficult to etch through the top barrier layer to reach the catalyst and the contacts may be slightly oxidized in the process. However, this process more closely matches the process flow of a production facility and is, therefore, preferred. The resistances of about 8 kΩ for the MWCNT vias are good considering that only the outer shell of the MWCNT has been contacted and, hence, a minimum resistance of 6.45 kΩ can be expected. For the current case of a 10 wall nanotube, this resistance could be reduced to about 645 Ω by etching the end of the MWCNT to expose all shells for contacting. This value is still higher than the ITRS requirement so, for a competitive device many more shells, or a bundle of thin metallic SWCNTs is necessary.

5 Carbon nanotube transistors

Since the first carbon nanotube transistor was demonstrated [6] there has been a steady improvement of the device properties. Critical aspects for the application of CNT field-effect transistors (CNTFETs) can be derived from the ITRS roadmap [1] and include the ability to create normally-on and normally-off *p*-type and *n*-type devices with sufficiently high on-currents, low off-currents and subthreshold slopes approaching the room temperature limit of 60 mV/dec. As an example, Fig. 9 shows the expected development of the maximum current through the smallest transistor as the devices are scaled down. The width of the smallest transistor is given by the half-pitch size. As can be seen, the current does not scale with the device size, indicating that the current density in the device will increase. Further, the effective gate oxide thickness must be scaled along with the transistor dimensions, necessitating the introduction of high dielectric constant materials that may not form good interface layers with the silicon channel.

Devices based on semiconducting single-walled CNTs should perform better than existing silicon transistors due to the ballistic transport in SWCNTs [22]. In theory, the transport in a semiconducting SWCNT should match that in metallic tubes because each SWCNT has two conduction or valence states and each can support both spin up and down electrons. In this way the on-resistance of a CNTFET can be as low as 6.45 kΩ (values as low as 10 kΩ have already been achieved [22]) and the conduction can reach 155 μS (up to 220 000 μS/μm) at low drain-source bias voltages. Above about 160 mV the drain-source current is expected to saturate due to excitation of the optical phonon modes of the CNTs, reaching a maximum at about 25 μA, as for the metallic nanotubes, which is equal to 35.7 mA/μm [11].

In addition, due to the absence of dangling bonds on the CNT surface, almost any gate oxide material can be used, including those with high dielectric constants [23]. Hence, the interface should not strongly influence the transistor properties. Further, the use of metal source, drain and gate electrodes significantly reduces the series resistance of the contacts to the CNTs compared to the higher resistivity doped Si and silicide contacts used for Si channel transistors.

Most of the CNTFETs reported to date were made by contacting individual SWCNTs that had been dispersed and deposited from solution. This method is not suitable for the production of many CNTFETS and the dispersion process may influence the properties of the nanotubes. For this reason, we have adopted the method first presented by Dai [24] involving the CCVD growth of SWCNTs between structured electrodes. In this way the nanotubes do not have to be chemically modified and the nanotubes are only grown where they are required. The large number of devices that can be simultaneously produced with this method have shown that about 2/3 of the SWCNTs are semiconducting and the remaining 1/3 are metallic or have a small band gap [25, 26].

For our first devices the source and drain contacts were subsequently improved by electroless palladium or nickel deposition or e-beam lithography defined metal layers and gated using the silicon substrate coated with a 200 nm thick thermal silicon oxide dielectric [26, 27]. More recently, we have

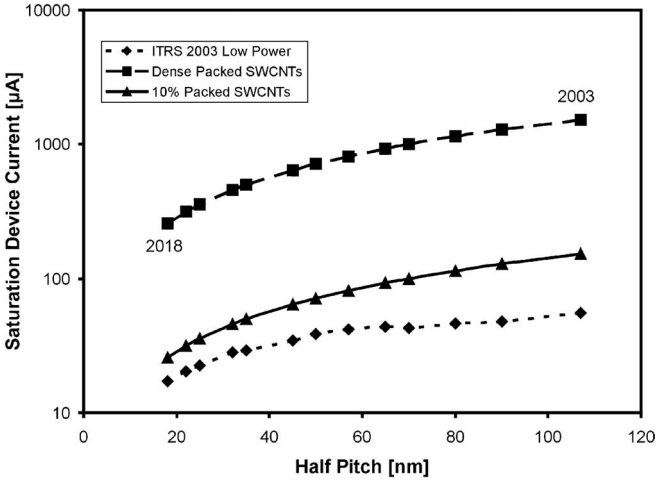

FIGURE 9 ITRS 2003 prediction of the saturation device current in the narrowest low power transistors up to 2018 (*diamonds*). The gate length is approximately half of the half pitch width which corresponds to the smallest device width. The saturation current of dense (*squares*) and 10% filled (*triangles*) flat, aligned arrays of 0.7 nm diameter semiconducting SWCNTs are shown for comparison

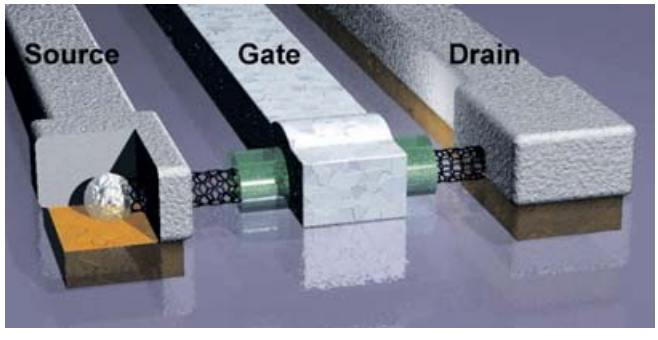

FIGURE 10 Schematic presentation of a top-gate SWCNT transistor. The SWCNT is grown from the catalyst particle on the left-hand electrode over to the right-hand electrode and both are encapsulated in an electroless metal plating process (Pd). The nanotube is coated with a gate dielectric (Ta_xO_y) and a metal gate (Al) is defined on top

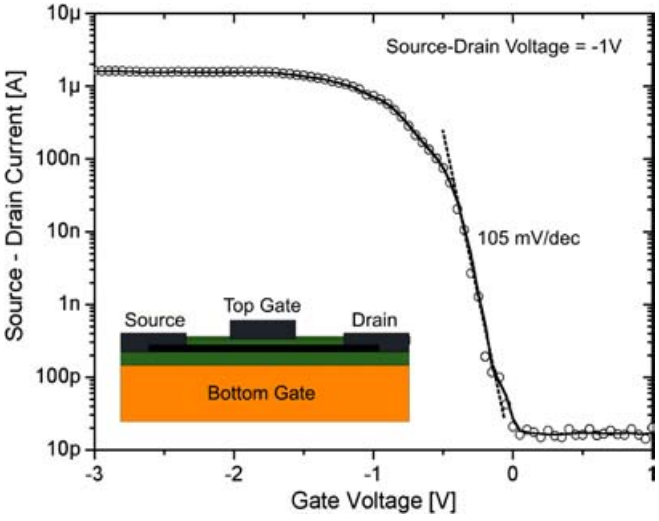

FIGURE 11 Gate voltage dependence of the source-drain current of a top-gate *p*-type CNT transistor. The CNT diameter is 0.7 nm, the source drain voltage 1 V, the Ta_xO_y gate oxide thickness approximately 8 nm, the source-drain separation about 2 μm and the gate length 600 nm. The source and drain contacts are Pd and the gate is Al. The off current minimum of about 15 pA is limited by the measurement apparatus. This device is normally off and exhibits a subthreshold slope of 105 mV/dec and a saturation on-current of 1.6 μA

added a thin Ta_xO_y dielectric coating and Al top-gate for improved performance. A schematic of these devices is shown in Fig. 10. Figure 11 presents the source-drain current dependence on the gate voltage of one of these devices. The as-grown SWCNTs are intrinsically *p*-type, as shown by the gate dependence and are normally off for the particular choice of contact and gate metals.

In order to understand the functioning of the *p*-type top gate CNTFET in Fig. 11 and the devices from other groups presented in the literature it is useful to consider the electrostatics governing their function. Several useful theoretical descriptions of the transistor properties for various geometries have been presented by Guo et al. [28–30] and Castro et al. [31]. A simple model showing the basics is presented in Fig. 12 in which a *p*-type semiconducting SWCNT with a band gap of 1 eV lies between source and drain contacts made of the same metal and is controlled by a gate made from a different metal.

The relative energies of the different components making up the CNTFET are determined by their respective work functions (WF). The work function of SWCNTs has been considered by Zhao et al. who calculated the energy of the highest occupied molecular orbitals (HOMO or valence band) of various small diameter tubes [32]. The present case of a 0.7 nm diameter semiconducting SWCNT corresponds most closely with the (10,0) tube for which a calculation has been made. This tube has a HOMO level of -5.2 eV. In this simplified case the CNT is considered to be undoped so that the Fermi energy is then at -4.7 eV and the lowest unoccupied molecular orbital (LUMO or conduction band) at -4.2 eV. The Fermi energy is constant over the device which means that in the absence of the gate the Fermi energy of the nanotube is the same as that for the Pd contacts (WF of -5.2 eV [33]) and the HOMO in the middle of the nanotube resides 0.5 eV lower, as shown in Fig. 12a. To compensate, the bands of the SWCNT bend by 0.5 eV near the contacts. In this case the WF of the metal (Pd) has been chosen to match the HOMO level of the SWCNT and the contact is assumed to be perfect so that there is no mismatch at the contact which would lead to a Schottky barrier for hole conduction [22].

Applying the Al top gate with a WF of -4.2 eV [33] shifts the SWCNT LUMO and HOMO down by a further 0.5 eV due to the -0.5 eV difference between the WFs , as indicated in Fig. 12b. Thus, even when a negative drain voltage of $V_{DS} = -1$ V is applied at zero gate voltage $V_{GS} = 0$

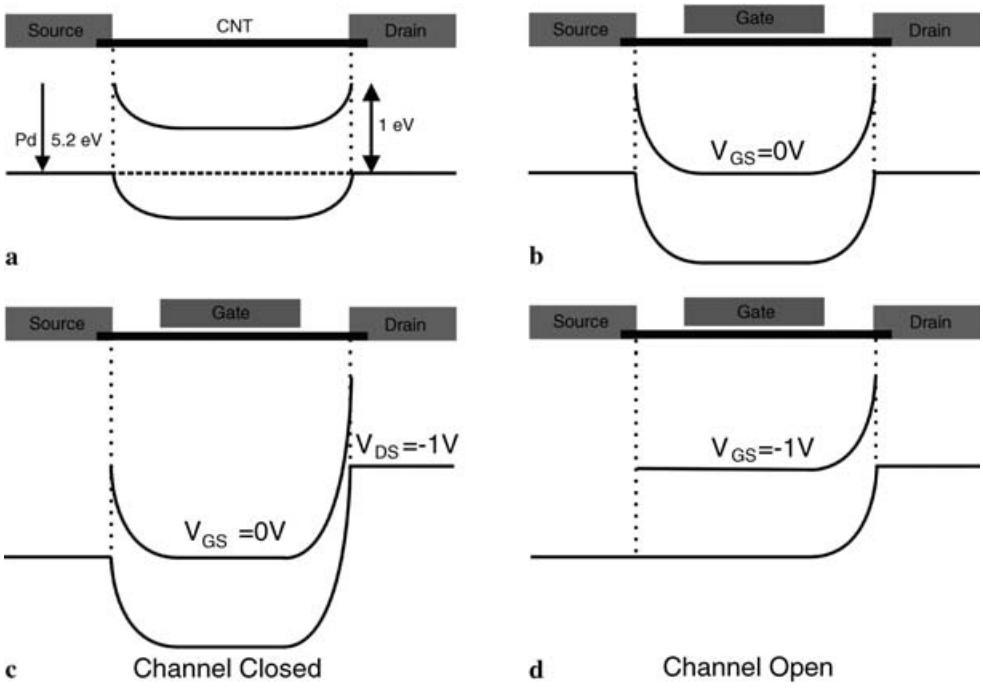

FIGURE 12 Simplified band diagram showing the function of a top gate *p*-type normally off CNTFET with a band gap of about 1 eV (0.7 nm diameter). The *top and bottom lines* represent the conduction and valence bands, respectively. (**a**) The source and drain metal work function (WF) is chosen to match the CNT WF to minimize the Schottky barriers at the contacts. (**b**) Shows the influence of the lower WF of the Al top gate and (**c**) the effect of applying a bias between the source and drain. (**d**) For a gate voltage $V_{GS} = -1$ V the channel is open and the holes can pass freely from source to drain. Increasing V_{GS} to 0 V closes the channel and current ceases to flow

(Fig. 12c) the holes still face a potential barrier of −1 V and no current flows, i.e., the transistor is normally off. Setting a negative gate voltage $V_{GS} = -1$ V removes this barrier and holes can move freely from source to drain via the LUMO and the transistor is on. Hence the properties of the CNTFET presented in Fig. 11 can be explained by bulk modulation of the SWCNT. Other effects, such as Schottky barriers, are relatively unimportant. The relatively low on current of 1.6 μA in our measurement can be explained by the 2 μm separation of the source and drain contacts, which is much larger than the 300 nm mean-free-path of the holes in the SWCNT [22]. In this case higher currents can be transported at higher drain-source bias.

Using this basic model, it is possible to consider the effect of changing the various metals contacting the SWCNT and hence control the CNTFET characteristics. For instance, changing the gate metal WF from −4.2 eV (Al) to −5.2 eV (Pd or Ni) is expected to raise the SWCNT LUMO level by +1 eV, converting the normally-off transistor into a normally-on transistor. The transistor is then off for a gate voltage $V_{GS} = +1$ V. To access the LUMO conduction band to create an *n*-type CNTFET requires the source and drain metal work functions to be changed to correspond to the higher energy, in this case −4.2 eV. Suitable metals are then Al with a WF of −4.2 eV [33] and Ta with −4.25 eV [33] with a small Schottky barrier, as discussed by Javey et al. [34]. A normally-on transistor is then possible using the same metal for the gate as used for the source and drain contacts. A normally-off transistor can be achieved by raising the gate WF above that of Al, e.g., Pd. Hence with a structured use of Al and Pd contacts all of the building blocks for a CMOS technology are available [34].

Larger deviations of the contact metal WFs from the LUMO and HOMO levels of the SWCNTs being used can lead to substantial Schottky barriers, as studied in detail by Wind et al. [35]. They used Ti and Co to contact *p*-type SWCNTs and used a segmented gate structure to control the resulting Schottky barrier (SB) transistors. The disadvantage with this approach is that the on-current is significantly reduced because all of the electrons or holes must tunnel through a barrier, reducing the transmission probability. Thus, the CNTFETs showing the highest on-currents are not SB transistors.

A further characteristic of this and other CNTFET designs is ambipolar behaviour at high drain-source biases. As can be seen in Fig. 12d, there is a short barrier for electrons to tunnel from the drain contact into the CNT LUMO that will become narrower as the drain voltage becomes more negative. This tunnelling can lead to a significant device current even though the transistor should block transport, i.e., there is a high off-current. The severity of this effect is related to the device geometry which determines how narrow the barrier is under particular bias conditions.

In addition, it is important to note that the considerations discussed above apply to SWCNTs with a band gap of 1 eV. As shown by Zhao et al. [32], the energies of the HOMO and LUMO are diameter dependent, implying that the contact metal WF has to be adjusted to the SWCNT diameter, and that the diameters must fall in a narrow distribution to avoid excessive SB variations over the many devices making up the microelectronic circuit.

A number of *p*-type CNTFET devices with various geometries have been reported in the literature. A selection of the CNTFETs with the best characteristics is compared with their silicon based counterparts in Table 1. In this comparison the device width is used to derive the standardized device parameters. It can be seen that the drive current (on current) of the *p*-CNTFETs is between 3 and 20 times larger than for the Si transistors. This is also mirrored in the transconductance values. The subthreshold slopes of the CNTFETs are somewhat worse than for the Si transistors, but this is related to the thicker gate oxides (except for the first one). Thus, it would appear that CNTFETs have superior properties to current state-of-the-art Si transistors.

Quite recently a very short channel (10 nm) CNT device was reported which was able to carry even more current that the limit allowed by the generation of optical phonons [36]. These results show that the mean-free path for phonon creation can be undercut to obtain ballistic transport at higher biases and allow more current to flow. The maximum value indicated was 70 μA for a 1.5 nm SWCNT. The other device parameters, such as subthreshold slope were not reported,

	CNT FET McEuen (2002)	CNT FET Seidel (2003)	CNT FET Javey (2003)	CNT FET Javey (2004)	CNT FET Seidel (2004)	TriGate Doyle (2003)	FinFET Yu (2002)	SON Harrison (2003)
Reference	37	39	23	39	This work	40	41	42
Channel Material	CNT	CNT	CNT	CNT	CNT	Si	Si	Si
Drive Voltage [V]	1.0	1.0	0.6	0.4	1.0	1.3	1.2	0.9
Drive Current [mA/μm]	2.96	4–20	14	11.6	2.4–6.4	0.88	0.72	0.914
Transconductance [μS/μm]	6666	260	3070	17 650	2640–6430	920	900	1170
Subthreshold Slope [mV/dec]	80	700–1100	150–170	110	105	69.5	101	70
On Resistance [Ω/μm]	473	50–250	43	22	155–425	1480	1667	985
Gate Length [nm]	1400	150–2000	300	50	600	60	10	70
Gate Oxide Thickness [nm]	1	200	67	8	8∗	1.5	1.7	2
Off Current [nA/μm]	N/A	1.0	1.0	600	22∗∗	120	20	1

∗ Estimated

∗∗ Limited by the measurement range of the parameter analyzer

TABLE 1 The characteristics of state-of-the-art *p*-type carbon nanotube and silicon transistors. The values have been scaled to the channel width, i.e., the Si fin width or the CNT diameter, for comparison of the different device designs

so a comparison with the other devices in Table 1 is not possible.

In addition to the problem of growing purely semiconducting SWCNTs of a certain diameter (which has not been achieved to date), many SWCNTs must be connected in parallel in order to reach the device sizes and currents predicted by the roadmap (Fig. 9). Fortunately, the comparison between 100% full and 10% full flat arrays of SWCNTs and the ITRS requirements shown in Fig. 9 indicates that only about 5% filling is required to meet the targets, i.e., for a 0.7 nm diameter SWCNT, the spacing between the tubes must be less than 14 nm. Further, the SWCNTs can be stacked vertically between gate electrode layers, increasing the on-current of the transistor. This lower density provides some flexibility for the methods leading to directed growth, for example in a gas flow [43] or electric field [44].

Since no technique has been developed to grow only semiconducting CNTs, the metallic tubes must be removed after growth. At present the only reliable method to eliminate the metallic tubes is the application of burn pulses, as described by Collins et al. [45]. While this is unsuitable for the control of complete microelectronic circuits in which the CNTFETs are networked together, we have successfully used it to create multiple SWCNT FET devices capable of switching several milliamperes, sufficient to power LEDs and small motors [46]. A schematic of such a high current device is shown in Fig. 13. It consists of a metallic back gate layer covered with a thin high dielectric constant layer on which a sparse layer of small diameter SWCNTs was grown. The palladium source and drain regions were defined on the SWCNT layer using electron beam lithography, metal deposition and lift-off.

As shown in Fig. 14, these transistors initially display an on/off ratio of about three due to the parallel connection of metallic and small band gap SWCNTs together with the semiconducting nanotubes. As progressively higher burn pulses are applied at high positive gate voltage first the metallic and then the small band gap SWCNTs are eliminated. The semiconducting tubes are unaffected since they are switched off by the positive gate voltage. Using this method on/off current ratios of over 100 could be achieved albeit at the expense of a high on-current [46]. Despite the relatively modest performance of this transistor, it demonstrates that high current devices can be created by the parallel connection of many SWCNTs. Further, this approach is applicable for CNTs deposited from solution, enabling the nanotubes to be treated beforehand, for instance to eliminate the metallic tubes in advance [12, 13] or to chemically functionalize them [14] for sensor applications.

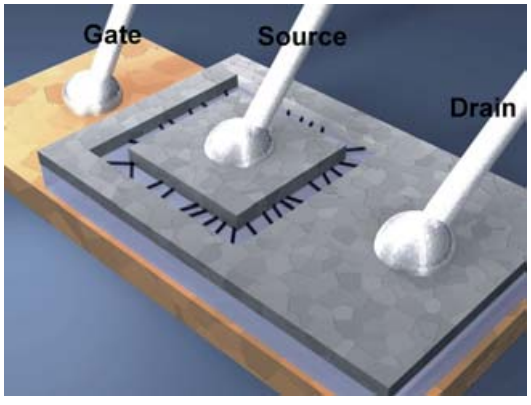

FIGURE 13 Schematic representation of a high current CNTFET made from a large number of parallel contacted SWCNTs. The transistor is controlled using a metal back gate and a separating high dielectric constant layer

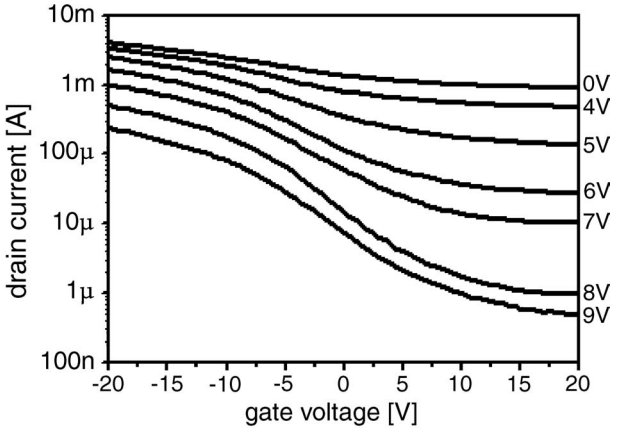

FIGURE 14 Burn pulse curves for a multiple SWCNT transistor with TaN back gate, a 53 nm thick Al_2O_3 gate dielectric layer and Pd source and drain contacts. The SWCNTs were grown using a thin nickel catalyst layer. The metallic and some of the small band gap nanotubes were burnt through at a positive gate voltage of 20 V at the voltages shown

6 Future devices

Combining the CNT via and lateral CNTFET results leads naturally to the idea of a vertical nanotube transistor [47]. Such a device is shown schematically in Fig. 15 in which a metal gate layer is inserted into the dielectric of a CNT via and a semiconducting SWCNT is used instead of a metallic MWCNT. There are two ways to obtain V-CNTFETS: (a) Deposit the bottom and top dielectrics and the gate metal layer on top of the source contact, etch through all three layers to the source, deposit the gate dielectric and

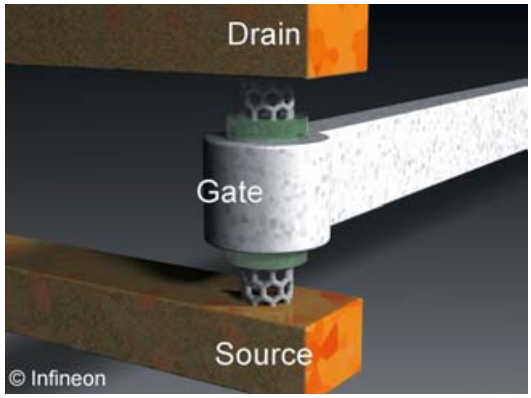

FIGURE 15 Vertical carbon nanotube field-effect transistor (V-CNTFET) concept. The SWCNT is either grown from a bottom source contact in a hole defined through separating dielectric layers and a ring gate, or the dielectric and gate are built on the nanotube after growth. A top drain contact completes the device. The advantages of these devices include the self-adjusted alignment of the nanotube and gate, optimum gate control and the minimal footprint required

grow the SWCNT, or (b) grow vertically aligned SWCNTs and deposit the spacer dielectric and gate metal layers on top. In both cases the transistor is completed by the structured deposition of a drain contact. These devices have several advantages over lateral transistors including self-alignment of the different components, small footprint, optimum control via the ring gate geometry and precise control of the separations via the thicknesses of the various layers. One difficulty with the production of V-CNTFETs is the generation of the narrow holes of about the SWCNT diameter (several nanometres) through several layers. One possible solution to this problem is to use block copolymer structuring [48] or anodized aluminium oxide [49] pores. Both of these materials form uniform, self-organized arrays of nanometre sized holes with diameters and densities that can be controlled by the process parameters.

7 Conclusions

Several different applications of carbon nanotubes in microelectronics have been presented and their relative merits discussed. The experimental results to date indicate that CNTs may be able to satisfy some of the ITRS conditions for devices and interconnects when their dimensions become very small. However, a number of processes need to be brought under control before a technology platform can be developed. These processes and possible solutions include:

- Growth of exclusively metallic or semiconducting single-walled carbon nanotubes. For transistors the number of small band gap tubes must be strongly suppressed to avoid compromising the device characteristics, whereas they are not a problem for interconnect applications. Since the density of semiconducting tubes must not be 100% to achieve acceptable device characteristics, the metallic tubes could be eliminated after growth by targeted chemical etching. Alternatively, if a growth rate difference (selective growth) can be engineered, then the conditions can be adjusted so that only the semiconducting tubes are long enough to bridge the gap between the source and drain contacts. The CNT properties could also be controlled by doping to create purely metallic or semiconducting nanotubes.
- For interconnect applications it is necessary to produce bundles of mostly metallic, small diameter single or double-walled carbon nanotubes in order to reach the same resistances predicted for ideal short copper vias and wires. In this case, the introduction of CNTs is restricted by their quantum resistance and not by their ability to withstand high current densities.
- The band gap, and therefore the CNT diameter, distribution of semiconducting SWCNTs should be narrow in order to produce devices with almost equivalent characteristics.
- For single CNT devices, the catalyst or deposition method must be so engineered that every position is filled to avoid breaks in the circuit. For multiple CNT devices the absence of a small fraction of the nanotubes may be acceptable.
- The CNT preparation must be compatible with the processes used to produce the other components in a hybrid system. For example, high growth temperatures may not be acceptable for the contacting of small silicon based devices in which the doping profiles are critical or lead to melting of the metals used to facilitate the contacts. In this case the lowest growth temperatures of less than 600 °C may not be a problem.
- The growth direction or placement of the CNTs should be adjustable to fit the requirements of the devices to be generated. This could be achieved by growth in predefined template arrays to separate the nanotubes in, for instance, a multiple SWCNT based transistor.
- Control over the length of the CNTs is necessary to accurately define the components. This could be achieved by etching after growth or self-limiting growth processes.

Considering the present rapid rate of development of carbon nanotube processes, it is anticipated that solutions to some of these factors will be developed in the not too distant future. In addition, novel device designs may be discovered that bypass the critical aspects of the existing methods and generate useful products.

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REFERENCES

1 International Technology Roadmap for Semiconductors 2003, http://public.itrs.net
2 S. Iijima: Nature **354**, 56 (1991)
3 N. Hamada, S. Sawada, A. Oshiyama: Phys. Rev. Lett. **68**, 1579 (1992)
4 T.W. Ebbesen, P.M. Ajayan: Nature **358**, 220 (1992)
5 T.W. Ebbesen, H.J. Lezec, H. Hiura, J.W. Bennett, H.F. Ghaemi, T. Thio: Nature **382**, 54 (1996)
6 S.J. Tans, A.R.M. Verschueren, C. Dekker: Nature **393**, 49 (1998)
7 S. Frank, P. Poncharal, Z.L. Wang, W.A. de Heer: Science **280**, 1744 (1998)
8 K. Keren, R.S. Berman, E. Buchstab, U. Sivan, E. Braun: Science **302**, 1380 (2003)
9 P.L. McEuen: Phys. World **13**, 31 (2000)
10 J. Park, S. Rosenblatt, Y. Yaish, V. Sazonova, H. Üstunel, S. Braig, T.A. Arias, P.W. Brouwer, P.L. McEuen: Nano Lett. **4**, 517 (2004)
11 Z. Yao, C.L. Kane, C. Dekker: Phys. Rev. Lett. **84**, 2941 (2000)
12 M. Zheng, A. Jagota, E.D. Semke, B.A. Diner, R.S. McLean, S.R. Lustig, R.E. Richardson, N.G. Tassi: Nature Mater. **2**, 338 (2003)
13 R. Krupke, F. Hennrich, H.B. Weber, M.M. Kappes, H. v.Löhneysen: Nano Lett. **3**, 1019 (2003)
14 S.B. Sinnott: J. Nanosci. Nanotech. **2**, 113 (2002)
15 R. Seidel, G.S. Duesberg, E. Unger, A.P. Graham, M. Liebau, F. Kreupl: J. Phys. Chem. B **108**, 1888 (2004)
16 G.S. Duesberg, A.P. Graham, F. Kreupl, M. Liebau, R. Seidel, E. Under, W. Hönlein: Diamond Rel. Mater. **13**, 354 (2004)
17 G. Steinlesberger, A. von Glasow, M. Engelhardt, G. Schindler, W. Hönlein, M. Holz, E. Bertagnolli: In Proceedings of the IEEE International Interconnect Technology Conference (IITC) (2002) p. 265
18 W. Steinhögl, G. Schindler, G. Steinlesberger, M. Engelhardt: Phys. Rev. B. **66**, 075 414 (2002)
19 A.P. Graham, G.S. Duesberg, F. Kreupl, R. Seidel, M. Liebau, E. Unger, W. Hönlein: In Proceedings of the XVII International Winterschool on the Electronic Properties of Novel Materials; H. Kuzmany, J. Fink, M. Mehring, S. Roth (Eds.), AIP Conference Proceedings **685**, 587 (2003)
20 F. Kreupl, A.P. Graham, W. Hönlein: Solid State Technol. **45**, 9 (2002)
21 M. Liebau, A.P. Graham, Z. Gabric, R. Seidel, E. Unger, G.S. Duesberg, F. Kreupl: AIP Conf. Proc. **723**(1), 536 (2004)

22 A. Javey, J. Guo, Q. Wang, M. Lundstrom, H. Dai: Nature **424**, 654 (2003)
23 A. Javey, H. Kim, M. Brink, Q. Wang, A. Ural, J. Guo, P. McIntyre, P. McEuan, M. Lundstrom, H. Dai: Nature Mater. **1**, 241 (2002)
24 A. Javey, Q. Wang, A. Ural, Y. Li, H. Dai: Nano Lett. **2**, 929 (2002)
25 W. Kim, H.C. Choi, M. Shim, Y. Li, D. Wang, H. Dai: Nano Lett. **2**, 703 (2002)
26 R.V. Seidel, A.P. Graham, B. Rajasekharan, E. Unger, M. Liebau, G.S. Duesberg, F. Kreupl, W. Hönlein: J. Appl. Phys. **96**, 6694 (2004)
27 R. Seidel, M. Liebau, E. Unger, A.P. Graham, G.S. Duesberg, F. Kreupl, W. Hönlein, W. Pompe: In Proceedings of the XVII International Winterschool on the Electronic Properties of Novel Materials; H. Kuzmany, J. Fink, M. Mehring, S. Roth (Eds.), AIP Conference Proceedings **685**, 95 (2003)
28 J. Guo, M. Lundstrom, S. Datta: Appl. Phys. Lett. **80**, 3192 (2002)
29 J. Guo, S. Goasguen, M. Lundstrom, S. Datta: Appl. Phys. Lett. **81**, 1486 (2002)
30 J. Guo, J. Wang, E. Polizzi, S. Datta, M. Lundstrom: IEEE Trans. Nanotechnol. **2**, 329 (2003)
31 L.C. Castro, D.L. John, D.L. Pulfrey: Proc. SPIE; J.C. Chiao, A.J. Hariz, D.N. Jamieson, G. Parish, V.K. Varadan (Eds.) **5276**, 1 (2004)
32 J. Zhao, J. Han, J.P. Lu: Phys. Rev. B **65**, 193401 (2002)
33 *Handbook of Chemistry and Physics*, 84th edn. (Chemical Rubber Company Press, Boca Raton 2004)
34 A. Javey, Q. Wang, W. Kim, H. Dai: IEDM Tech. Dig. 741 (2003)
35 S.J. Wind, M. Radosavljevic, J. Appenzeller, P. Avouris: J. Vac. Sci. Technol., B **21**, 2856 (2003)
36 A. Javey, J. Guo, M. Paulsson, Q. Wang, D. Mann, M. Lundstrom, H. Dai: Phys. Rev. Lett. **92**, 106804 (2004)
37 S. Rosenblatt, Y. Yaish, J. Park, J. Gore, V. Sazonova, P.L. McEuen: Nano Lett. **2**, 869 (2002)
38 R. Seidel, M. Liebau, G.S. Duesberg, F. Kreupl, E. Unger, A.P. Graham, W. Hoenlein, W. Pompe: Nano Lett. **3**, 965 (2003)
39 A. Javey, J. Guo, D.B. Farmer, Q. Wang, E. Yenilmez, R.G. Gordon, M. Lundstrom, H. Dai: Nano Lett. **4**, 1319 (2004)
40 B. Doyle, B. Boyanov, S. Datta, M. Doczy, S. Hareland, B. Jin, J. Kavalieros, T. Linton, R. Rios, R. Chau: Symposium on VLSI Technology Digest of Technical Papers (2003)
41 B. Yu, L. Chang, S. Ahmed, H. Wang, S. Bell, C.-Y. Yang, C. Tabery, C. Ho, Q. Xiang, T.-J. King, J. Boker, C. Hu, M.-R. Lin, D. Kyser: IEDM Tech. Dig. 251 (2002)
42 S. Harrison, P. Coronel, F. Leverd, R. Cerutti, R. Palla, D. Delille, S. Borel, S. Jullian, R. Pantel, S. Descombes, D. Dutartre, Y. Morand, M.P. Samson, D. Lenoble, A. Talbot, A. Villaret, S. Monfray, P. Mazoyer, J. Bustos, H. Brut, A. Cros, D. Munteanu, J.L. Autran, T. Skotnicki: IEDM 2003 conference proceedings (IEEE, Piscataway, N.J. 2003) p. 18.6.1–4
43 S. Huang, X. Cai, J. Liu: J. Am. Chem. Soc. **125**, 5636 (2003)
44 A. Ural, Y. Li, H. Dai: Appl. Phys. Lett. **81**, 3464 (2002)
45 P.G. Collins, M. Hersam, M. Arnold, R. Martel, P. Avouris: Phys. Rev. Lett. **86**, 3128 (2001)
46 R. Seidel, A.P. Graham, E. Unger, G.S. Duesberg, M. Liebau, W. Steinhoegl, F. Kreupl, W. Hoenlein: Nano Lett. **4**, 831 (2004)
47 W. Hönlein, F. Kreupl, G.S. Duesberg, A.P. Graham, M. Liebau, R. Seidel, E. Unger: Mater. Sci. Eng., C **23**, 663 (2003)
48 S.H. Kim, M.J. Misner, T. Xu, M. Kimura, T.P. Russell: Adv. Mater. **16**, 226 (2004)
49 W.B. Choi, B.H. Cgeong, J.J. Kim, J. Chu, E. Bae: Adv. Func. Mater. **13**, 80 (2003)