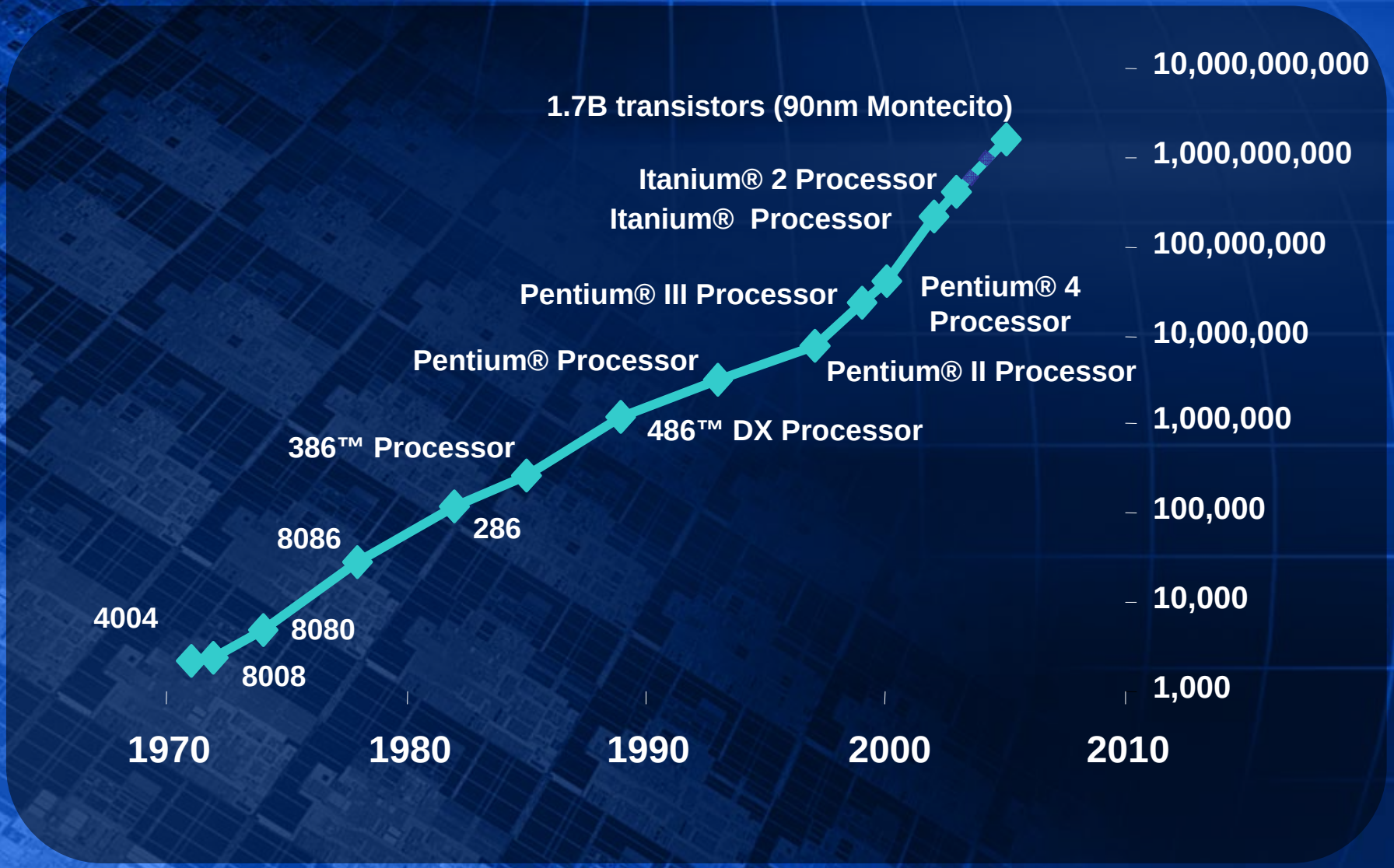
Silicon Nanotechnology at Intel

Ken David
Director of Components Research
Technology and Manufacturing Group
Intel Corporation
October 22, 2004

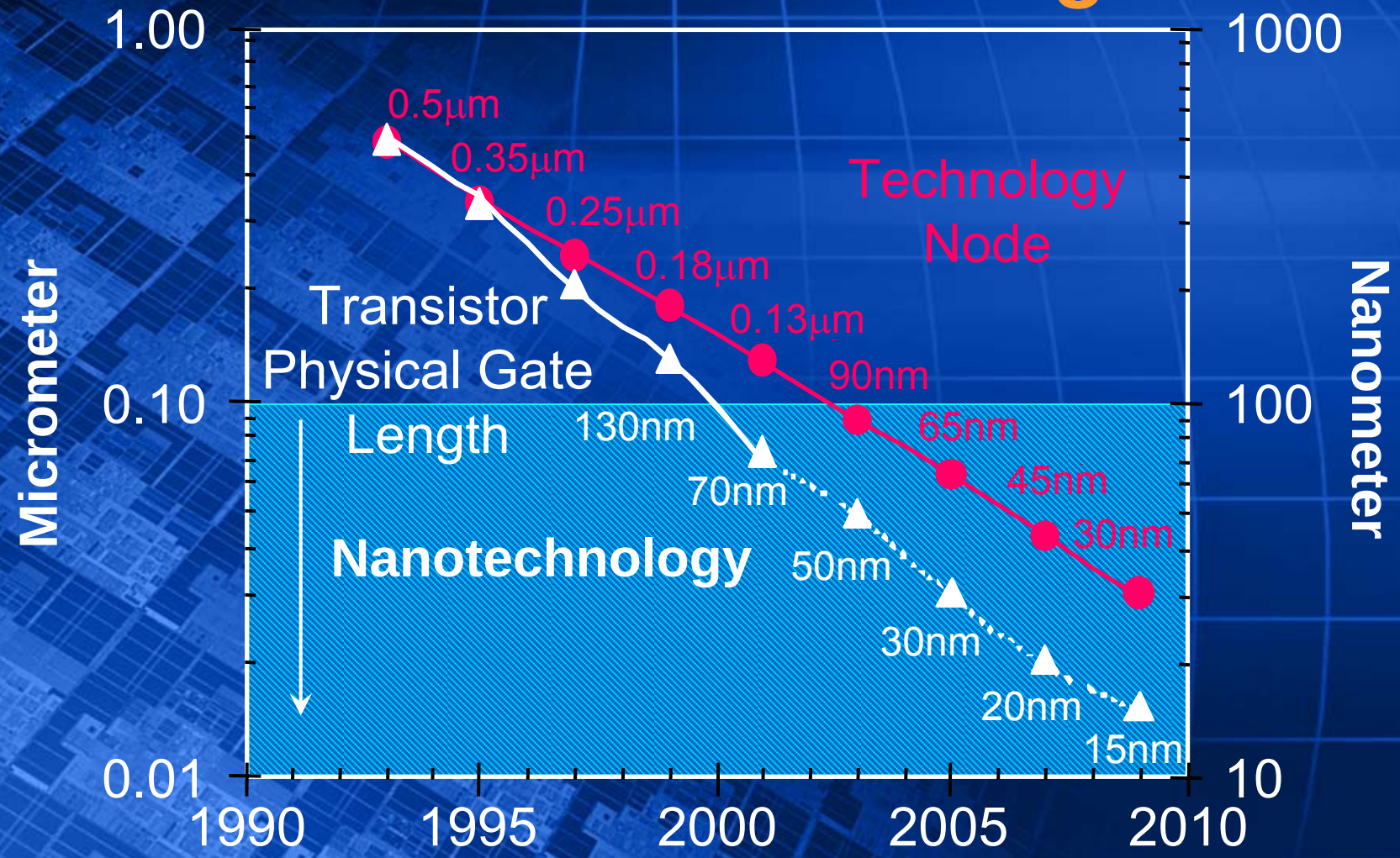
Moore's Law Continues…



Source: Intel

Increase in microprocessor complexity owing to improvement in transistors, interconnect and packaging

Transistor Scaling



Scaling to improve device speed/frequency of operation and to pack more transistors in a microprocessor.

Nanotechnology Research at Intel

Nanoscale materials, processes and technologies will continue the improvement of our products:

- **Transistor research – for improved device performance and scaling.**
- **Interconnect research – for improved wire conductivity and scaling.**
- **Manufacturing research – for improved usefulness of nanomaterials**

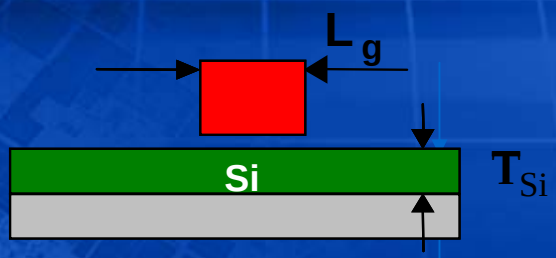
Transistor Nanotechnology Research at Intel

- Novel device architectures, e.g. Tri-gate
- Carbon Nanotubes
- Si and Non-Si Nanowires
- III-V Materials, e.g. InSb

GOALS:

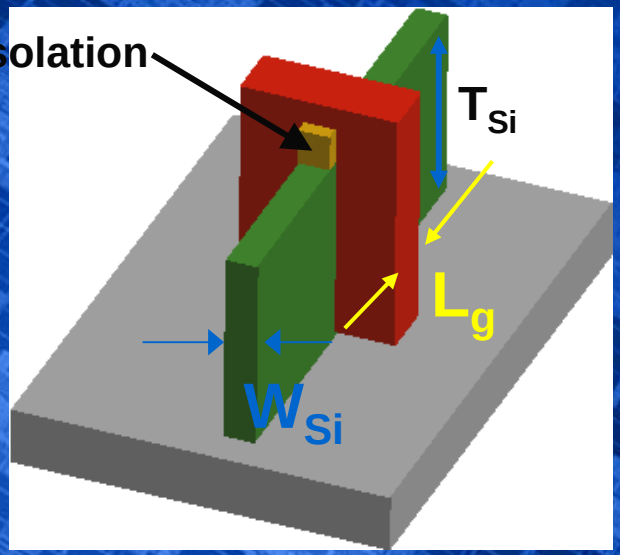
- Continue improving device speed/clock frequency
- Maintain/reduce power consumption
- Further dimensional scaling

New Device Architecture
Tri-gate



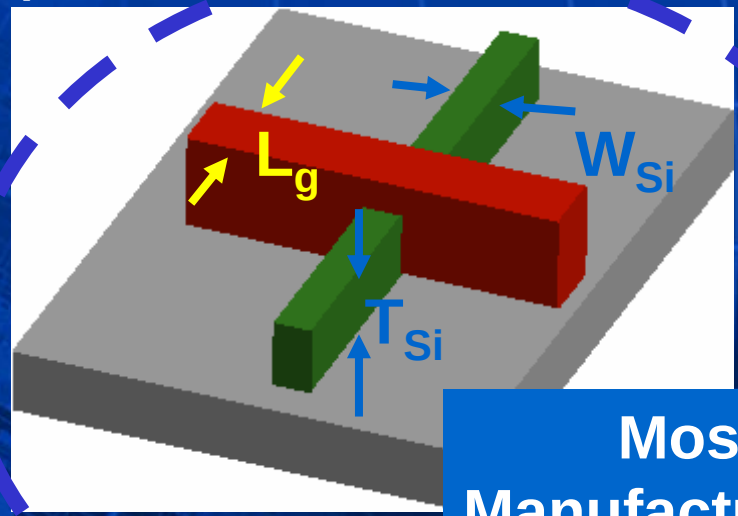
(Planar)

Planar fully depleted SOI



Double-gate (e.g. FINFET)

(Non-Planar)

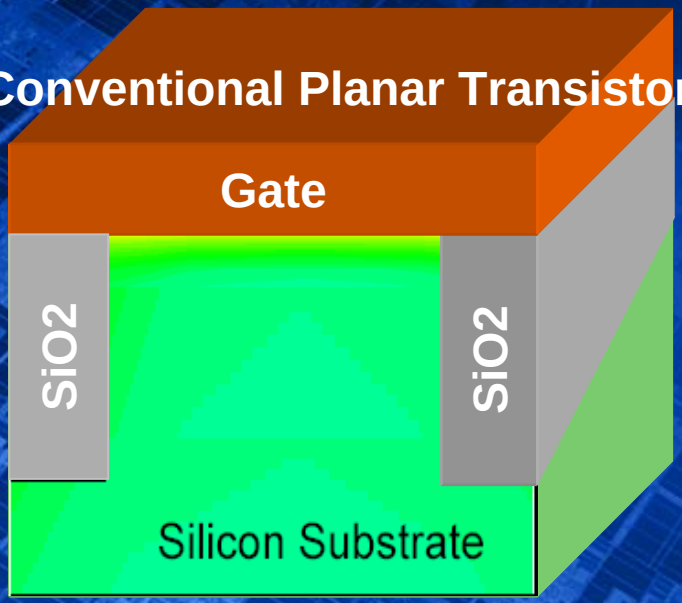


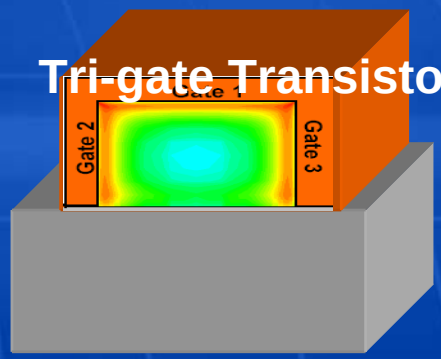
Most Manufacturable

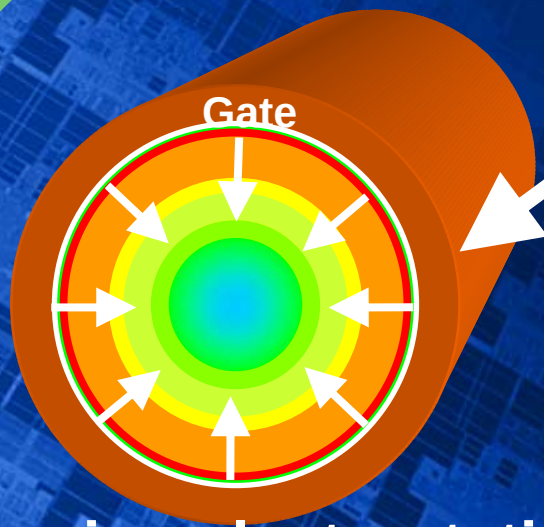
Tri-gate

(Non-Planar)

Nano-Device Structure Evolution





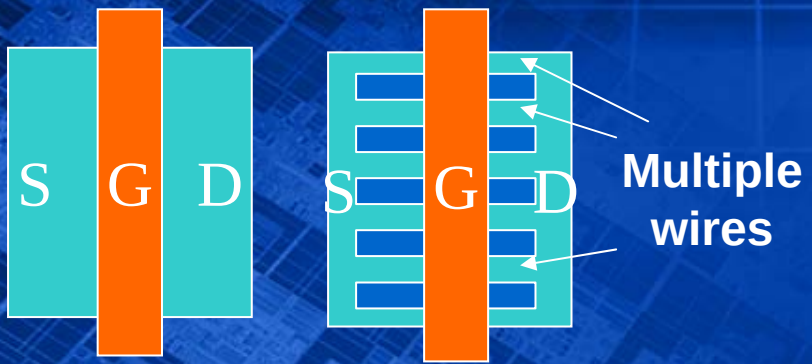


Improved Electrostatics

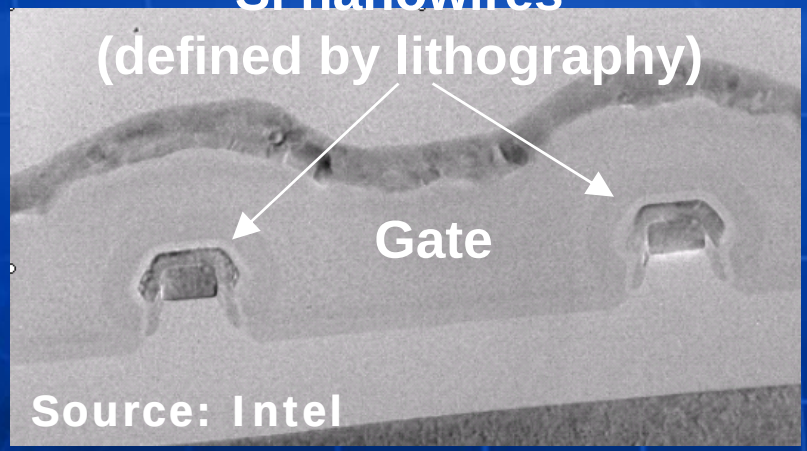
Best Electrostatics and Scalability

Improving electrostatics optimizes power consumption and performance

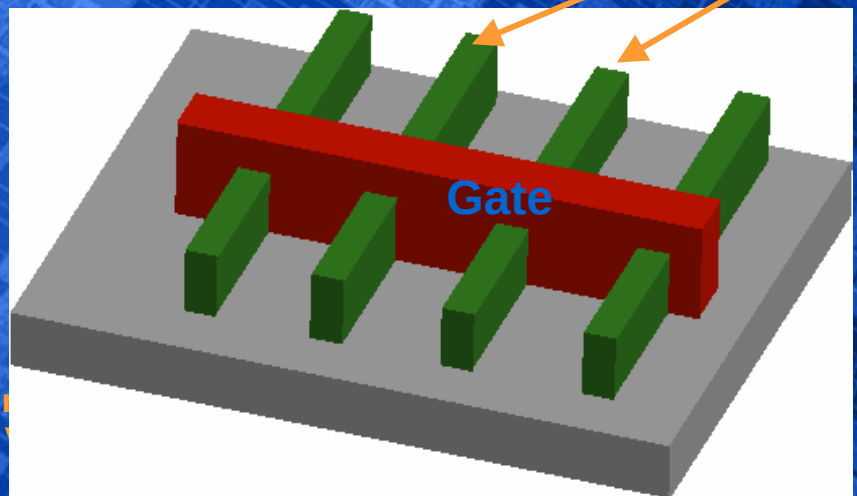
Tri-Gate Architecture: Template for the future

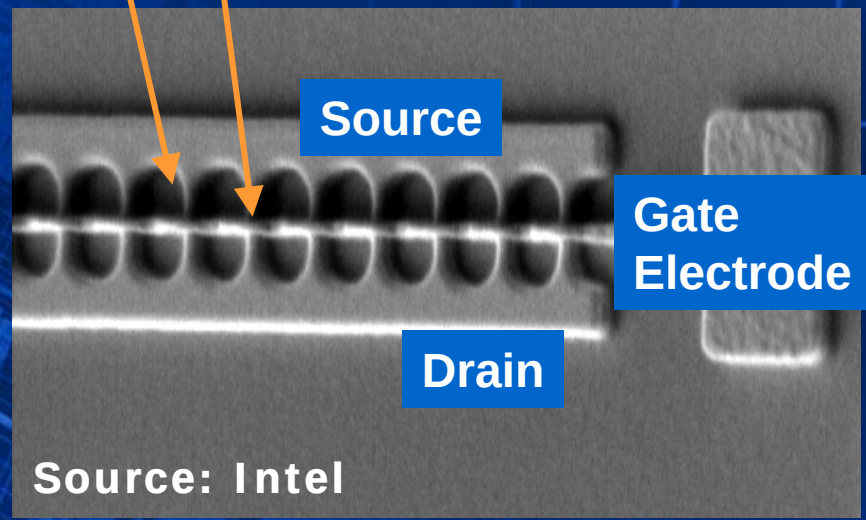


Total Drive Current = I_d per nanotube/nanowire x no. of tubes/wires

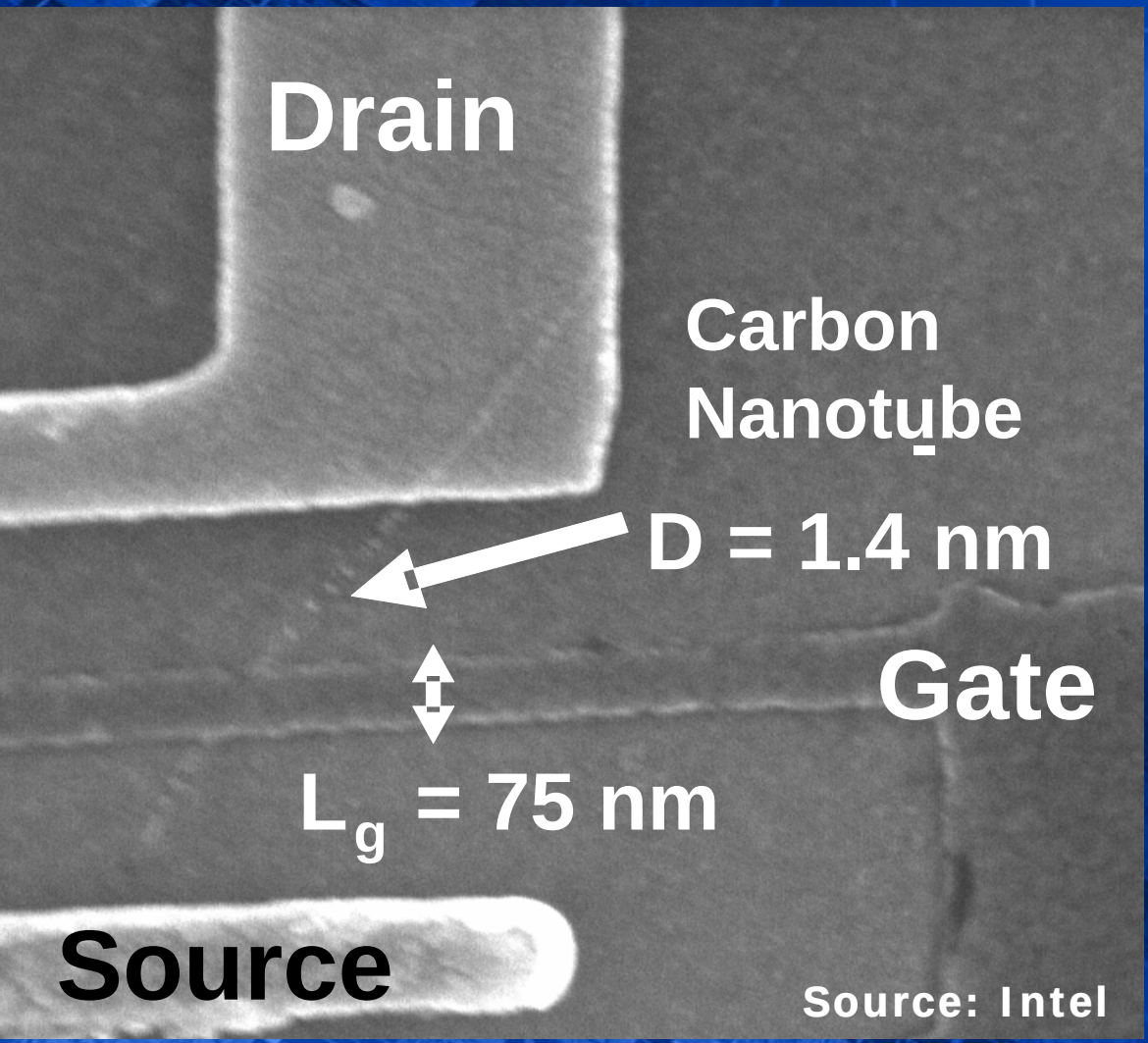


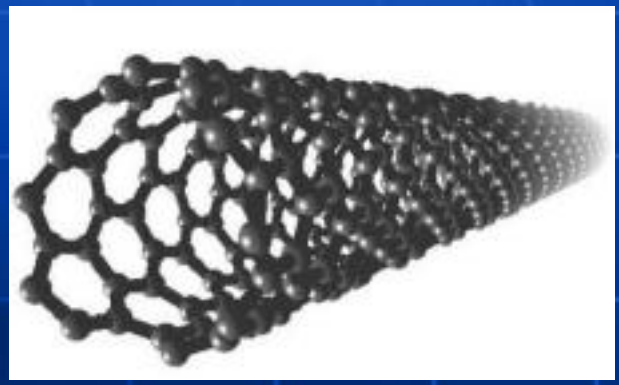
Silicon body, nanowires, nanotubes, etc.





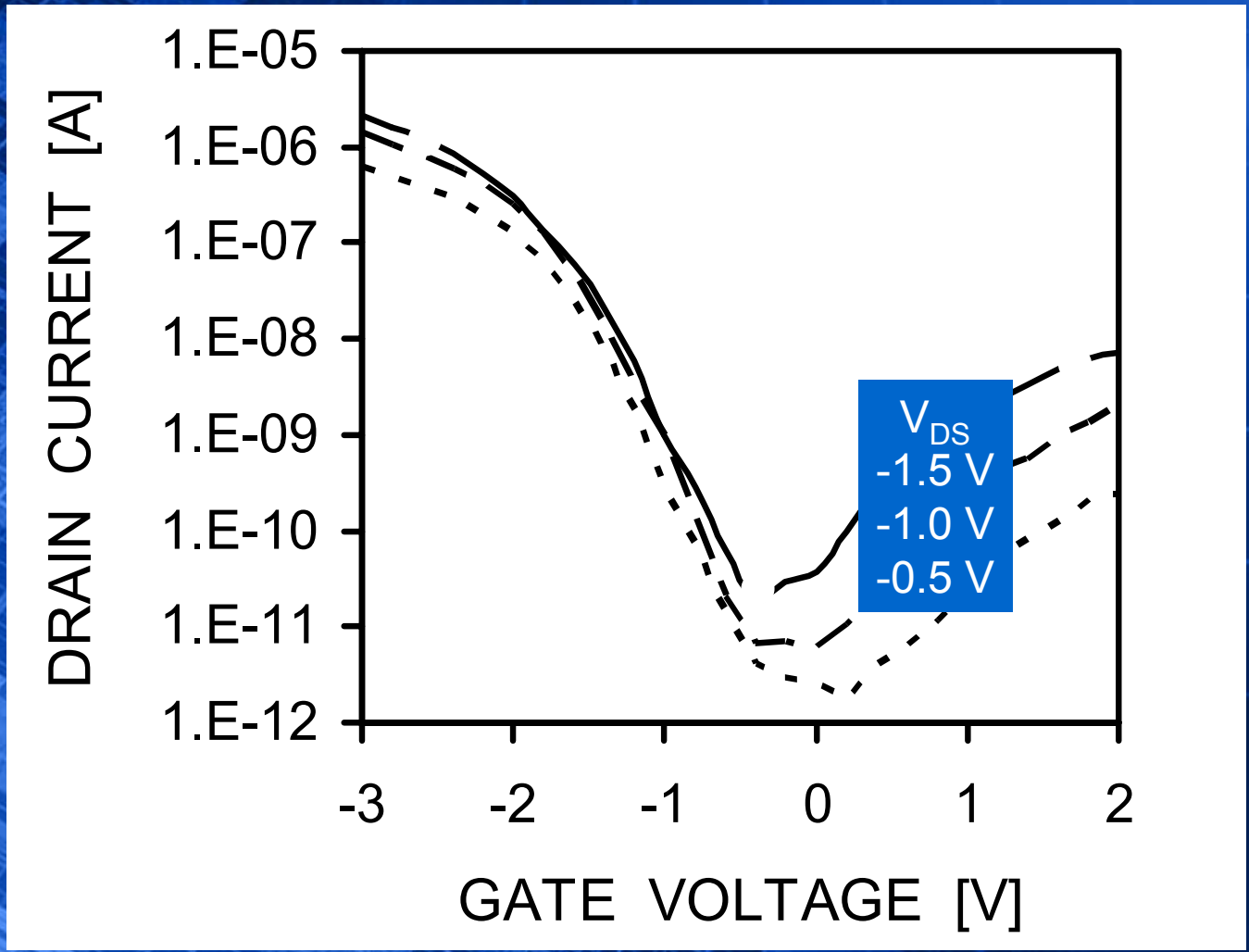
Carbon Nanotube Transistor





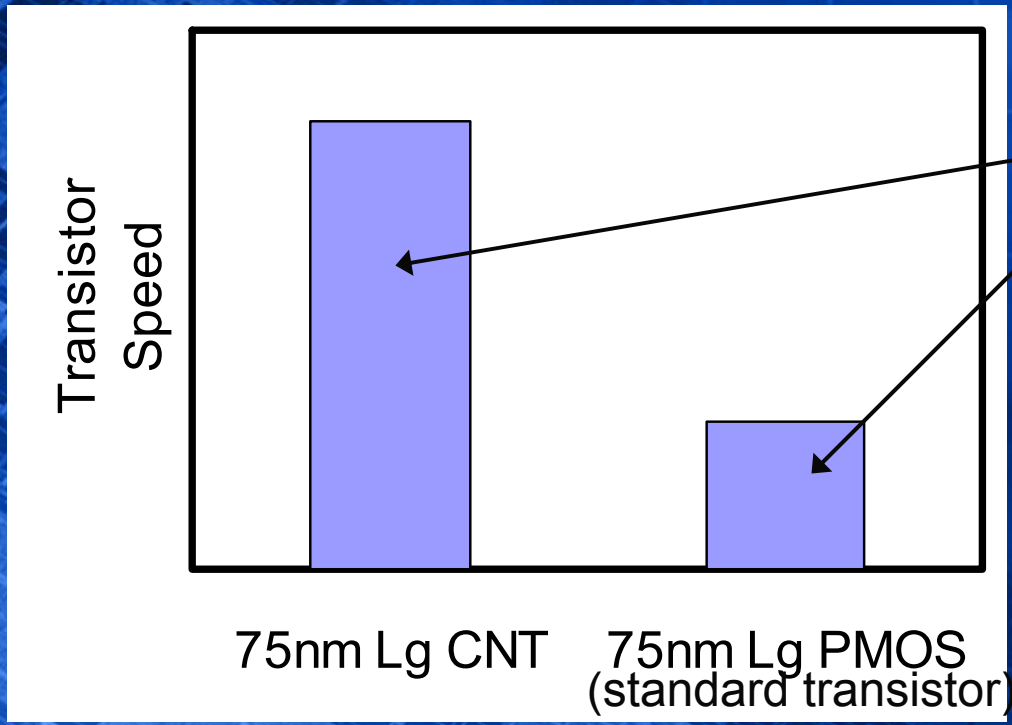
Chemically synthesized semiconducting nanotubes with diameter=2nm form the transistor channel.

Carbon Nanotube Research
Transistor Made at Intel



Nanotubes show transistor action similar to Si CMOS with excellent switching performance!

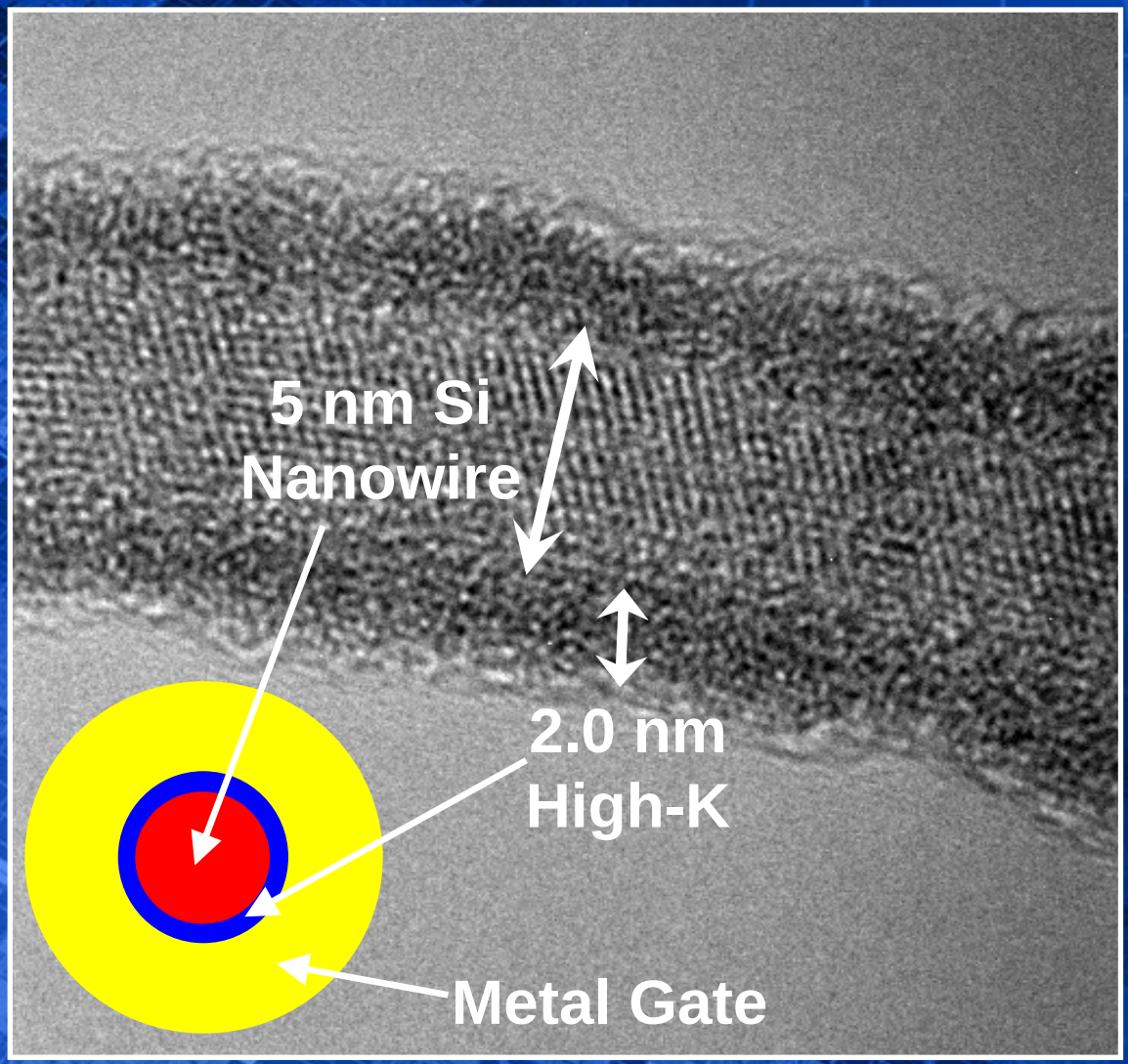
Relative performance benefit of Carbon Nanotube transistors



Potentially 3X faster transistor at same size and power consumption with use of CNT

CNT shows promise, but much device engineering optimization still to come !

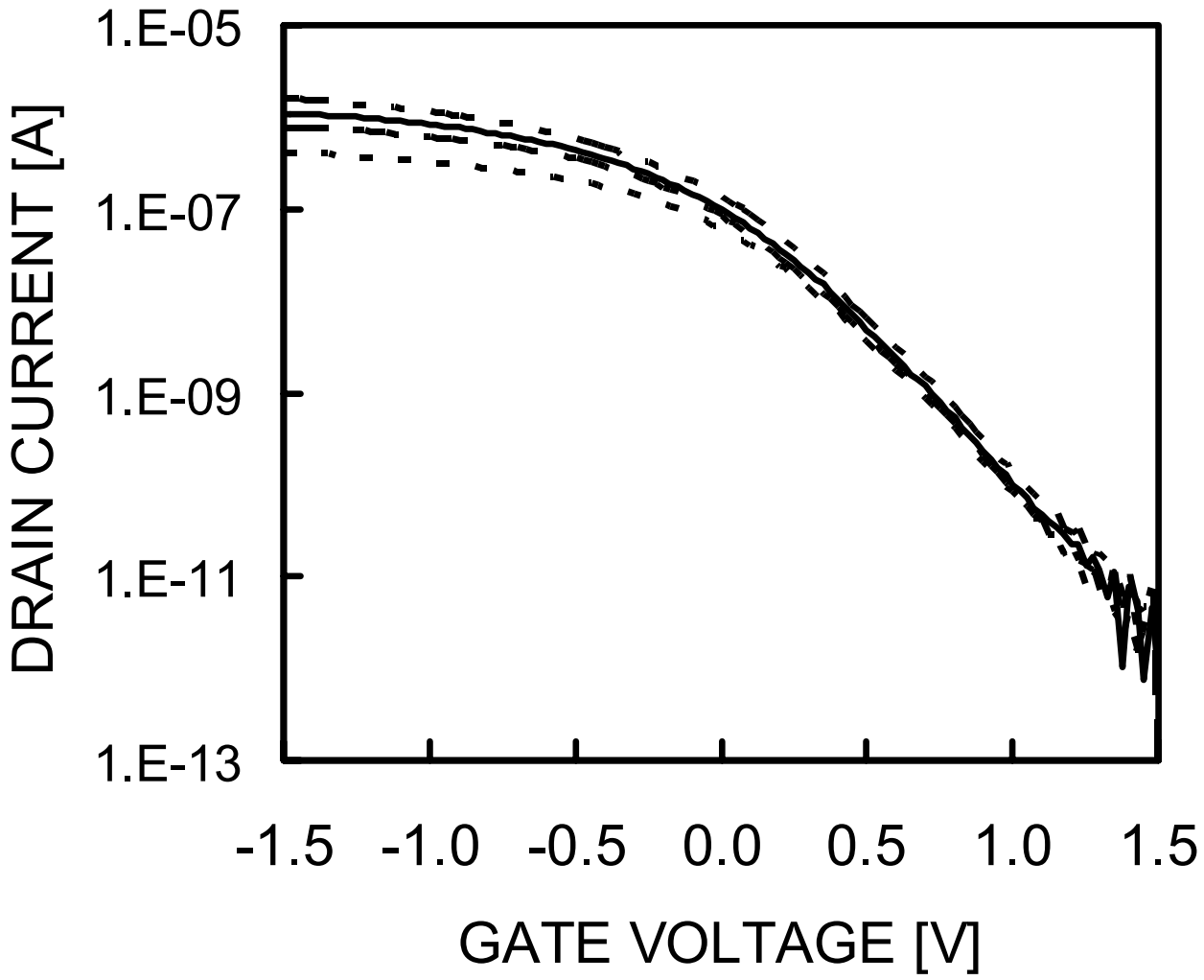
Semiconductor Nanowires



Chemically synthesized silicon nanowires with diameters <20nm (not defined by lithography).

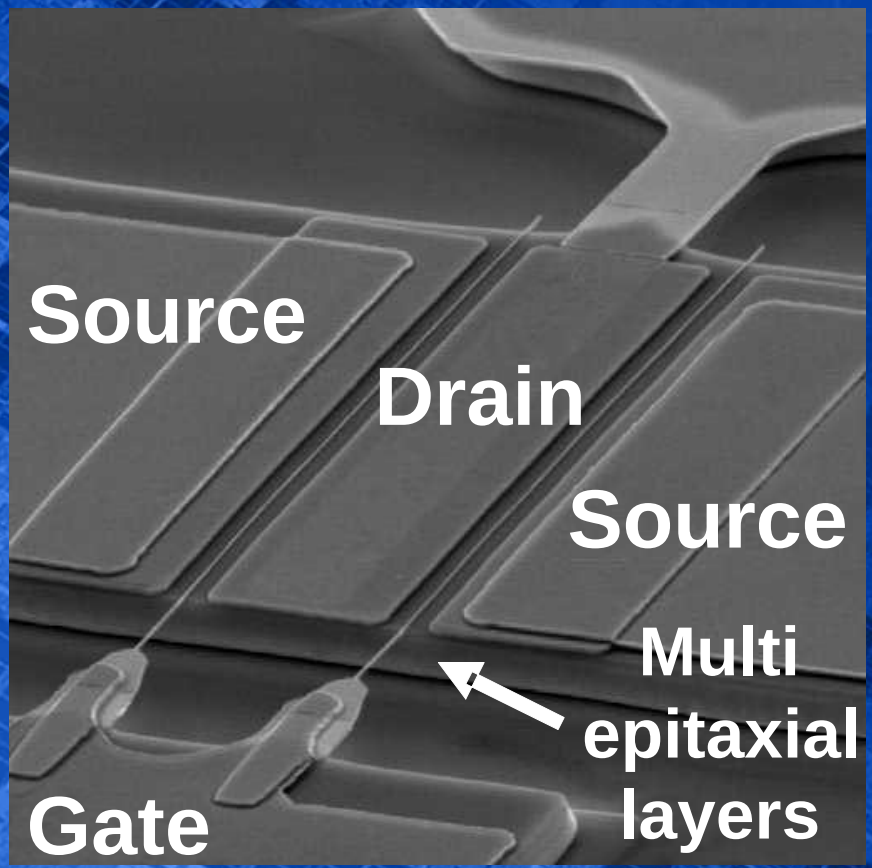
Source: Intel

Si-Nanowire Research Transistor Made at Intel



Functional Si nanowire transistors obtained and characterized.

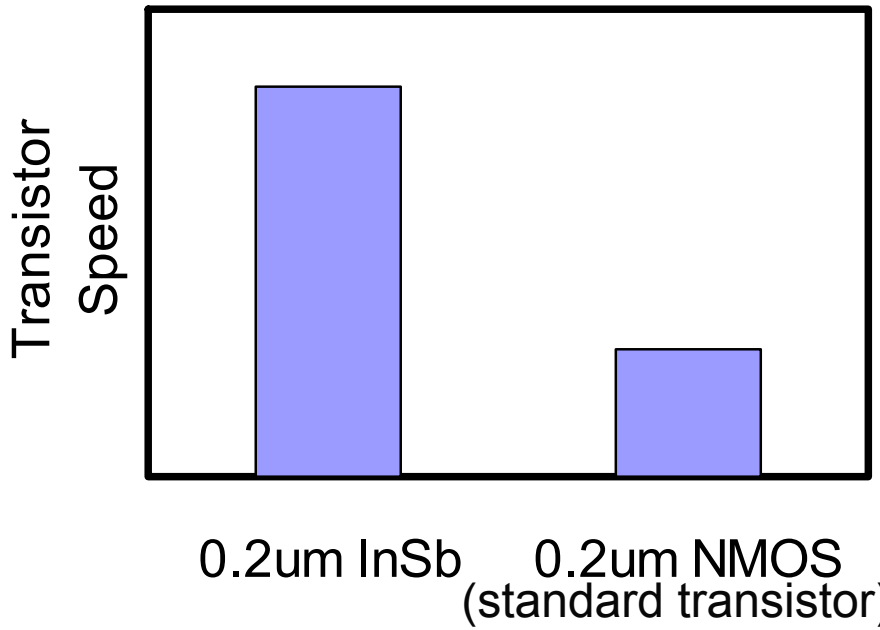
Another Nano Concept: Compound Semiconductor (III-V) Transistors

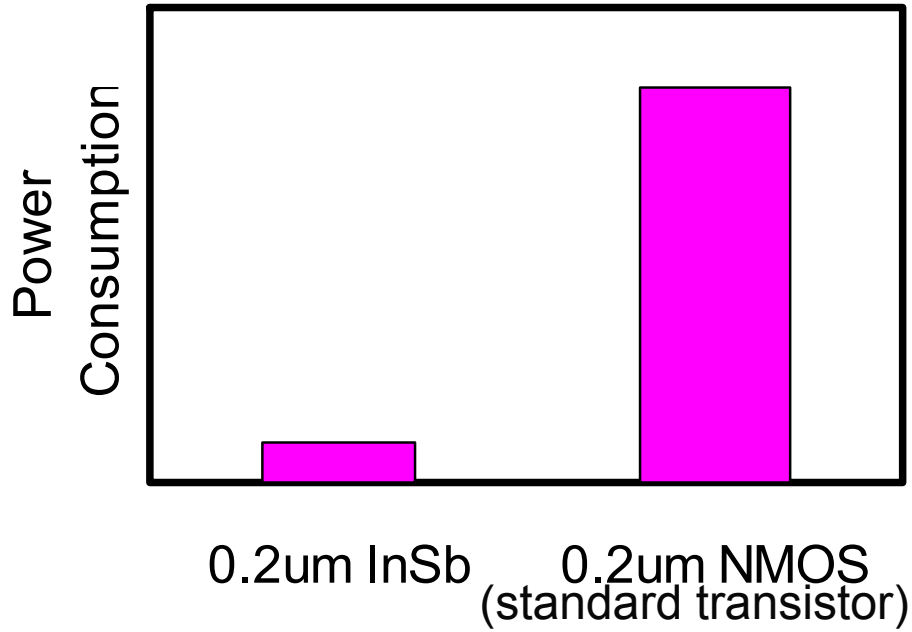


Source: Intel

Research transistor based on multi-epitaxial layer structure in compound semiconductors.

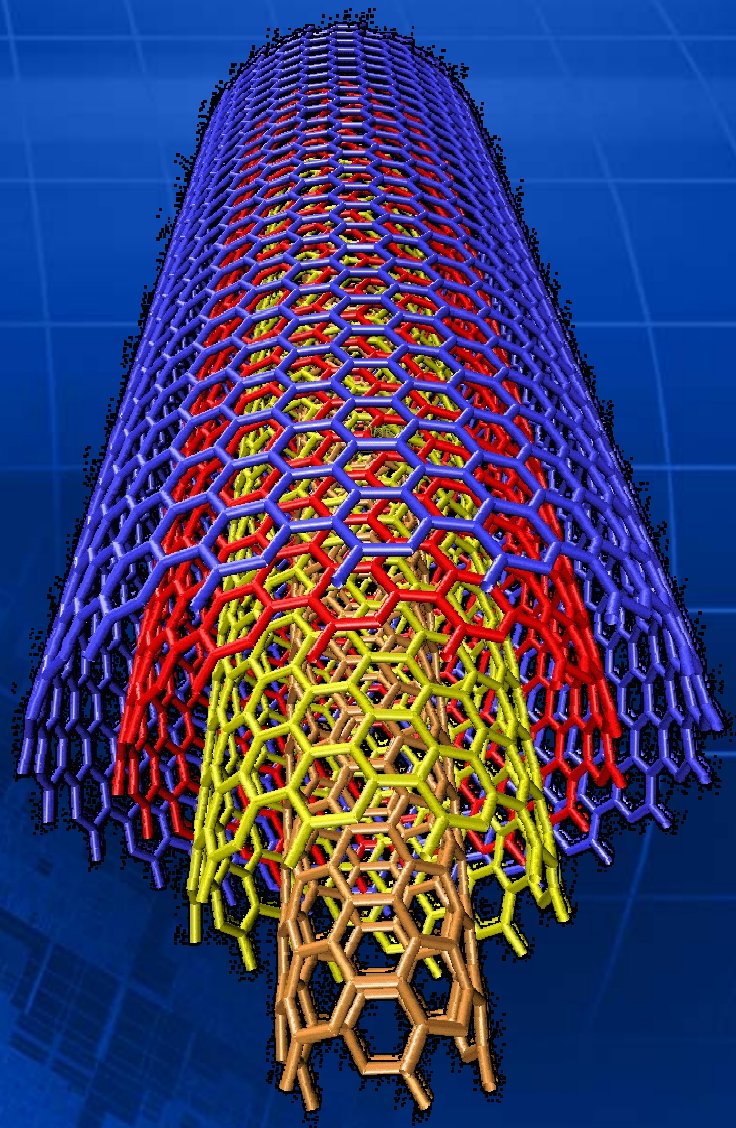
Relative performance benefit of compound semiconductor transistors





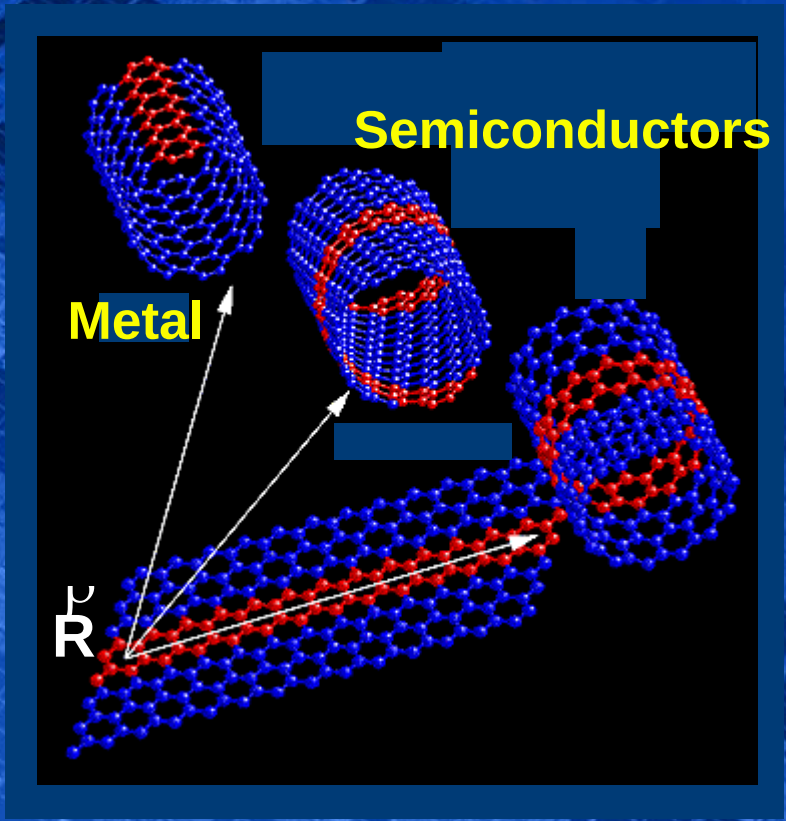
- **III-V transistors show promise**
  - **Integration with silicon key**

Carbon Nanotube Interconnects



Intel Nanotechnology
Virtual Open House

Carbon Nanotube Tutorial



- Rolled-up graphene sheet(s)
- Roll-up vector determines electronic properties of tubes
  - metallic
  - semiconducting
- Dimensions:

  1-25nm depending on how they are form.

Carbon Nanotube Interconnects

- Resistance of Metal lines increases as lines are scaled.
  - Electrons collide with walls of wire causing increase in resistance.
  - Collisions can damage wire over time

- **Nanotubes:**

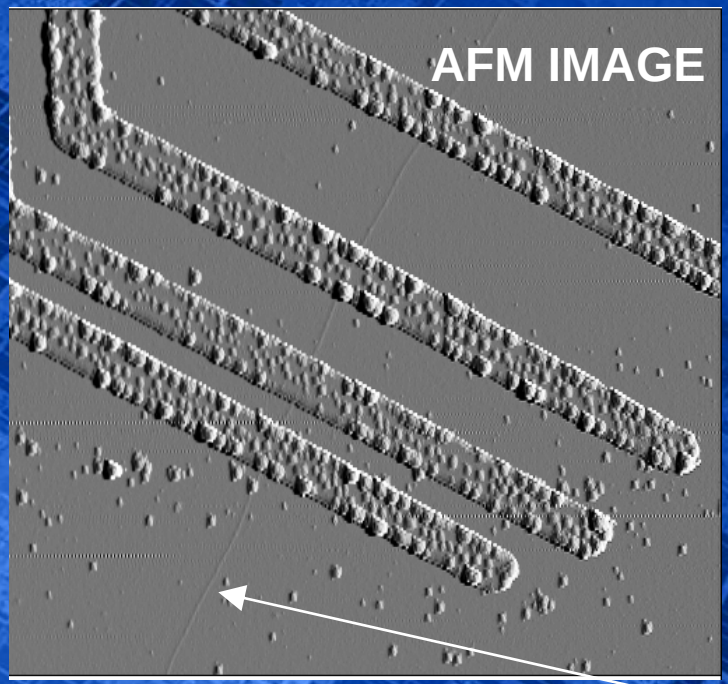
  Conduct current in a linear fashion and avoid these collisions: 1-D transport

  Able to pass high current without failure: 10^9 A/cm^2 (Cu 10^6 A/cm^2)

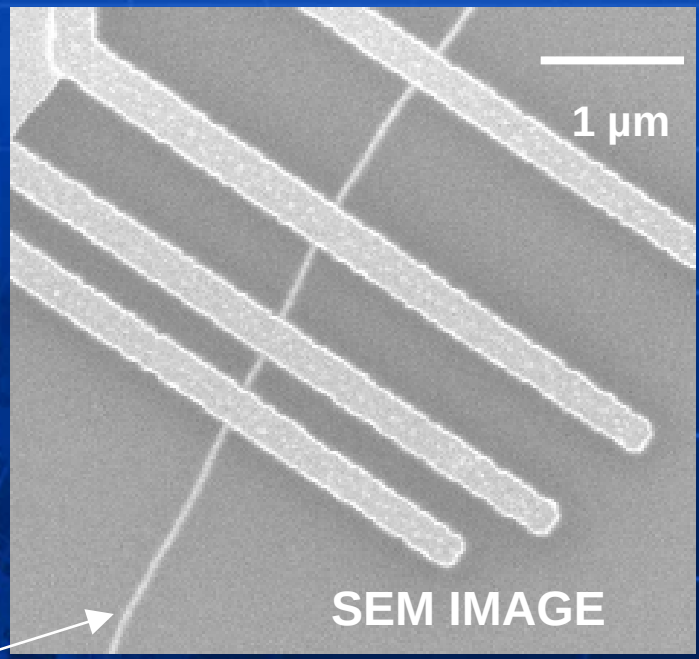
  Good mechanical stability (strength and toughness); enables other processing (etch/cleans)

Results – Aligned Nanotubes

- Single tube measurement research structures



Source: Intel



Source: Intel

Aligned, separated and long (few microns) single-walled nanotubes with narrow diameter distribution (~1.0 nm) have been produced with resistance lower than copper.

Nanomaterial Manufacturing Research

Source: Intel

Carbon nanotubes have important material properties

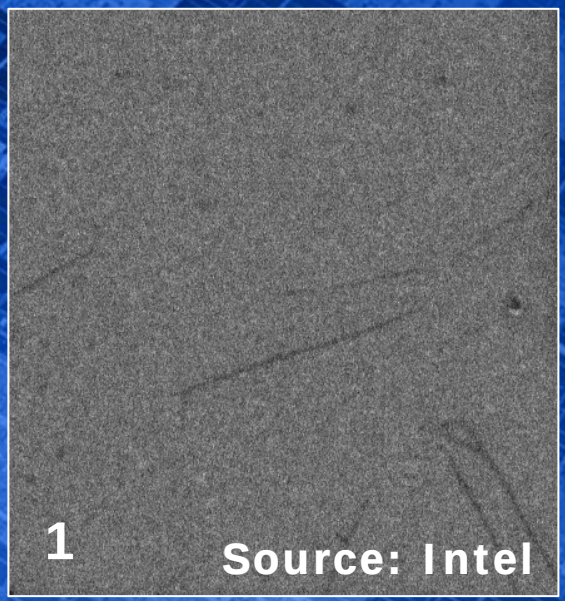
- High thermal conductivity
- High current carrying capability
- Metallic or semiconducting

In their current form nanomaterials are difficult to utilize to build integrated circuits.

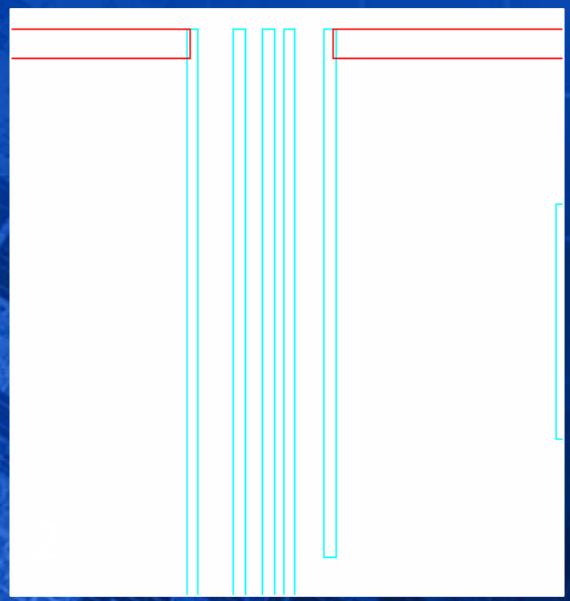
Intel has research programs to bring these materials from lab to fab

Nanodevice patterning

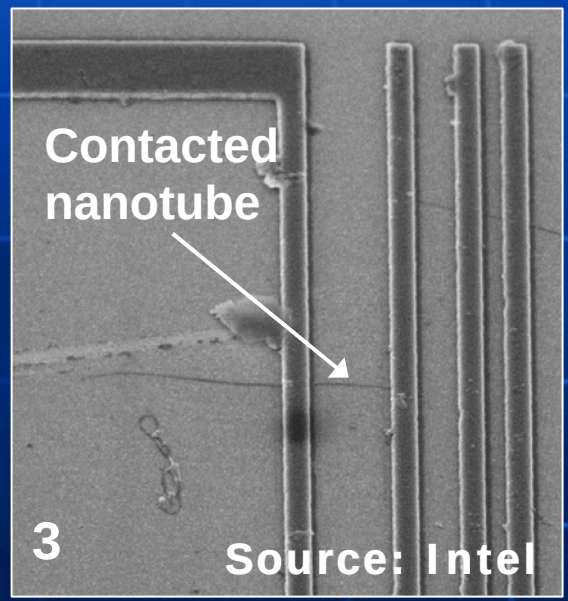
- Nanotube paterning process developed to make devices.



SEM image following nanotube deposition



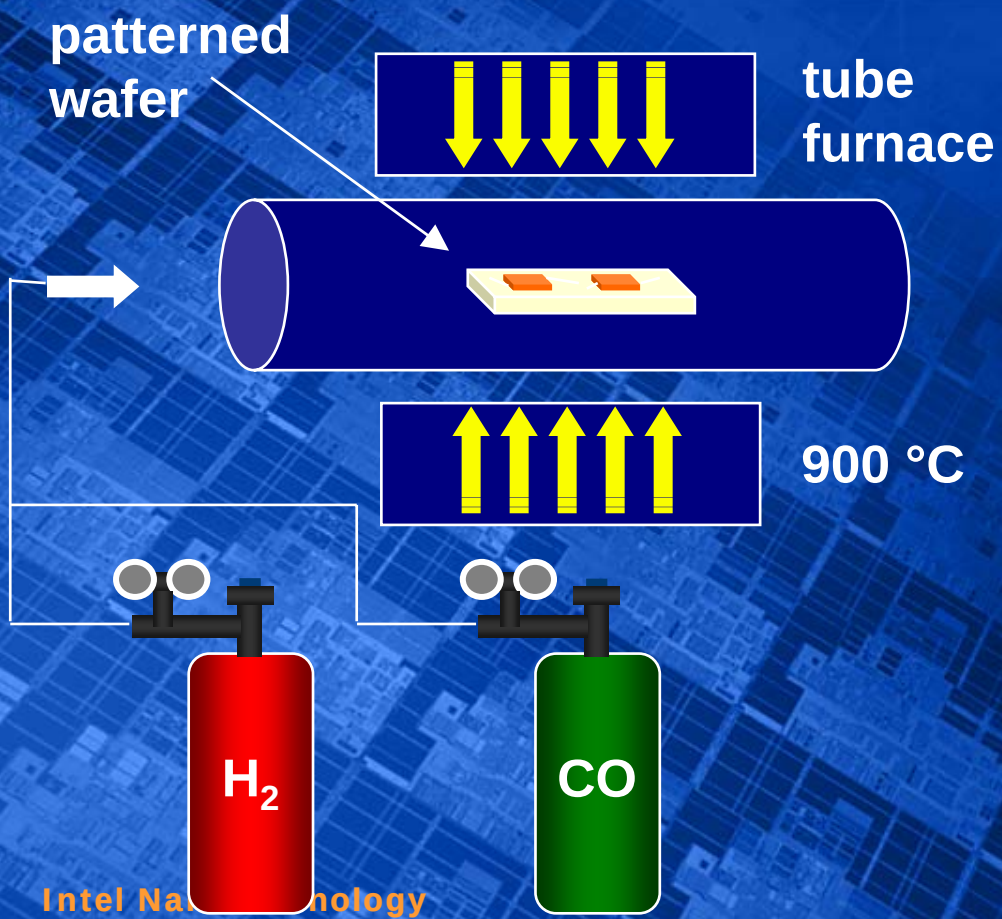
Mask for e-beam litho

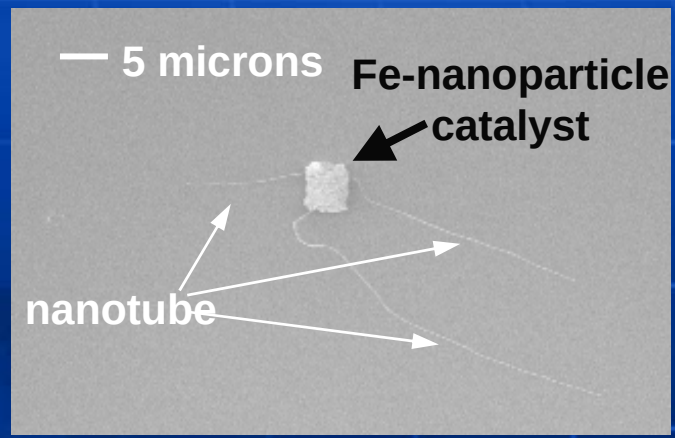


Metal electrodes after:
- e-beam litho
- contact evaporation
- liftoff

Carbon Nanotube Growth

Chemical Vapor Deposition (CVD)





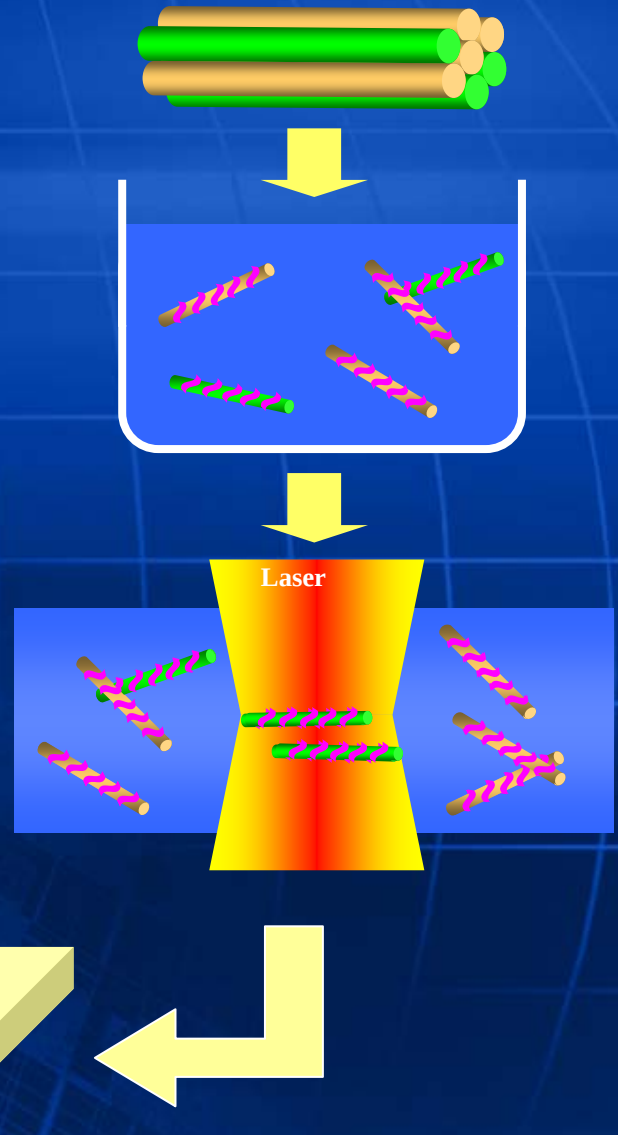
Source: Intel

CVD method has been utilized to grow individual carbon nanotubes from patterned catalysts on wafers

Intel Nanomanufacturing Research

Our Approaches:

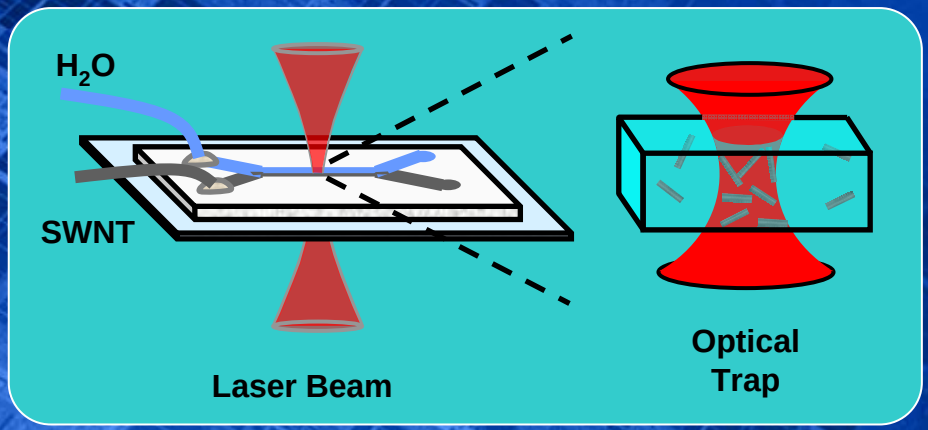
- **Nanotube functionalization**
  - To isolate individual tubes from mixed bundle
- **Sorting**
  - Separate nanotube types & sizes
- **Assembly into useful forms**
  - Directed self assembly

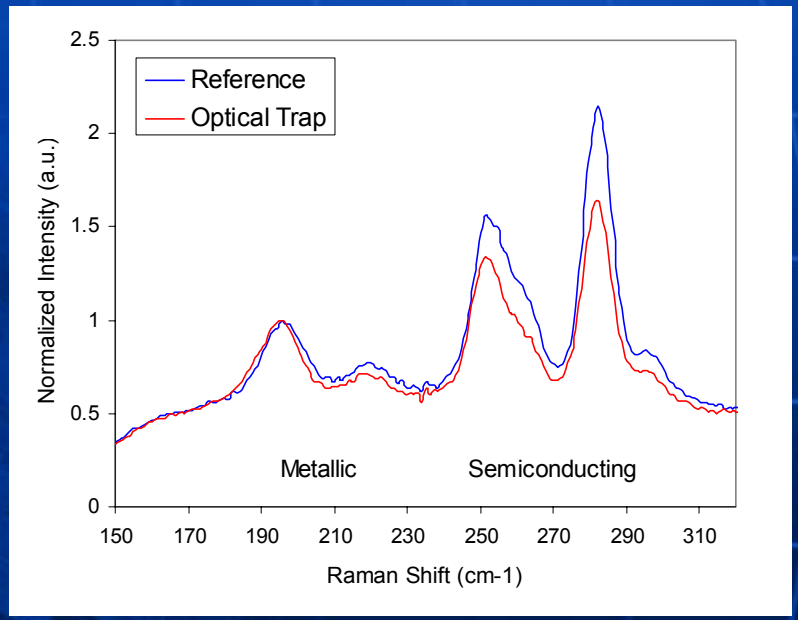


Nanomanufacturing Research

Optical Trapping To Sort Nanotubes

Current Research Results





Optical Trapping Produces a Small Enrichment of Metallic Nanotubes

Directed Self Assembly

Research Results

Source: Intel

Electric Field Alignment **Aligned Nanotubes**

Nanotubes are aligned parallel to the electric field

Conclusions

- Moore's Law is alive and well: CMOS transistor scaling is expected to continue until around 2020, with new architectures such as trigate, carbon nanotubes, nanowires and III-V.
- Intel has initiated internal research programs as well as extensive joint research programs with universities and consortia on nanotechnology
- Promising research results in areas such as spintronics, phase change, and optical switches, may provide a path for beyond 2020.