Innovation and Integration in the Nanoelectronics Era

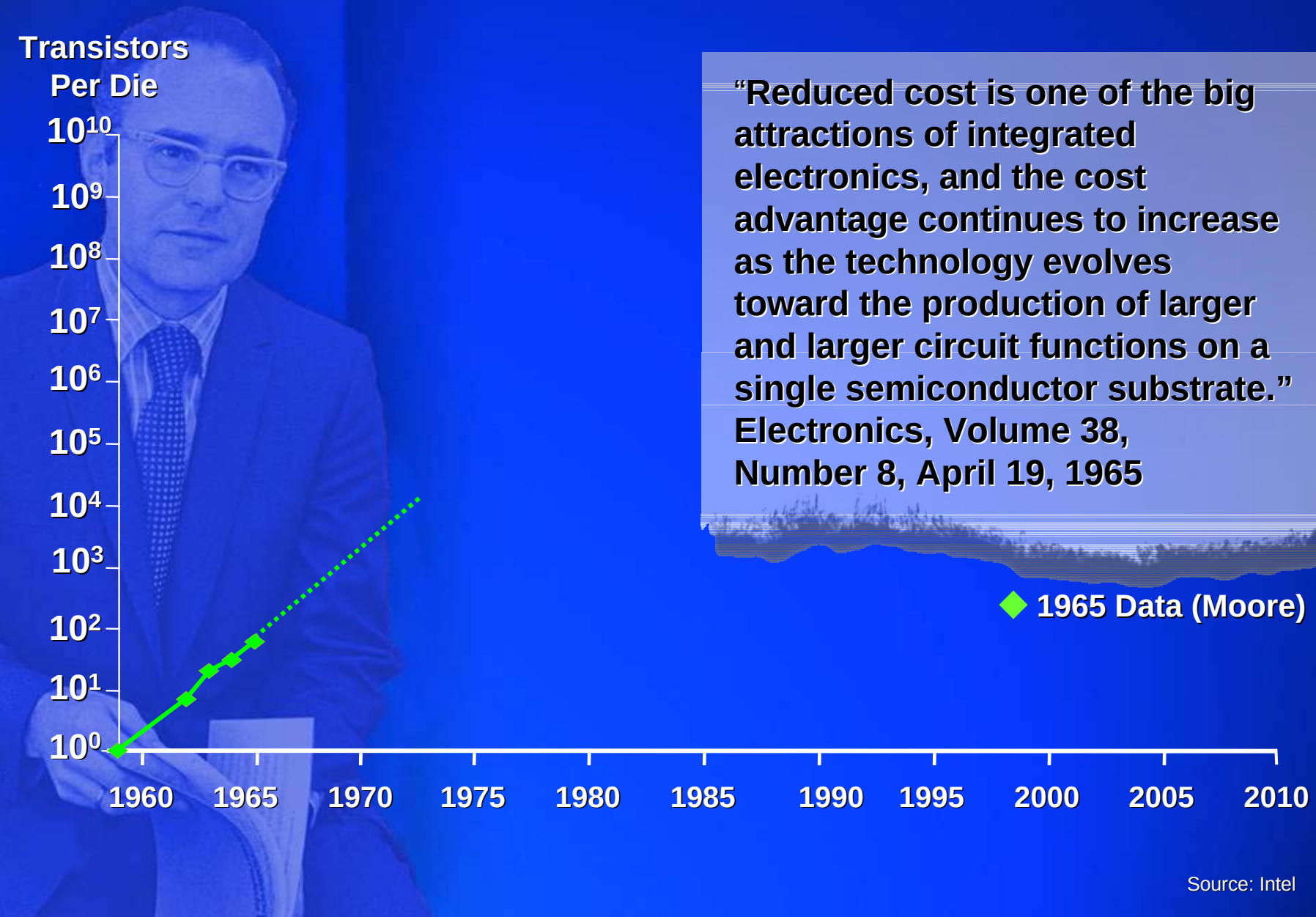
Sunlin Chou
Technology and Manufacturing Group
Intel Corporation

International Solid-State Circuits Conference
February 2005

Key Points

- Moore’s Law thriving after 40 years

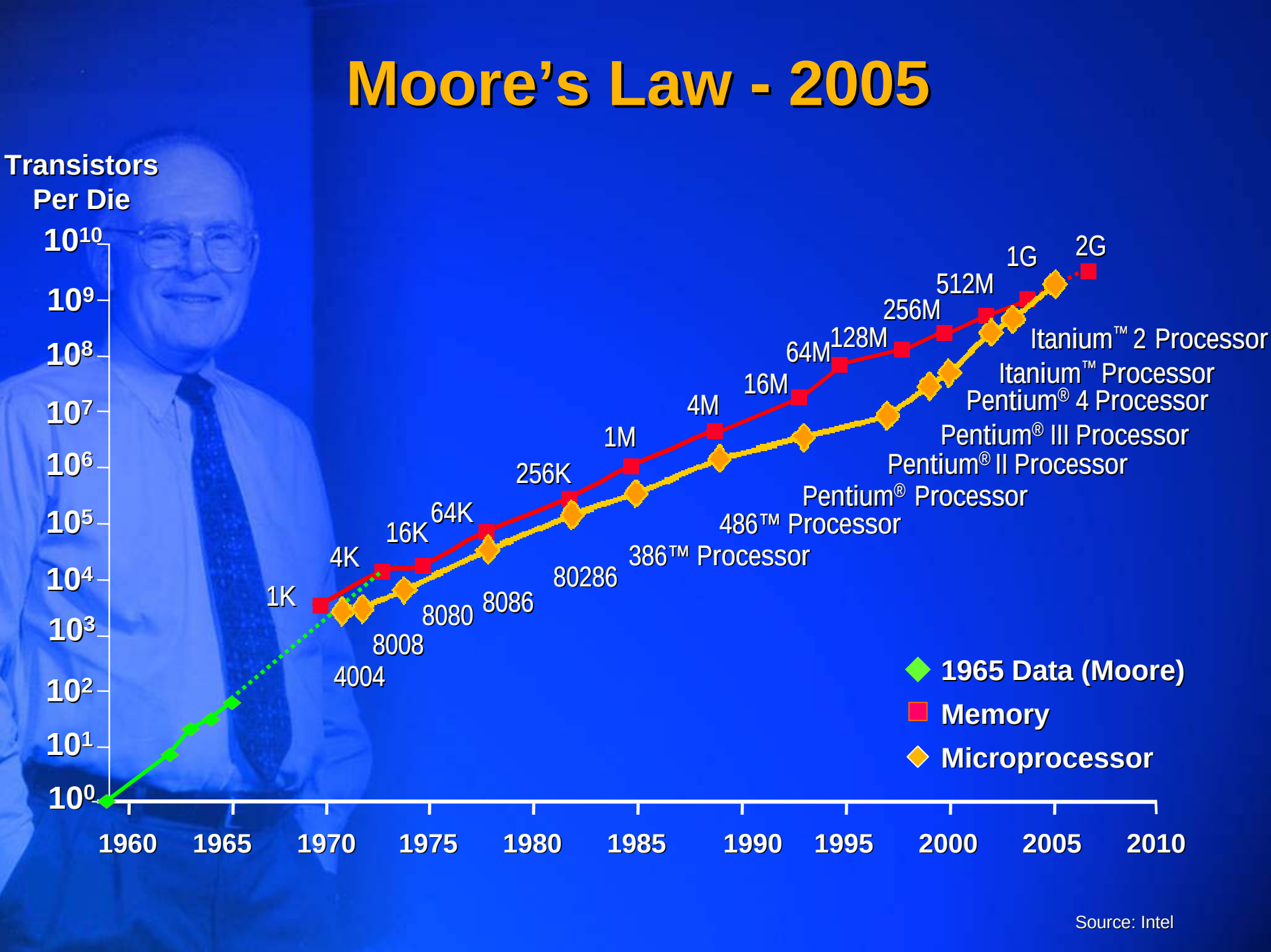
Moore's Law - 1965



"Reduced cost is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate."
Electronics, Volume 38, Number 8, April 19, 1965

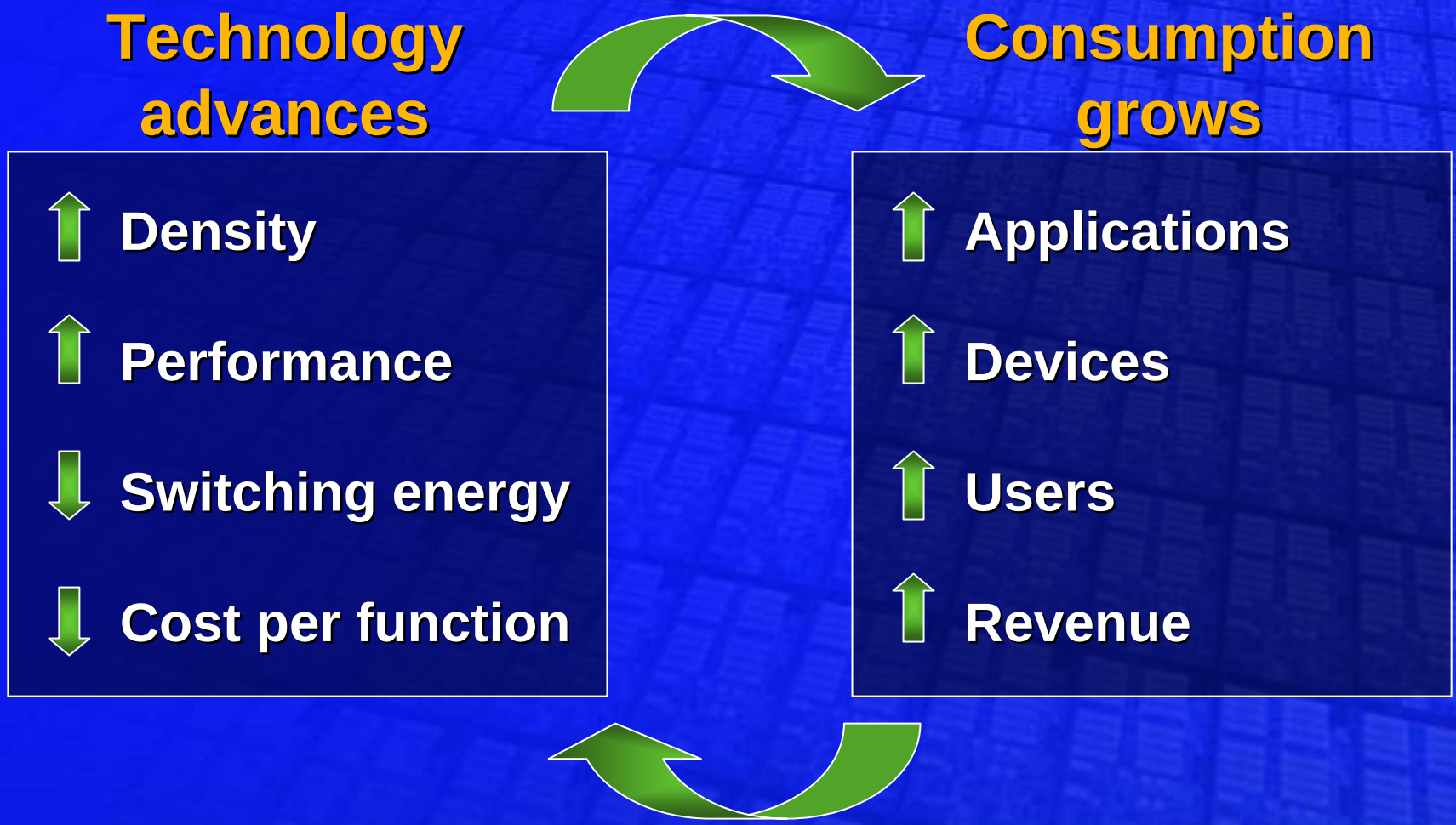
Source: Intel

Moore's Law - 2005

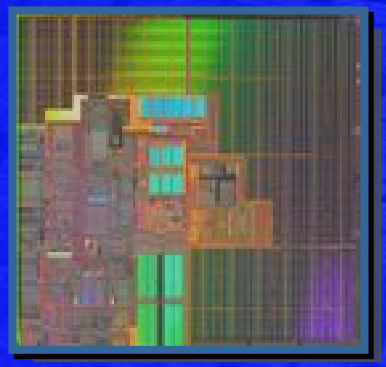


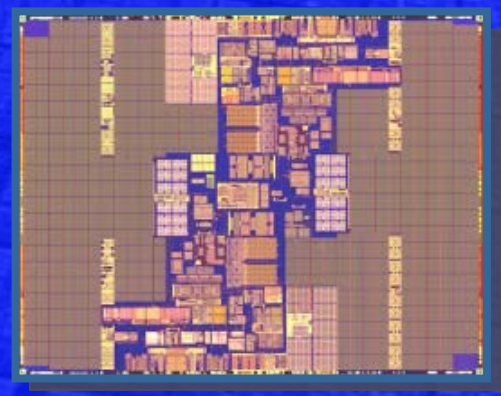
Source: Intel

The IC Growth Cycle



Silicon Scaling Still Improves Density, Performance, Power, Cost





	130 nm Madison	90 nm Montecito	
Cores/Threads	1/1	2/4	
Transistors	0.41	1.72	Billion
L3 Cache	6	24	MByte
Frequency	1.5	>1.7	GHz
Relative Performance	1	>1.5x	
Thermal Design Power	130	~100	Watt

Source: Intel

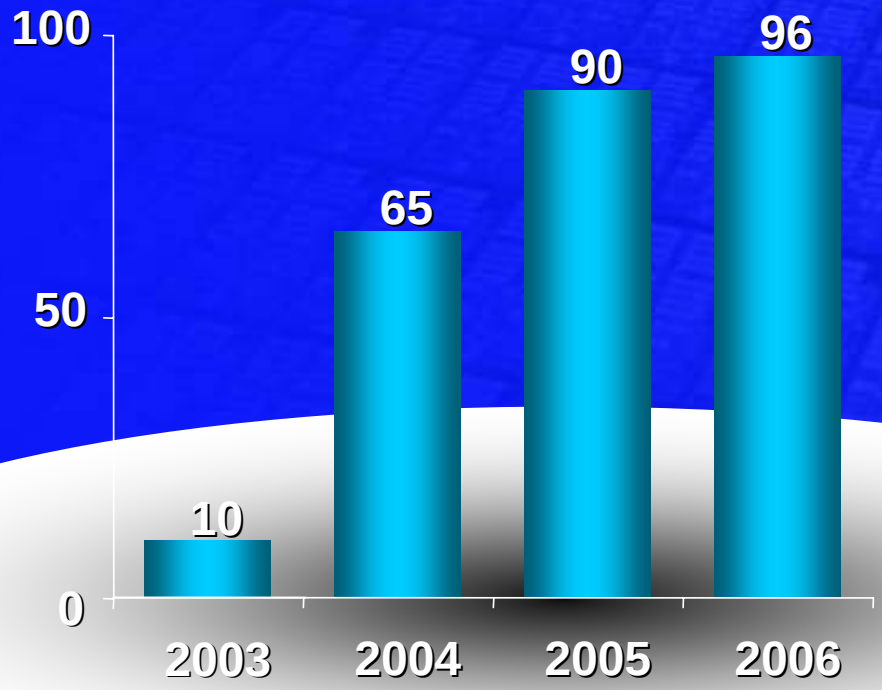
Key Points

- Moore’s Law thriving after 40 years
- Convergence drives IC industry growth

Convergence Drives Growth

Convergence
Wireless Mobile PC

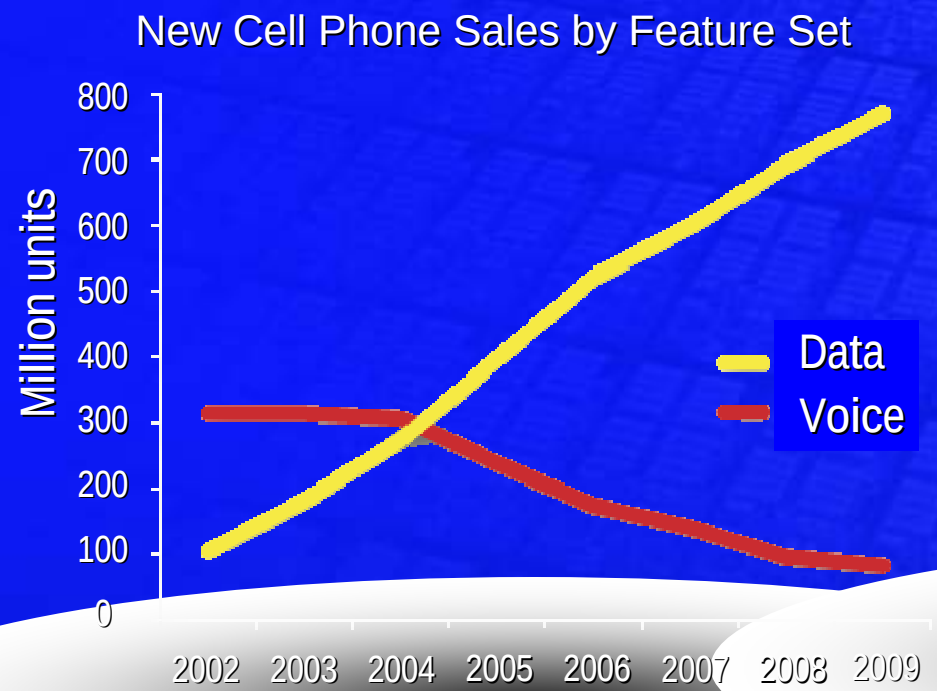
% of Notebooks that have Wireless



Source: IDC

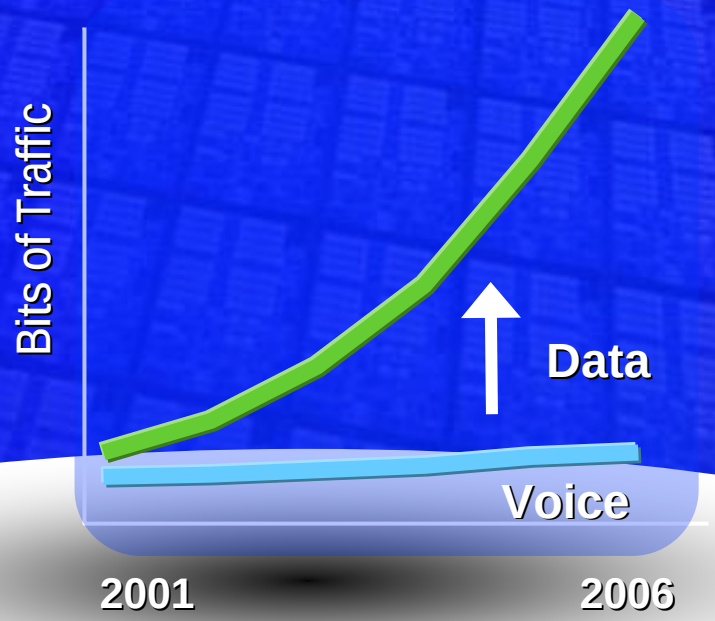
Convergence
Data Phones and Traffic

2004: Data Phones Cross-over Voice



Source: WebFeet Research

Data Traffic: 56% Annual Growth thru 2006

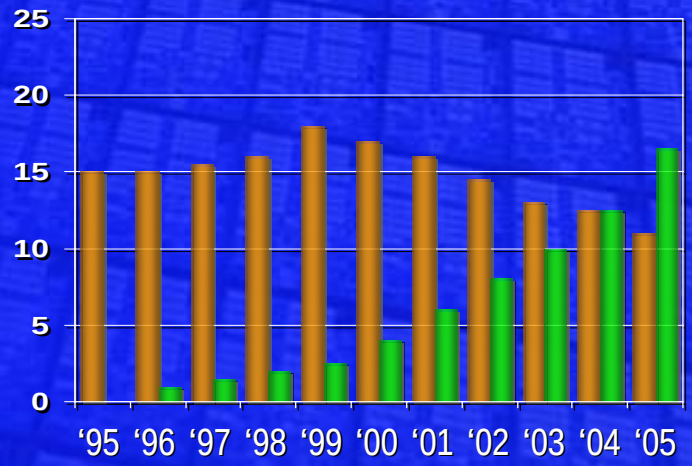


Source: Goldman Sachs and Co., McKinsey & Company, Dec. 2002

Convergence
Digital Consumer Electronics

The Great Crossover
Digital Technologies Surpass Analog

Camera Sales
Millions



Sources: Consumer Electronics Association, Photo Marketing Association International, Photofinishing News, SBCA/Sky Trends

Key Points

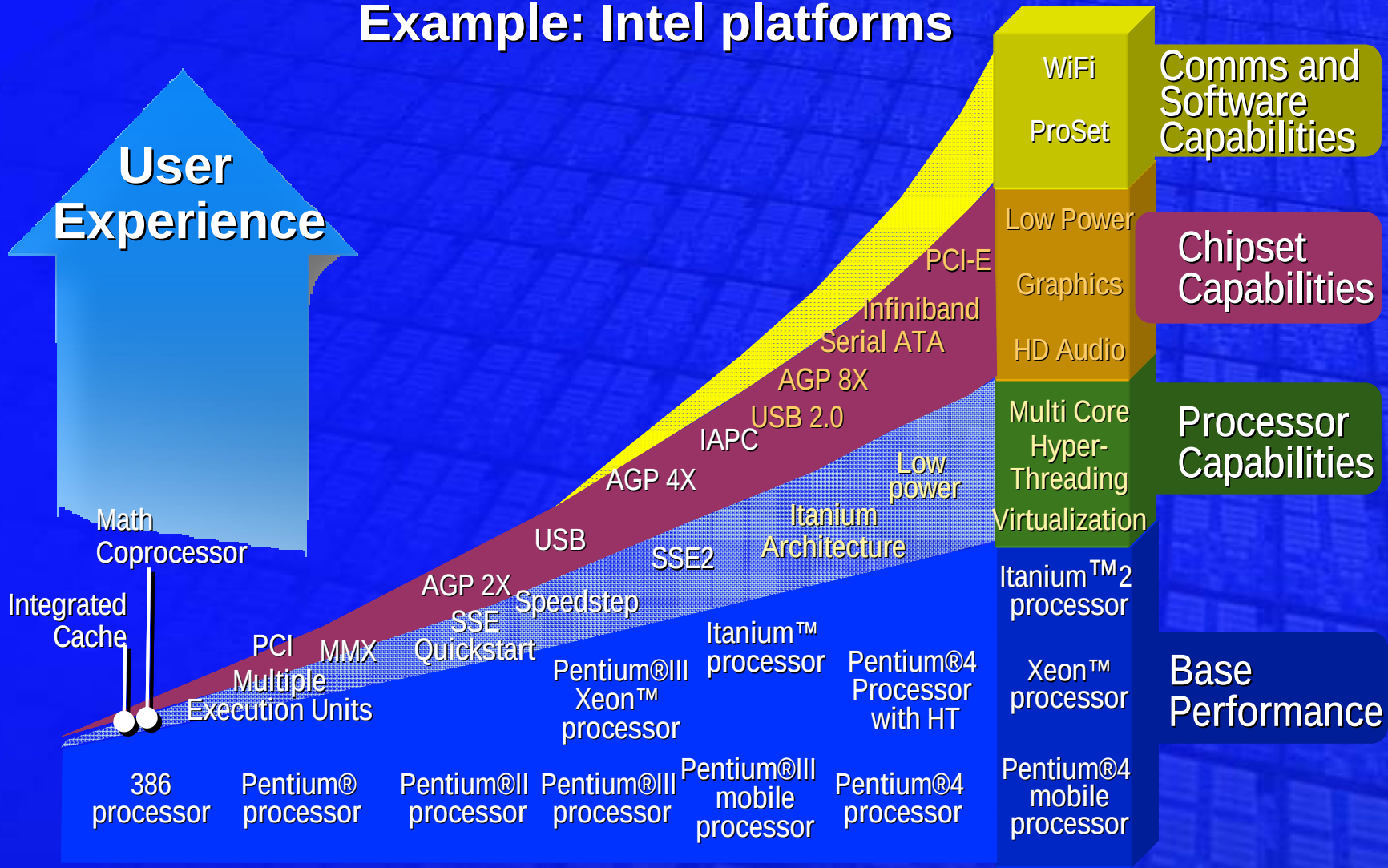
- Moore’s Law thriving after 40 years
- Convergence drives IC industry growth
- Integrated platforms optimize user experience
- Multi-core parallelism going mainstream

Demand Growth Driven by Better User Experiences

Security
Virtualization
Multitasking
Manageability
Ease of Use
Battery Life
Compactness
Wireless Mobility
Multimedia
Networking
Graphics
Computing
Memory

Platforms Optimize User Experience

Example: Intel platforms

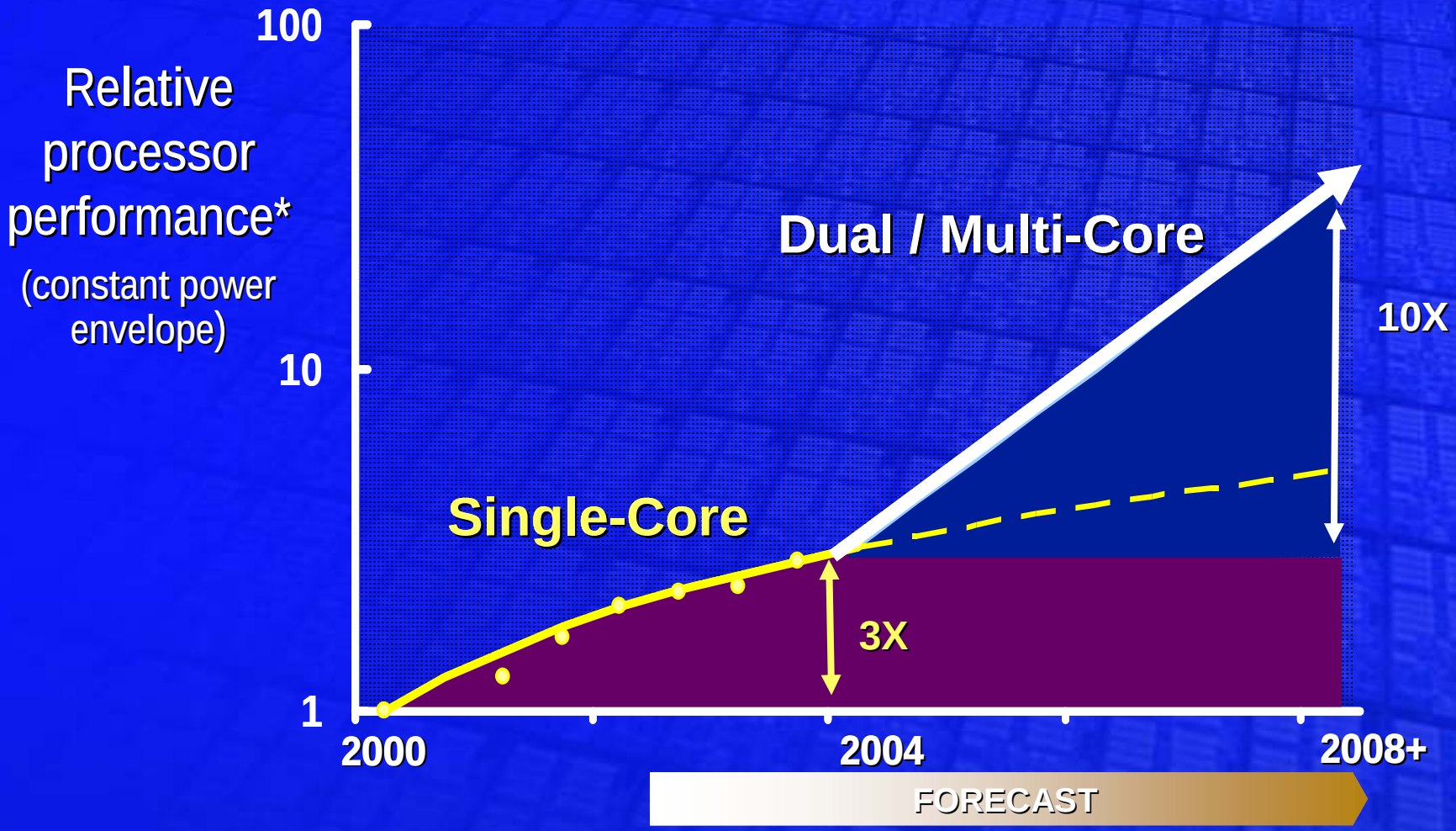


Innovate and Integrate

RMS Applications Growing

Emerging workloads increase need for high performance parallel processing

Performance and Power Efficiency Increase with Parallel Architecture

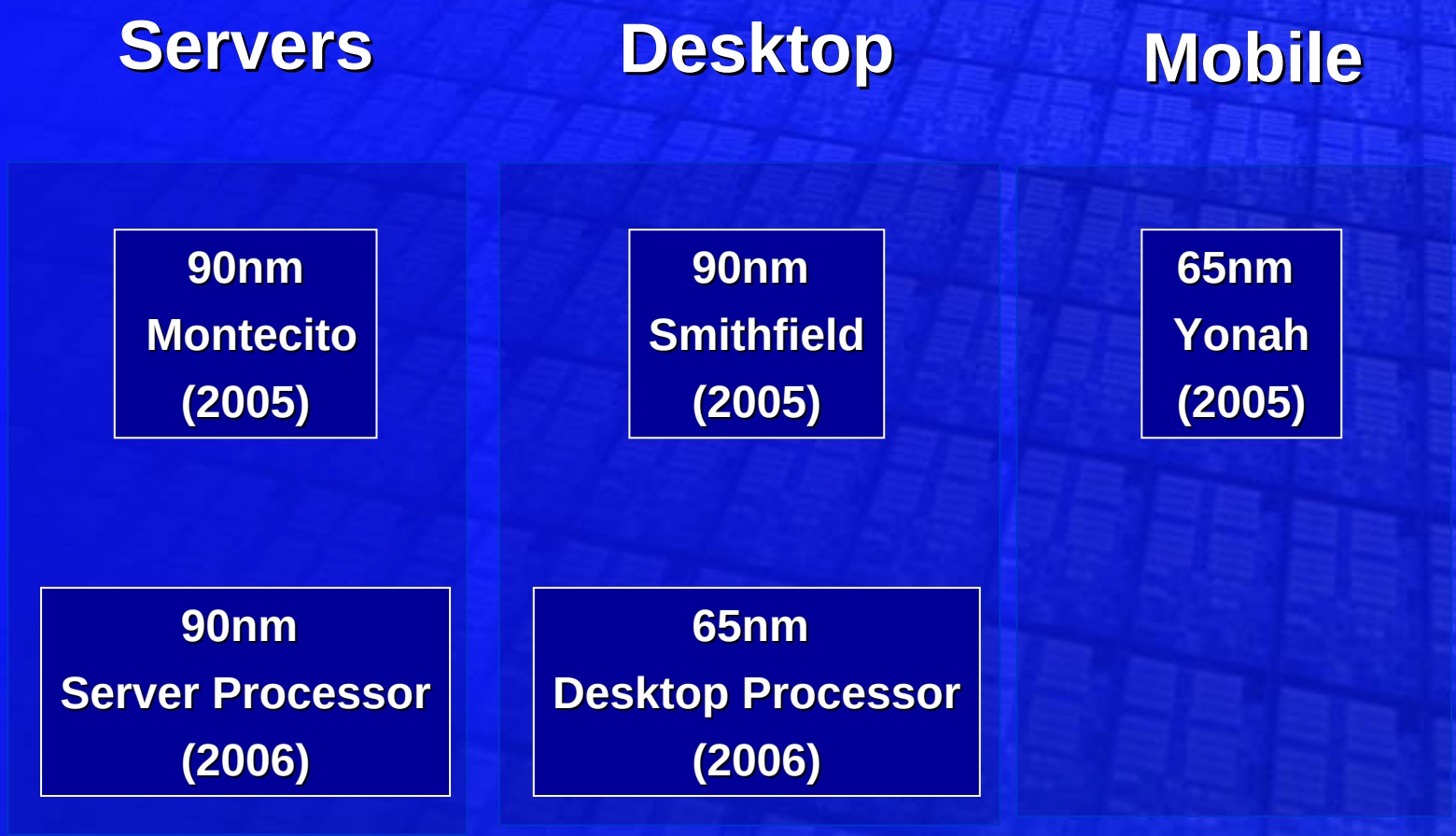


*Average of SPECInt2000 and SPECFP2000 rates for Intel desktop processors vs initial Intel® Pentium® 4 Processor

Source: Intel

Multi-Core Parallelism Going Mainstream

Dual-Core Processor Plans (Intel)



Source: Intel

Key Points

- Moore's Law thriving after 40 years
- Convergence drives IC industry growth
- Integrated platforms optimize user experience
- Multi-core parallelism going mainstream
- Holistic solutions deliver power efficiency

Silicon Technology Changes to Increase Power Efficiency

1960's: Bipolar

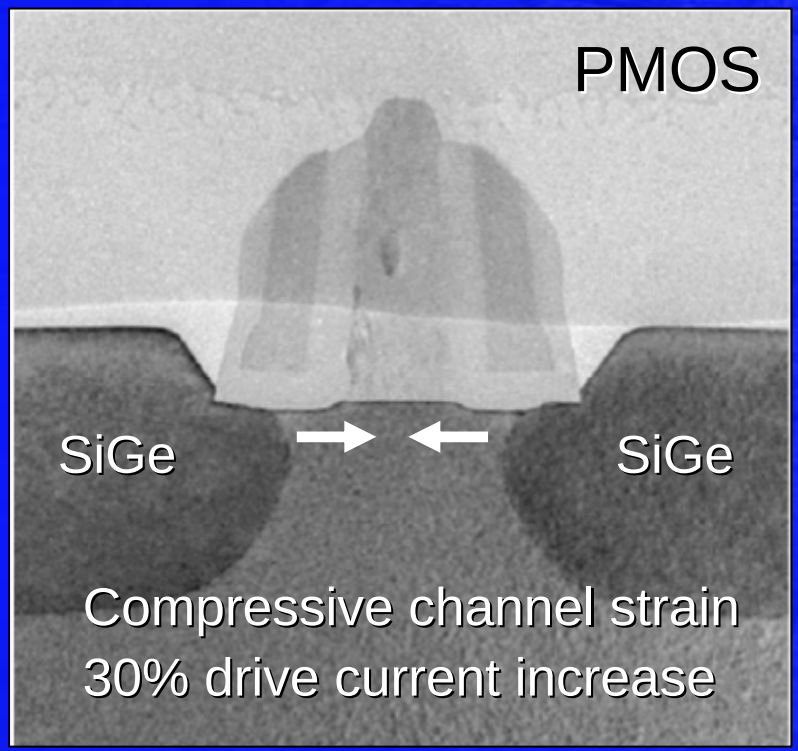
1970's: PMOS, NMOS

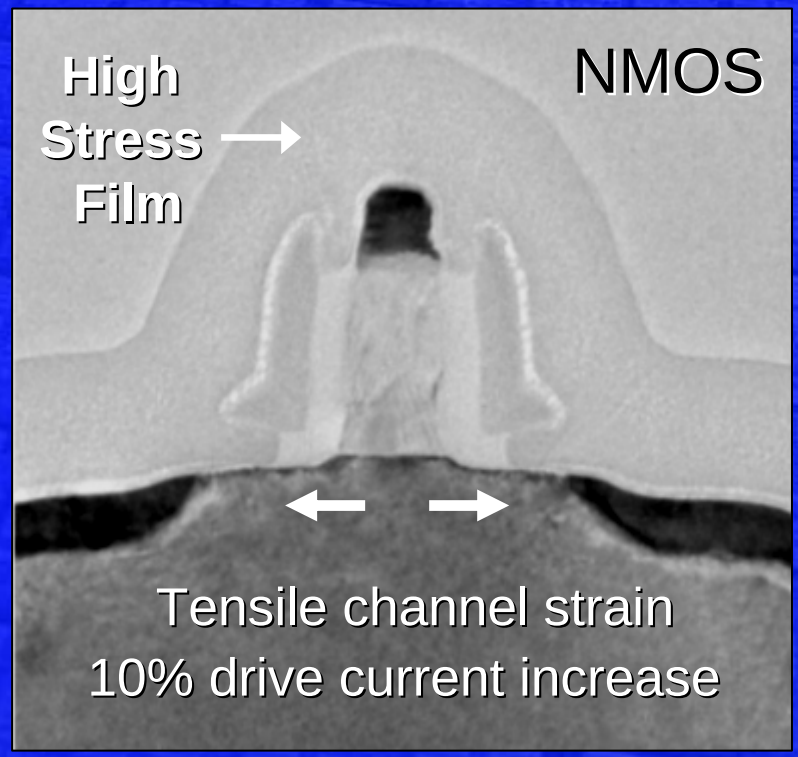
1980's: CMOS

1990's: Voltage scaling ($P = CV^2f$)

2000's: Power efficient scaling/design

Power Efficient 90nm Transistors with Strained Silicon

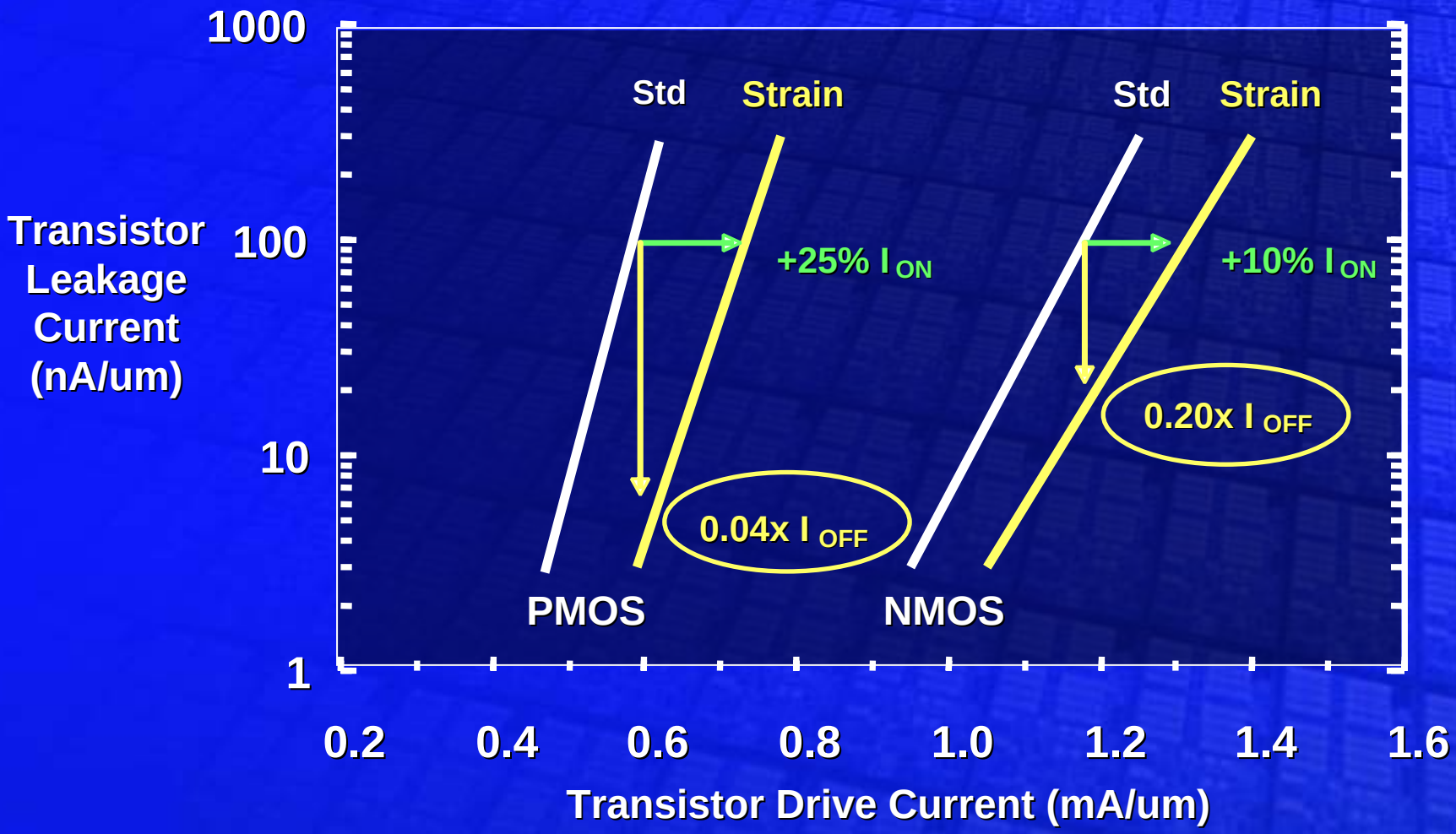




Innovate and integrate for cost effective production

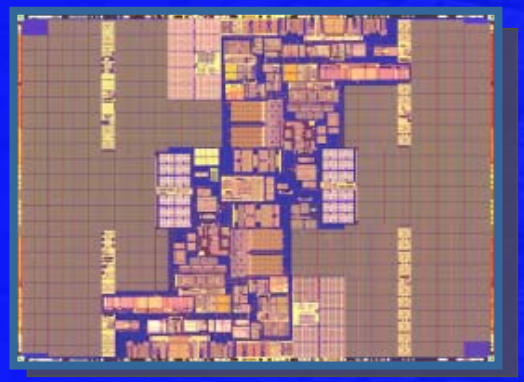
Source: Intel

Strained Silicon Improves Transistor Performance and/or Reduces Leakage

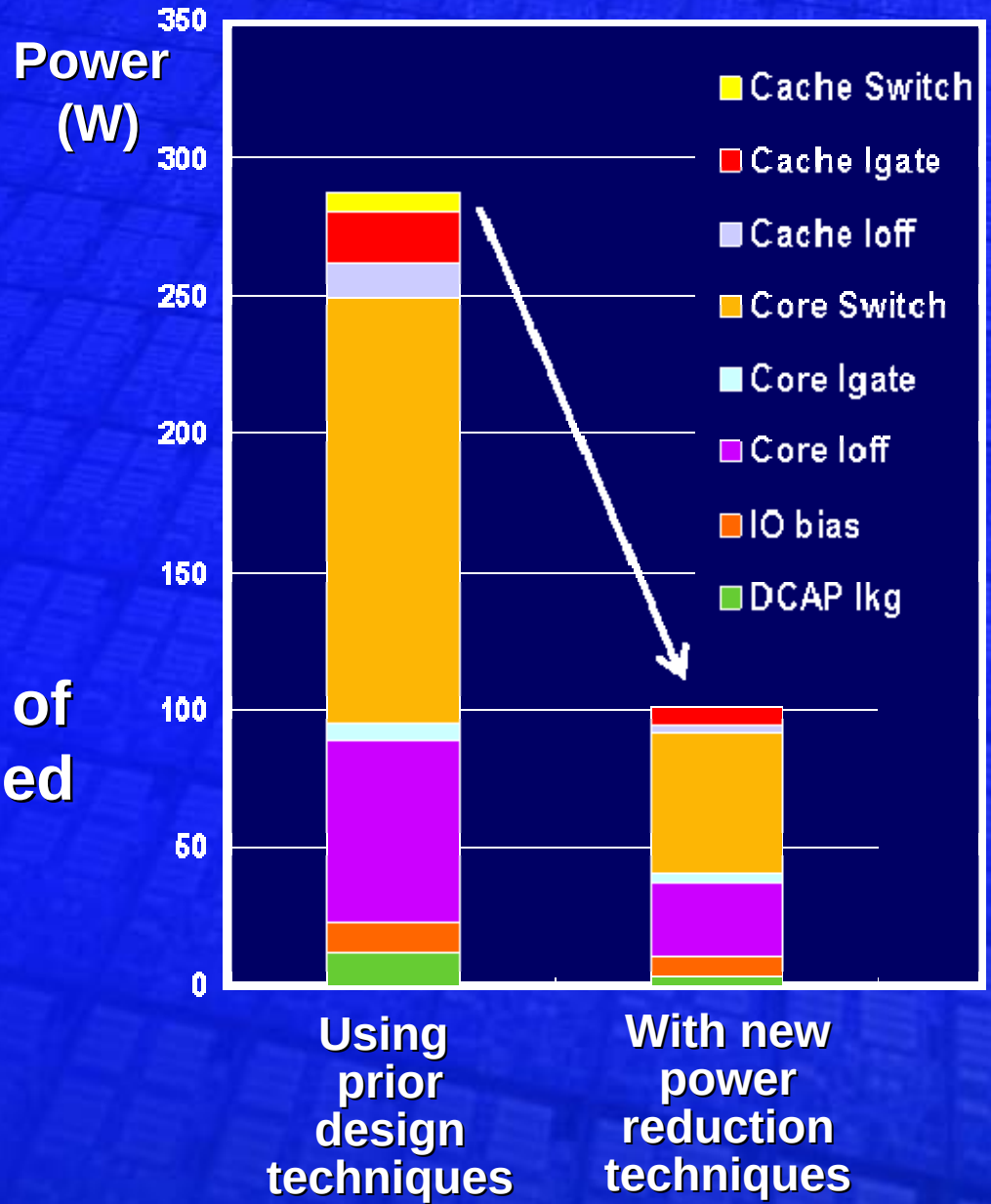


Source: Intel

Advances in Power Efficient Design

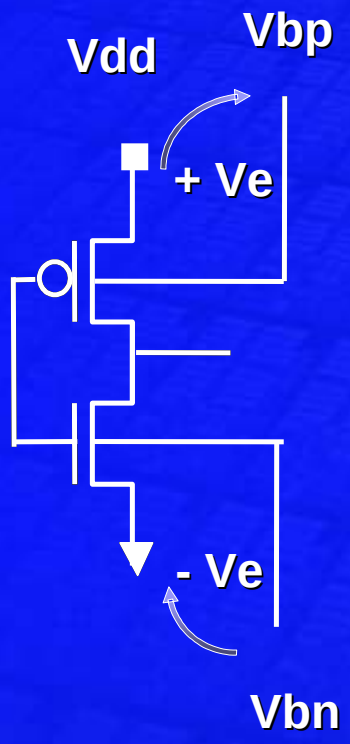


ISSCC 2005 P10.1
"The Implementation of a 2-core Multi-Threaded Itanium™ Family Processor"

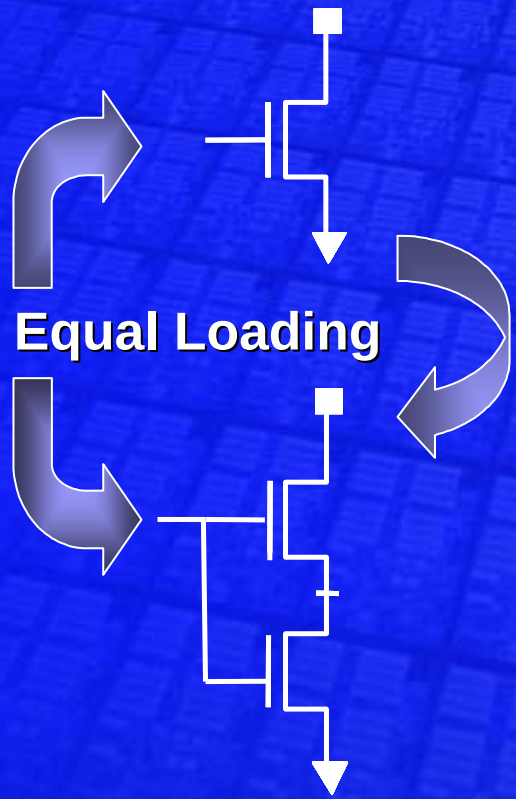


Circuit Techniques Reduce Source Drain Leakage

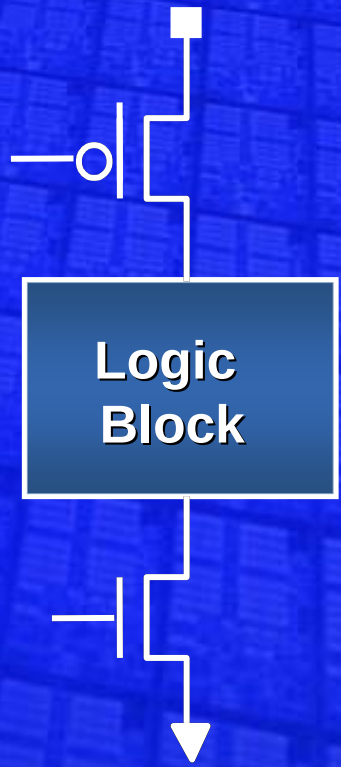
Body Bias



Stack Effect

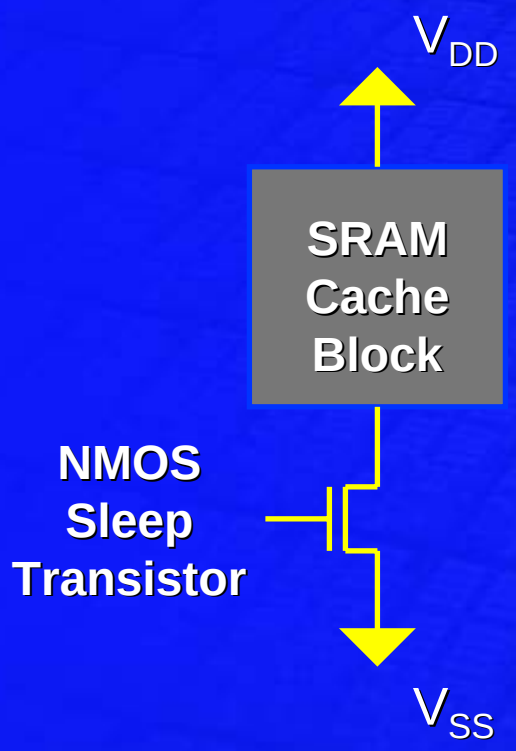


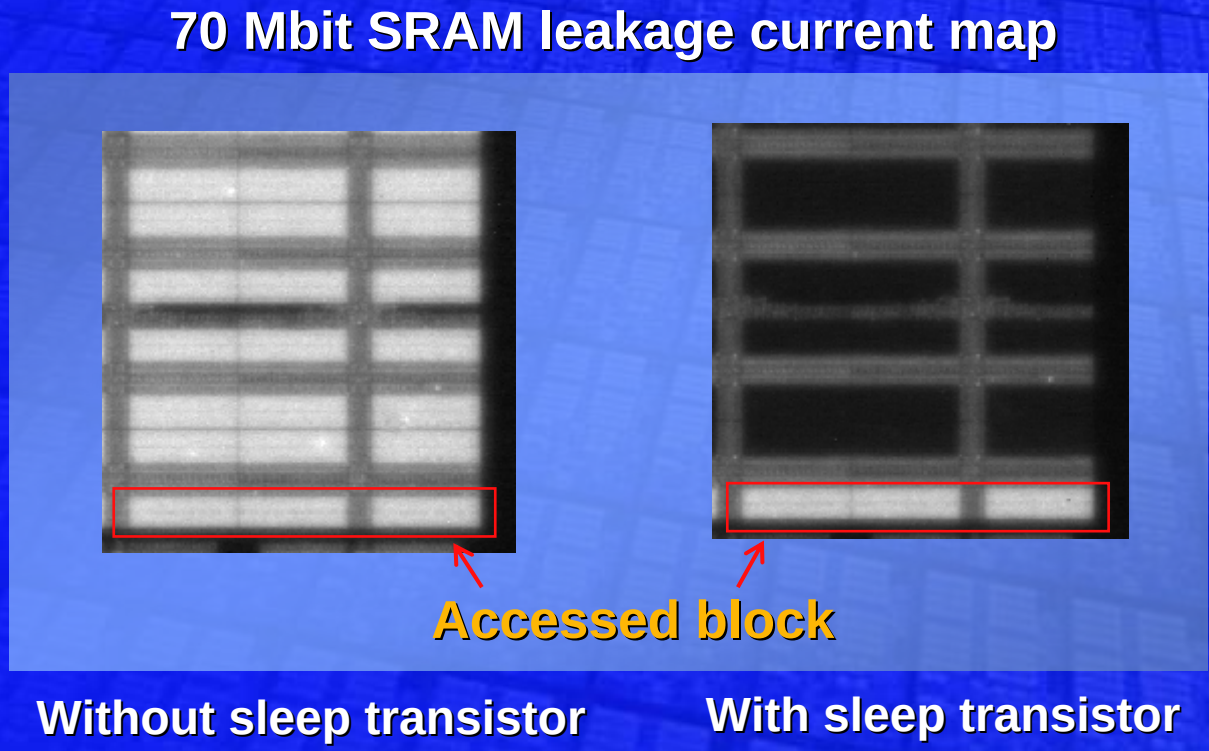
Sleep Transistor



Leakage Reduction	2 - 10X	2 - 10X	2 - 1000X

Sleep Transistor Reduces SRAM Leakage Power

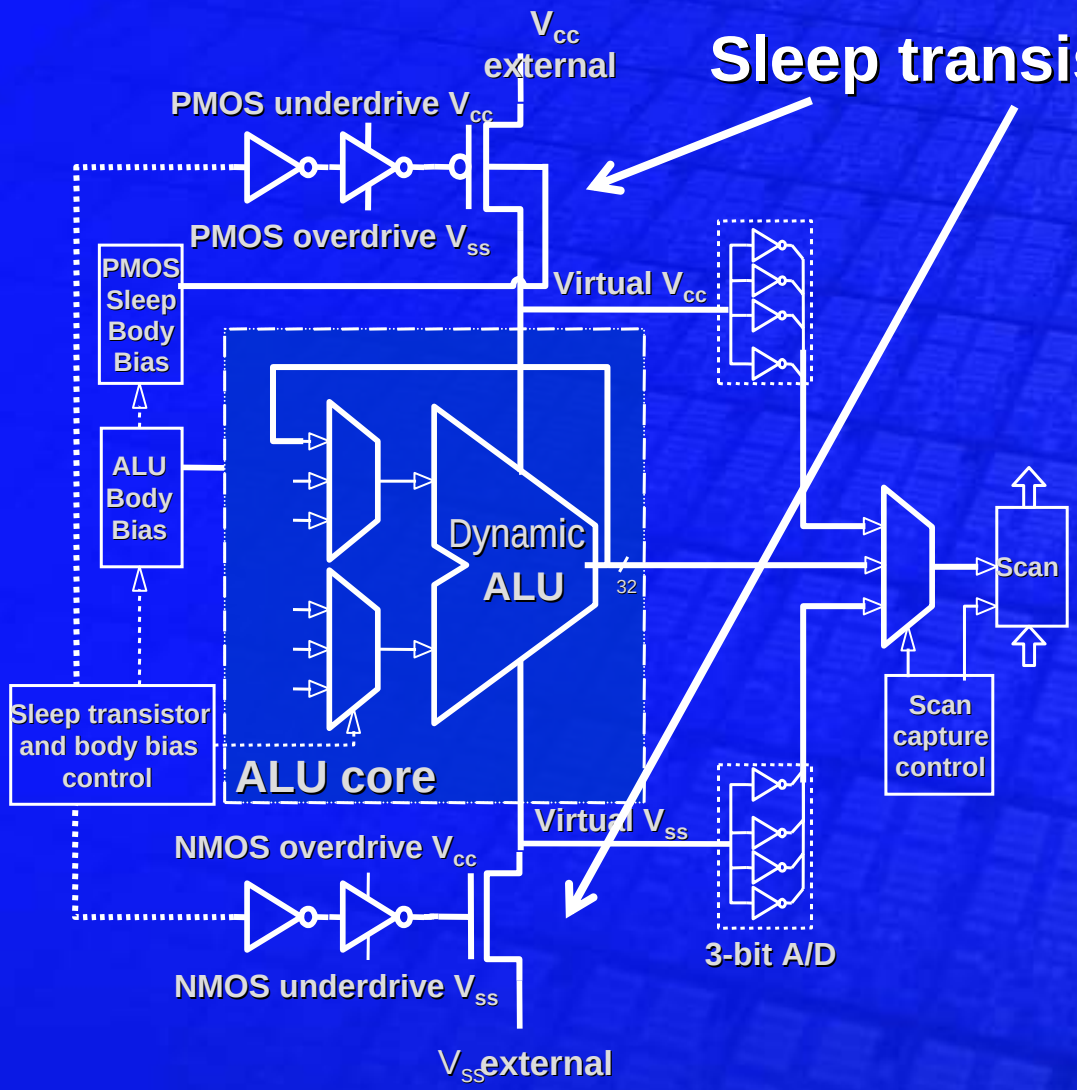


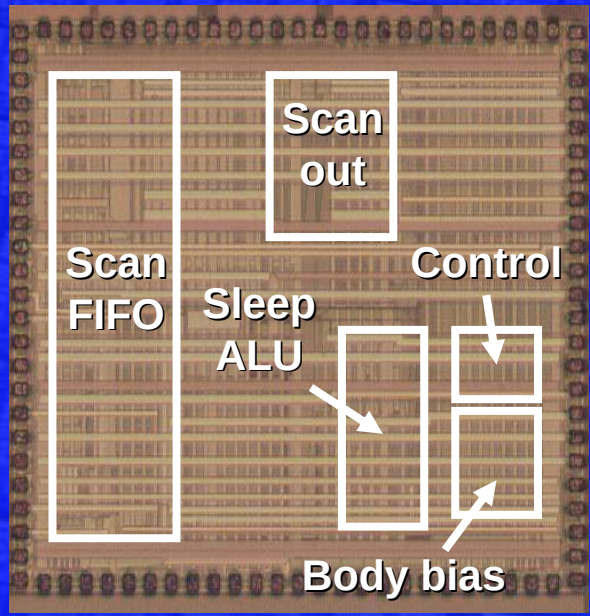


>3x SRAM leakage reduction on inactive blocks

Source: Intel

Sleep Transistors Reduce ALU Leakage





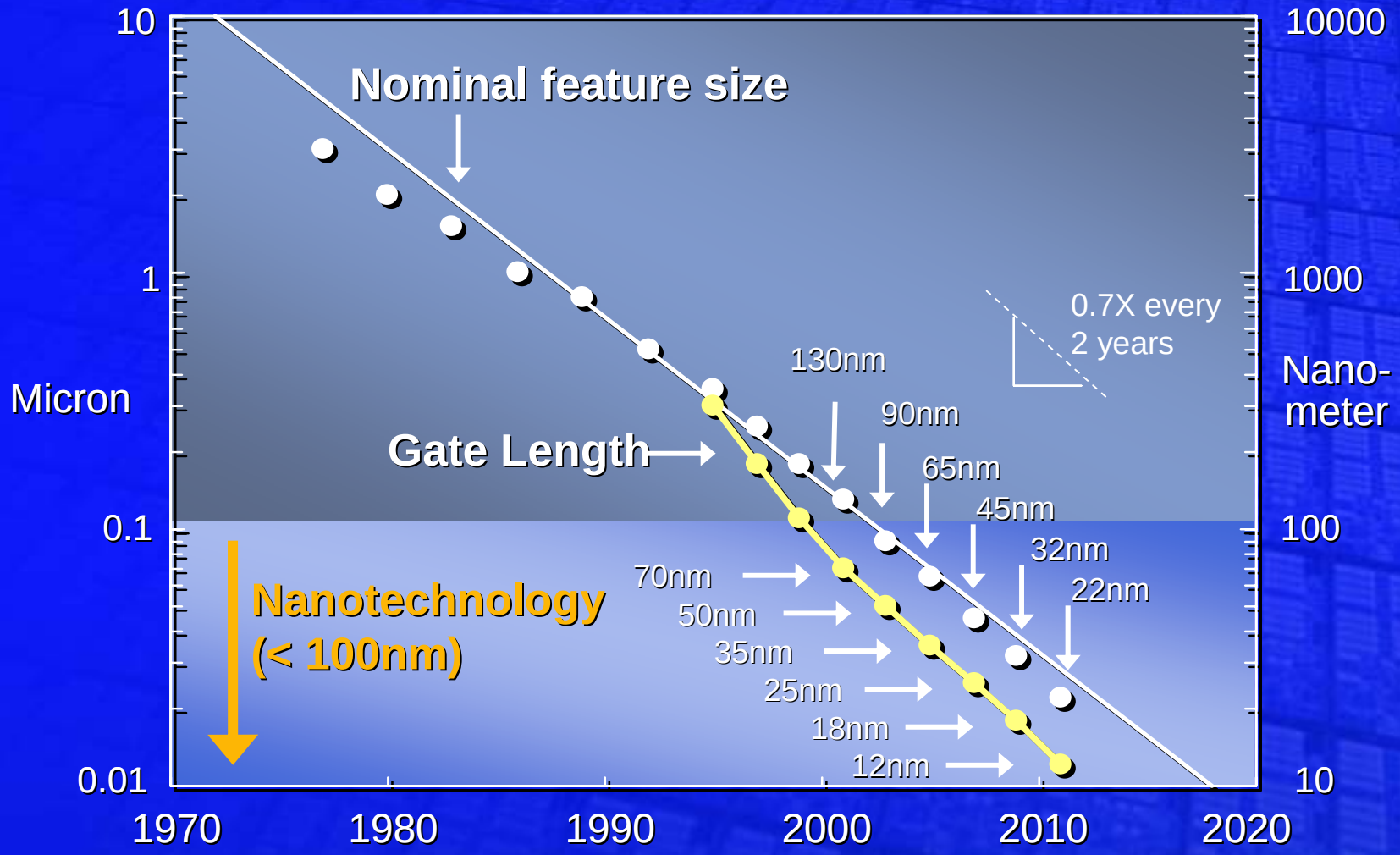
37X leakage reduction demonstrated on test chip

Source: ISSCC 2003, Paper 6.1

Key Points

- Moore’s Law thriving after 40 years
- Convergence drives IC industry growth
- Integrated platforms optimize user experience
- Multi-core parallelism going mainstream
- Holistic solutions deliver power efficiency
- Nanotechnology will extend IC advances
- Lithography innovations remain vital

Silicon Technology Reaches Nanoscale



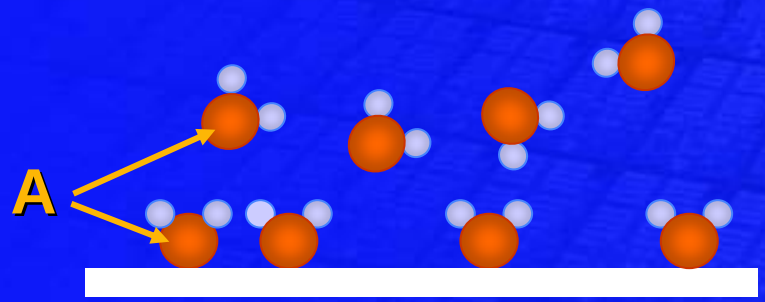
Source: Intel

Nanotechnology Hallmarks (For Nanoelectronics)

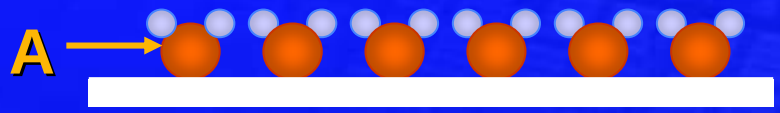
- Structures measured in nanometers
  - Less than 0.1-micron (100nm)
- New processes, materials, device structures
  - Incrementally changing silicon technology base
- Materials manipulated on atomic scale
  - In one or more dimensions
- Increasing use of self-assembly
  - Using chemical properties to form structures

Nanotechnology innovations will extend silicon technology and Moore's Law

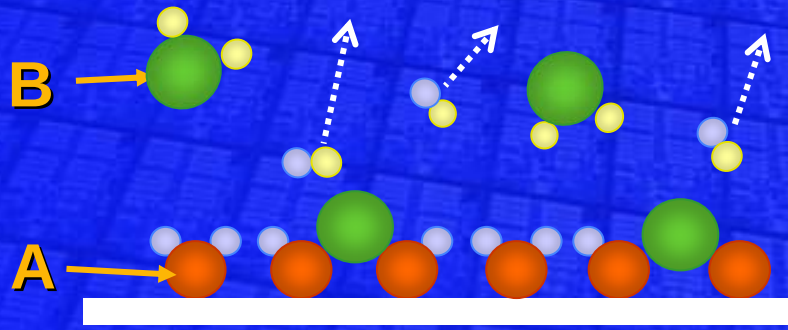
Design Your Own Film with Atomic Layer Deposition (ALD)



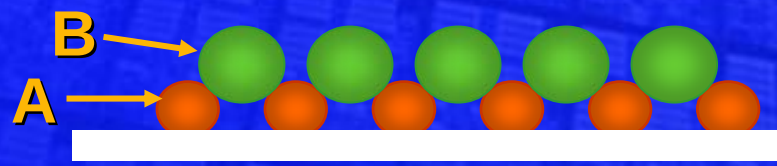
Step 1



Step 2



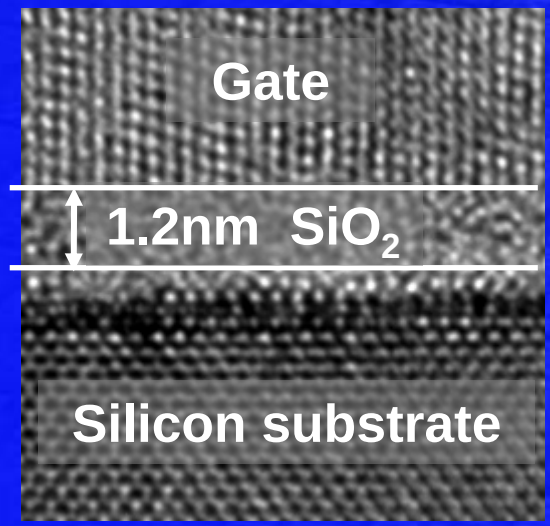
Step 3

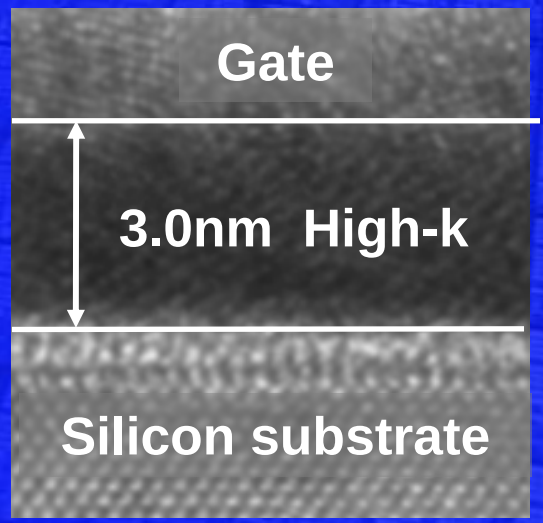


Step 4

Atomic level manipulation + Self-assembly

ALD Enables High-k Dielectric to Reduce Gate Leakage





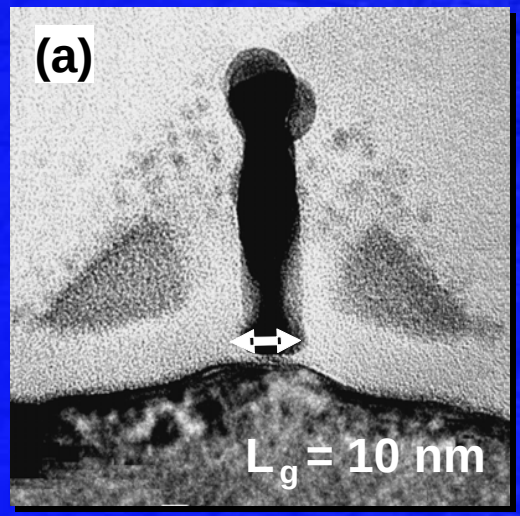
	High-k vs. SiO_2	Benefit
Gate capacitance	60% greater	Faster transistors
Gate dielectric leakage	> 100x reduction	Lower power

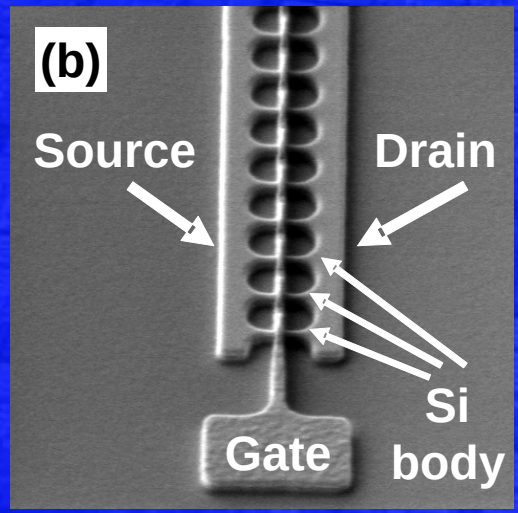
Process integration is the key challenge

Source: Intel

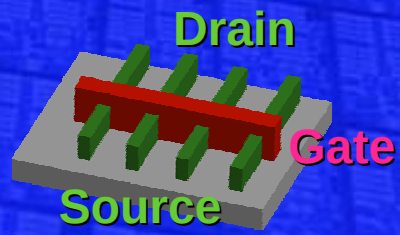
Nanostructures for the Next Decade (Transistor Research at Intel)

Si Device Miniaturization

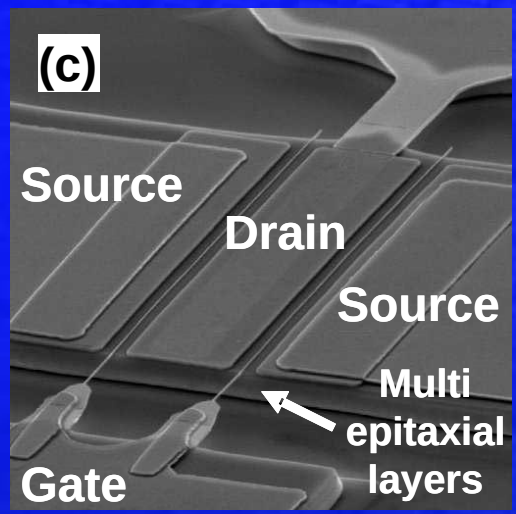


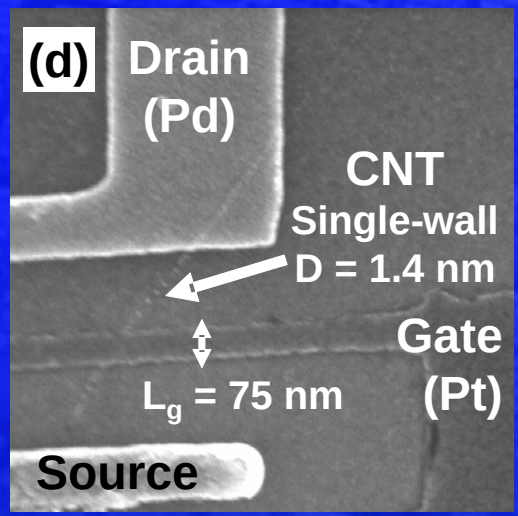


Non-planar Tri-Gate Architecture

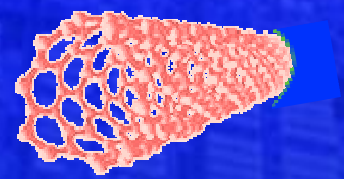


III-V Device Research



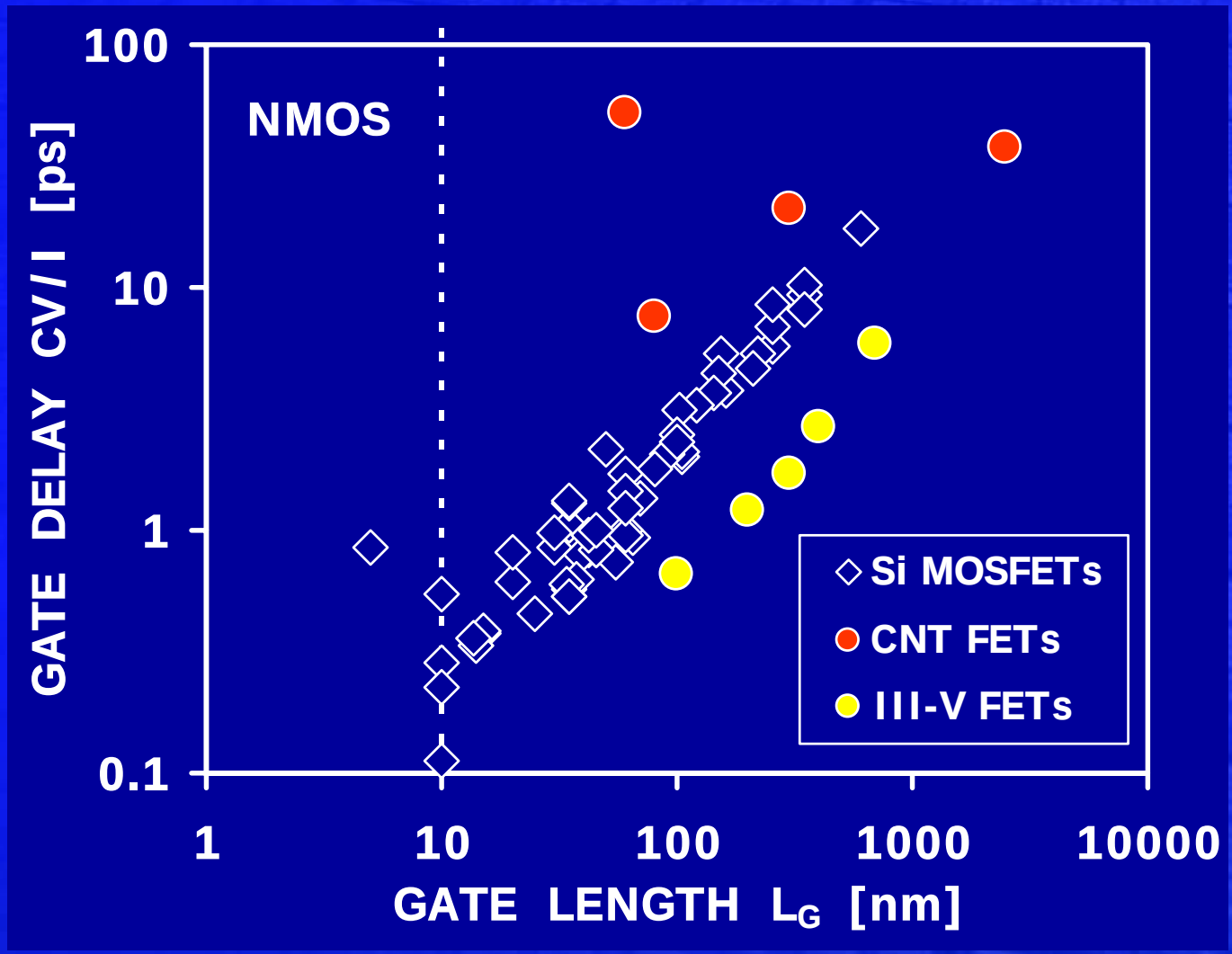


Carbon Nanotube Transistor



Source: Intel

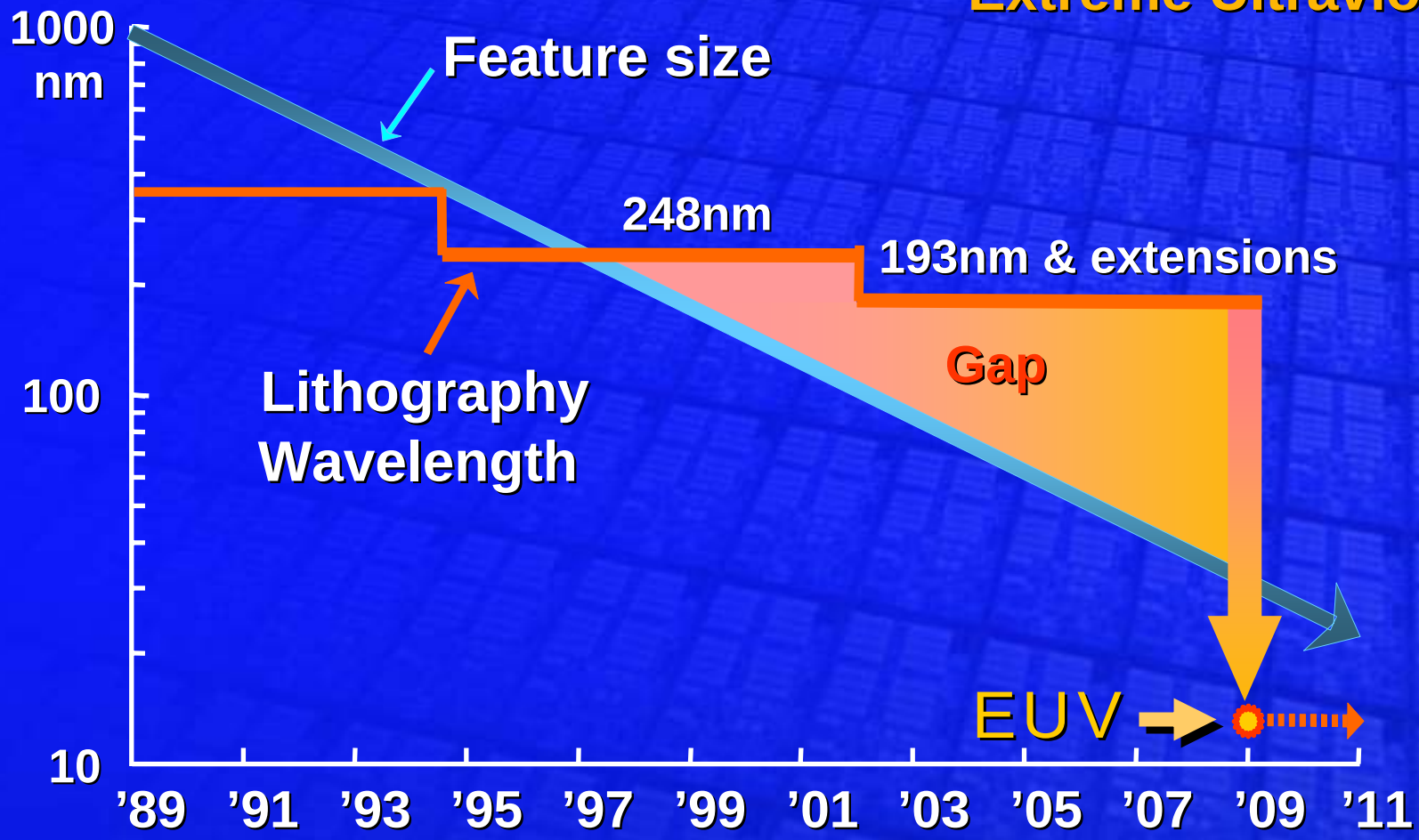
Benchmarking Nanotransistor Progress



Source: Intel compilation of published data

Lithography Must Break Through to Shorter Wavelength (EUV* @ 13.5nm)

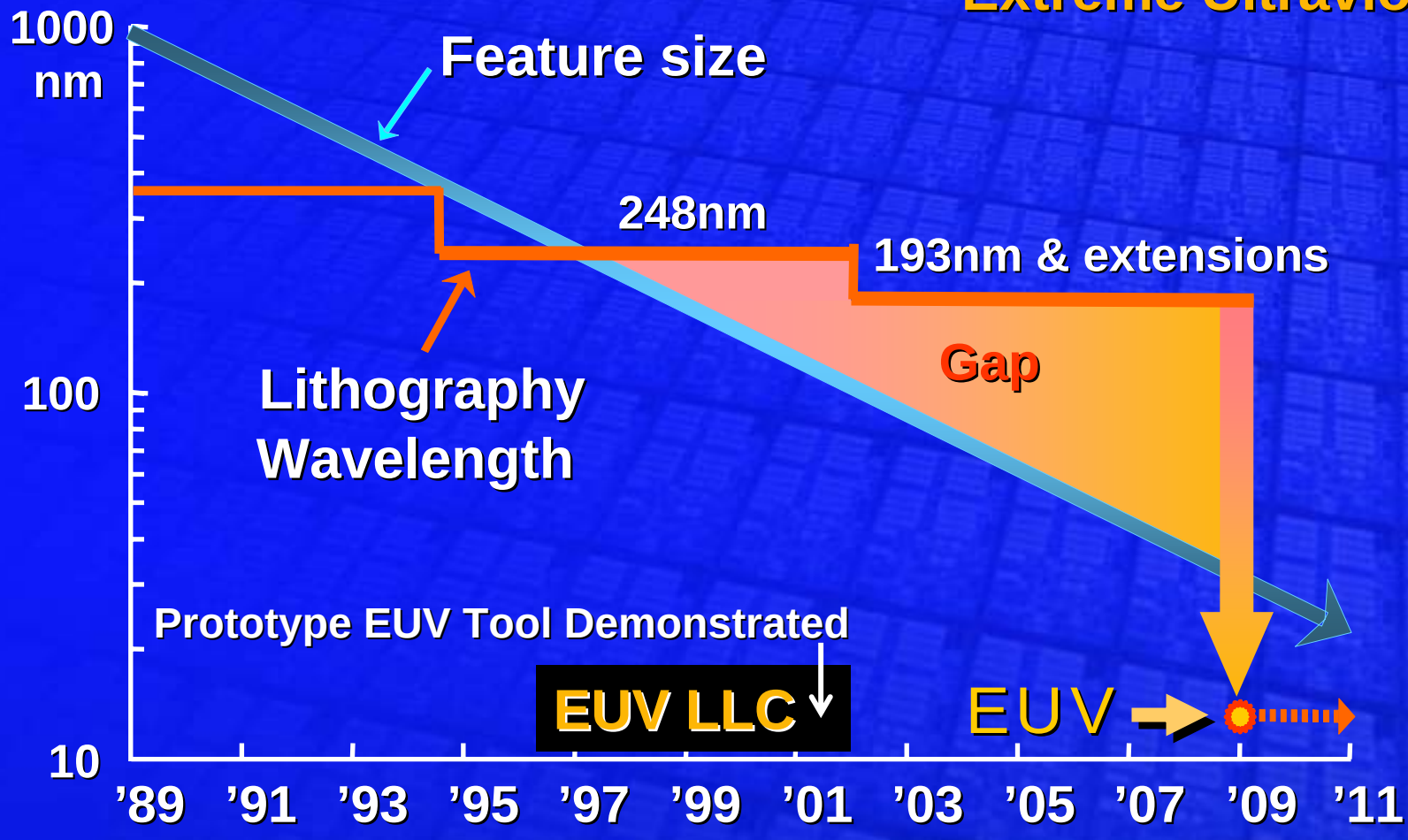
* Extreme Ultraviolet



Source: Intel

Lithography Must Break Through to Shorter Wavelength (EUV* @ 13.5nm)

* Extreme Ultraviolet

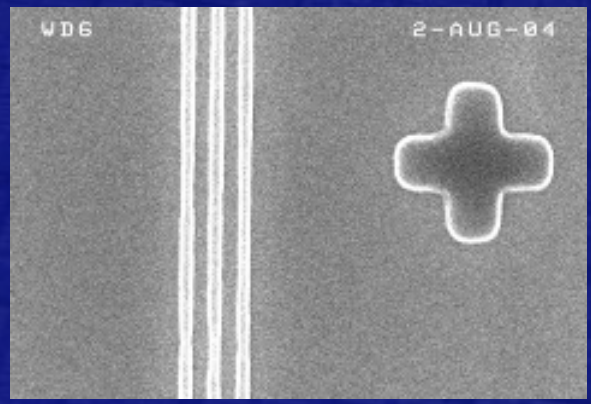


EUV LLC invested heavily to spur innovation

Source: Intel

EUV Lithography in Commercial Development

EUV Micro exposure tool (MET)



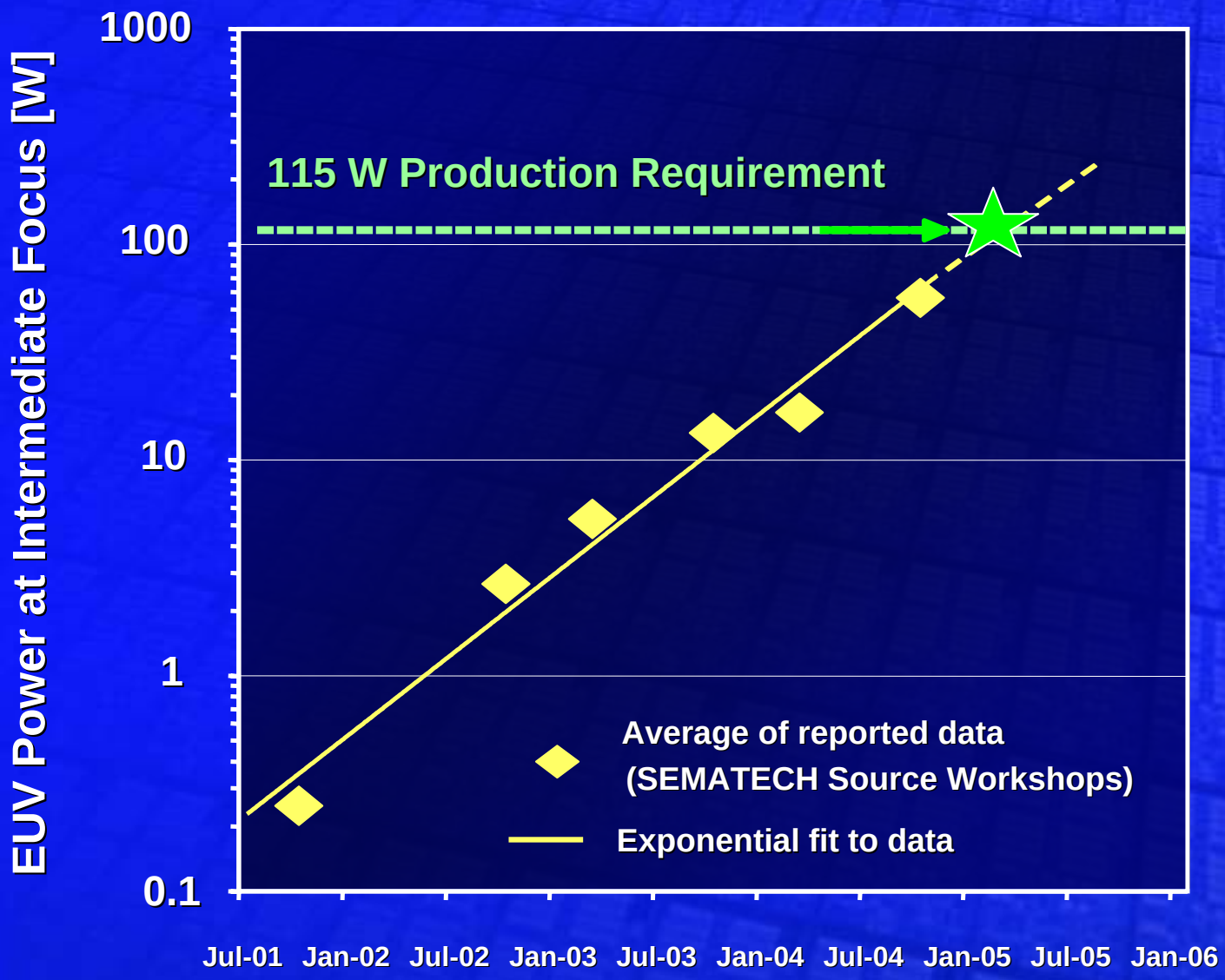
EUV MET Image (8/04)

Integrated development in progress

- Source power and lifetime
- Defect free mask fabrication and handling
- Optics lifetime
- Resist performance

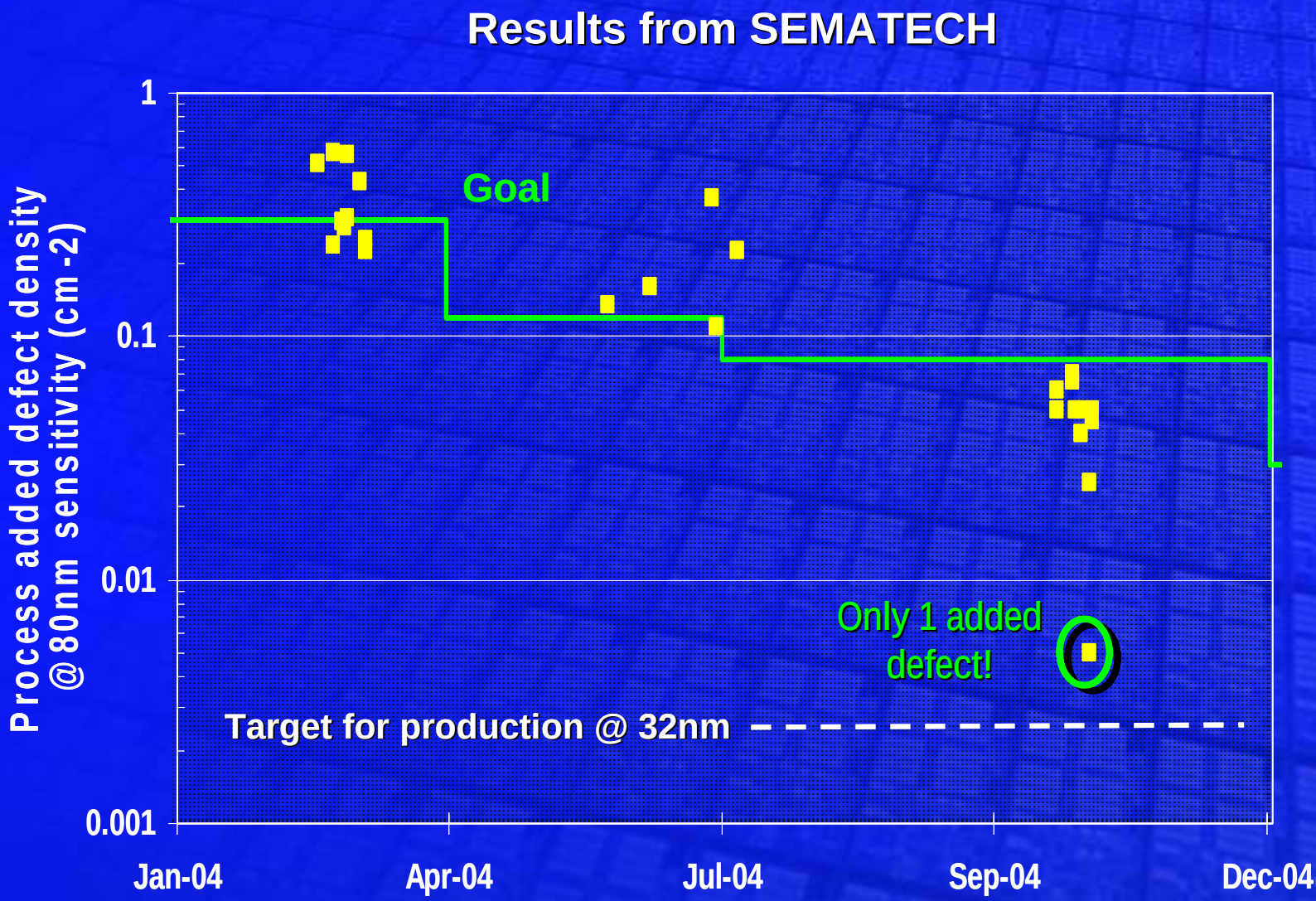
Source: Intel

EUV Source Power Increased



Source: SEMATECH

EUV Mask Blank Defects Reduced

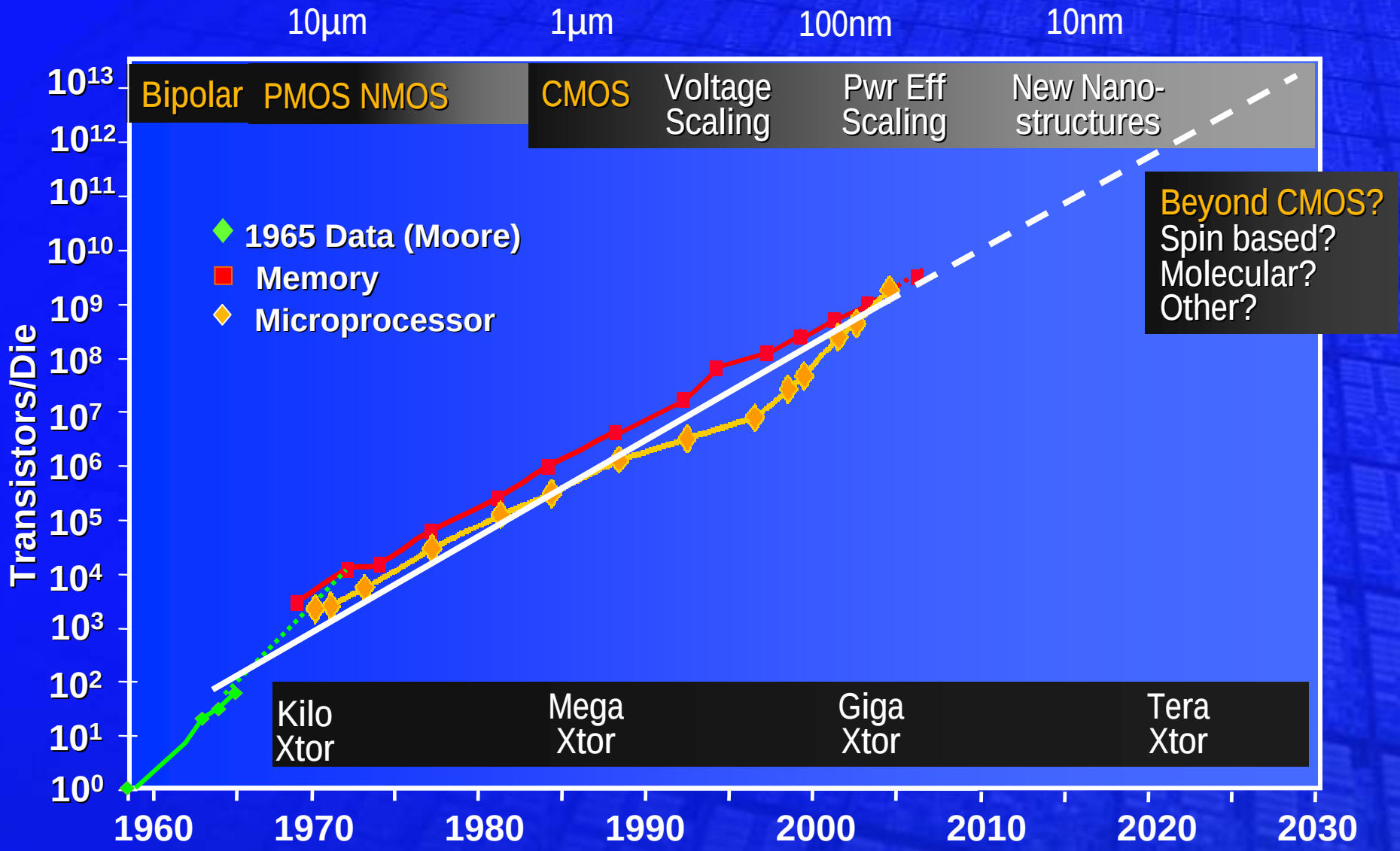


Source: SEMATECH

Key Points

- Moore's Law thriving after 40 years
- Convergence drives IC industry growth
- Integrated platforms optimize user experience
- Multi-core parallelism going mainstream
- Holistic solutions deliver power efficiency
- Nanotechnology will extend IC advances
- Lithography innovations remain vital
- **Moore's Law will outlive CMOS**
- **Future rides on innovation and integration**

Moore's Law Will Outlive CMOS



Innovation and Integration Will Sustain Moore's Law

Innovation		Integration
Identify needs and create capabilities that drive growth	→	Deliver platforms to optimize user experience
Anticipate barriers and seek timely breakthroughs	→	Integrate new materials, devices, processes
Make strategic technology transitions	→	Coordinate strategic shifts across industry

Key Points

- Moore's Law thriving after 40 years
- Convergence drives IC industry growth
- Integrated platforms optimize user experience
- Multi-core parallelism going mainstream
- Holistic solutions deliver power efficiency
- Nanotechnology will extend IC advances
- Lithography innovations remain vital
- Moore's Law will outlive CMOS
- Future rides on innovation and integration