Wide Range Work Function Modulation of Binary Alloys for MOSFET Application

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***Abstract*—This paper explores the characteristics of the binary alloys Ta–Pt and Ta–Ti for gate electrode application. With a proper composition of high and low work function metals, the work function of the metal alloys can be modulated from 4.16 eV to 5.05 eV continuously. The alloys show good thermal stability and inner chemical activity on both silicon dioxide and hafnium dioxide. Thermal stress generated from the alloy film increases interface state density and hence effective oxide charges. This problem can be greatly reduced with W/Ta–Pt stack structure, where W acts as the main conducting metal and Ta–Pt acts as work function control metal. All of these properties make them suitable for use in all device applications.**

***Index Terms*—Alloy, metal gate, work function.**

I. Introduction

As MOS devices are scaled down, the gate oxide thickness will decrease to be thinner than 2 nm. Several problems were observed together with the thin down of gate oxide such as poly-Si gate depletion, boron penetration, quantum effect, and gate leakage current [1]–[4]. Using metal to replace poly-Si as gate electrode can solve the first two problems [5], [6]. However, to fabricate surface channel devices with suitable threshold voltage (V_{th}), the gate electrode should have suitable work function (Φ_m), i.e., metals with $\Phi_m \sim 4.0$–4.2 eV and $\Phi_m \sim 5.0$–5.2 eV are suitable for NMOSFETs and PMOSFETs, respectively. It was reported that the Φ_m of metal nitrides could be modulated with the nitrogen content [7]–[9]. Unfortunately, the magnitude of modulation is not wide enough. Recently, metal alloys were proposed for work function modulation [10], [11]. However, the Φ_m drops abruptly once new alloy phase forms. Ni–Ti inter-diffusion was also proposed to produce dual work function metal gate [12], but the thermal stability is poor.

In this work, we propose a new Ta-based binary alloy system of Ta–Pt and Ta–Ti. Wide range and continuous Φ_m modulation from 4.16 eV to 5.05 eV could be achieved.

II. Experiments

A simple MOS structure was fabricated to characterize the binary alloy systems. The starting material was (100)-oriented phosphorus doped Si wafer. Following standard RCA cleaning, gate oxide of 11-nm-thick was thermally grown. The gate electrodes were patterned using the liftoff process. Ta_xPt_y and Ta_xTi_y alloys were cosputtered to a thickness of 60 nm on patterned photoresist. Table I lists the deposition conditions and the atomic composition analyzed with Rutherford Backscattering Spectroscopy (RBS). After gate patterning, samples were annealed in N_2 ambient at 400, 500, and 600 °C for 30 min followed by Al deposition at the back.

III. Results and Discussion

The work function of an A_xB_{1-x} alloy can be approximately expressed as

$$\begin{aligned}\Phi_m &= x\Phi_{m,A} + (1-x)\Phi_{m,B} \\ &\quad + x(1-x)\left[\frac{(\Phi_{m,A}-\Phi_{m,B})(\rho_A-\rho_B)}{x\rho_A+(1-x)\rho_B}\right] \\ &= x\Phi_{m,A} + (1-x)\Phi_{m,B} \\ &\quad + x(1-x)\left[\frac{(\Phi_{m,A}-\Phi_{m,B})(\frac{\rho_A}{\rho_B}-1)}{x\frac{\rho_A}{\rho_B}+(1-x)}\right]\end{aligned}$$

where $\Phi_{m,A}$ and $\Phi_{m,B}$ are the pure constituent work functions of A and B, respectively, and ρ_A and ρ_B are the pure constituent total densities of states [14]. The density of states at Fermi energy $\rho(\varepsilon_F)$ is proportional to the electronic specific heat constant $C_e = (1/3)\pi^2\rho(\varepsilon_F)k_B^2T$, where k_B is Boltzmen constant and T is temperature. In the case of $C_{e,A}/C_{e,B} \sim 1$, the Φ_m changes with x linearly as $\phi(x) = \phi_B + x(\phi_A - \phi_B)$ [15]. The C_e values of Pt, Ta, and Ti are 6.8, 5.9, and 3.35 mJ/mole/K^2, respectively [16]. Since the C_e values of Ta and Pt are very close, a nearly linear correlation can be expected.

The approximate work function $(\Phi_{m,app})$ of annealed samples was extracted by comparing the measured capacitance–voltage $(C$–$V)$ curves with the theoretical C–V curve [9], [13]. The $\Phi_{m,app}$ is defined as $\Phi_{m,app.} = \Phi_m$–Q_{ss}/C_{ox}, where Q_{ss} is effective oxide charges and C_{ox} is capacitance at accumulation mode. As the gate oxide thickness is 11 nm, a Q_{ss} of 1×10^{11} cm^{-2} results in a Φ_m deviation of 0.05eV only. Fig. 1 shows the extracted $\Phi_{m,app}$ of 400 °C annealed samples. The Q_{ss} of poly-Si gate devices is around 5×10^{10} cm^{-2}. The Q_{ss} of metal gate devices might be higher than that of poly-Si gate. However, since the interface state density (D_{it}) of metal gate devices is similar to that of poly-Si gate, it is believed that the Q_{ss} of metal gate will not be much higher than that of poly-Si gate. Therefore, the $\Phi_{m,app}$ should be very close to the Φ_m. With increasing contents of high Φ_m elements, Pt in Ta–Pt alloys or Ta in Ta–Ti alloy, the $\Phi_{m,app}$ shifts toward higher value. The $Ta_{0.63}$ $Ti_{0.37}$ alloy and $Ta_{0.58}Pt_{0.42}$ alloy

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TABLE I
DEPOSITION CONDITIONS USED IN THIS WORK AND ATOMIC COMPOSITIONS OF ALLOYS ANALYZED WITH RBS

Sample ID	Sputtering Power (W)			Atomic Ratio (%)		
	Ta	Pt	Ti	Ta	Pt	Ti
A1	50	0	50	63	0	37
A2	150	0	0	100	0	0
A3	100	30	0	74	26	0
A4	50	30	0	65	35	0
A5	30	30	0	58	42	0
A6	0	30	0	0	100	0

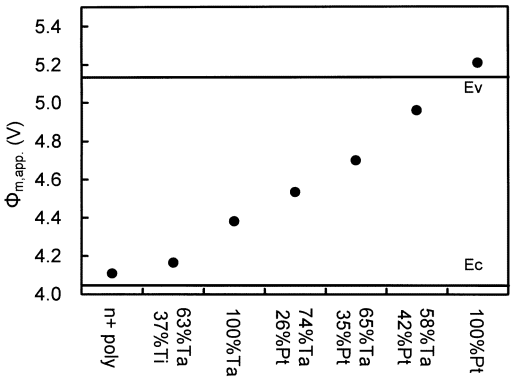

Fig. 1. Extracted approximate work function ($\Phi_{m,\,app,}$) of 400 °C annealed samples.

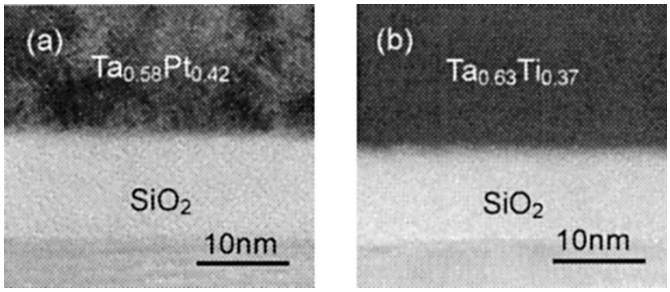

Fig. 2. Cross-sectional TEM micrographs of (a) $Ta_{0.58}Pt_{0.42}/SiO_2$ structure and (b) $Ta_{0.63}Ti_{0.37}/SiO_2$ structure after annealing in N_2 ambient for 30 minutes at 600 °C. No Interfacial reaction are observed.

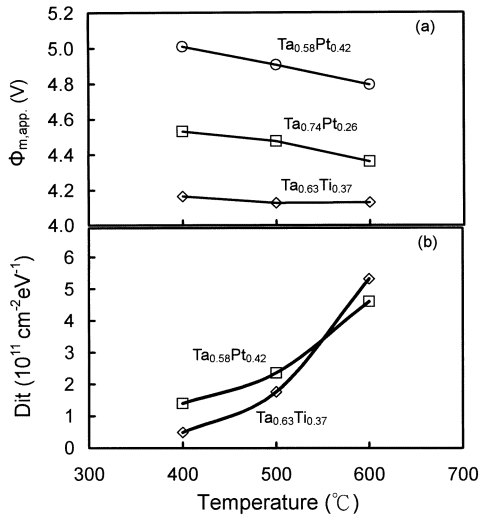

Fig. 3. (a) Approximate work function ($\Phi_{m,\,app}$) and (b) interface state density (D_{it}) versus annealing temperatures.

show $\Phi_{m,\,app}$ of about 4.16 eV and 5.05 eV and is suitable for NMOSFETs and PMOSFETs, respectively. As expected, the $\Phi_{m,\,app}$ can be modulated continuously by adjusting the atomic composition of the alloy. This property allows for the use of the alloy system to obtain precise work function. For example, fully-depleted SOI devices require Φ_m of close to 4.6 eV [17], and can be achieved using the alloys with Ta/Pt ratio close to 0.74/0.26.

Fig. 2(a) and (b) show the Transmission Electron Microscopic (TEM) micrographs of $Ta_{0.58}Pt_{0.42}/SiO_2$ and $Ta_{0.63}Ti_{0.37}/SiO_2$ structures after annealing at 600 °C, respectively. The alloys are almost amorphous and no interfacial layer was formed. Furthermore, no compound phases were observed from the X-ray diffraction (XRD) spectrums. The change of EOT after annealing at 600 °C is less than 1%, i.e., less than 0.1 nm. These results imply that the alloys are thermally stable up to 600 °C on SiO_2. This temperature is high enough for replacement gate process and is better than most of low work function elemental metals such as Ti [18].

Fig. 3(a) shows that the $\Phi_{m,\,app}$ decreases slightly with the increase of annealing temperature. Since the alloys are thermally stable on SiO_2, this phenomenon cannot be attributed to the interaction between alloy and oxide. Fig. 3(b) shows that the D_{it} also increases with the increase of annealing temperature. It is thus postulated that the decrease of $\Phi_{m,\,app}$ comes from the thermal stress generated oxide charges. To reduce the effect of thermal stress, a stack gate electrode of W(50 nm)/Ta–Pt(10 nm) is proposed. The thermal expansion coefficient of W (4.4×10^{-6} °C^{-1}) is lower than that of Pt (9.0×10^{-6} °C^{-1}) and Ta (6.6×10^{-6} °C^{-1}) and is close to that of Si (2.4×10^{-6} °C^{-1}). Another benefit of using stack structure is that the resistivity of W (5.3×10^{-6} Ω-cm) is much lower than the resistivity of alloys ($>300 \times 10^{-6}$ Ω-cm). In this structure, the Ta–Pt alloy determines the work function and the W layer serves as the main conducting material.

Fig. 4 shows the C–V characteristics of W(50 nm)/Ta–Pt(10 nm)/HfO_2(5 nm)/p-type Si structure after annealing at 600 °C and 800 °C in N_2 ambient for 30 min. The apparent kink in the curve of 600 °C annealed sample points to the insufficient

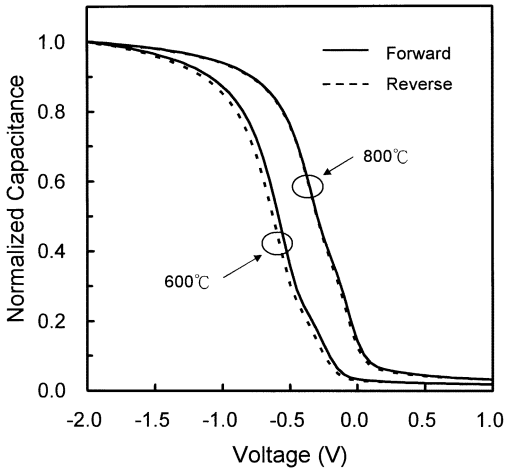

Fig. 4. C–V characteristic of the $Ta_{0.58}Pt_{0.42}/HfO_2$/p-Si sample after annealing at 600 °C and 800 °C in N_2 ambient for 30 minutes.

passivation of interface states at the HfO_2/Si interface. The smaller kink and negligible hysteresis phenomenon of the 800 °C annealed sample imply that the stack structure is stable up to 800 °C. The reduction of kink and hysteresis also confirms that thermal stress can be reduced by the stacked metal gate. The flatband voltage difference between 600 and 800 °C annealed devices may be attributed to the reduction of Q_{ss} and/or the change of Φ_m due to interaction between W and Ta–Pt or between Ta–Pt and HfO_2. A 900 °C annealing distorts the C–V characteristic. The stability of metal gate/high-K dielectric system is under investigation.

IV. Conclusion

This work explores the characteristics of the binary alloys Ta–Pt and Ta–Ti for gate electrode application. With a proper composition of high and low work function metals, the work function of the metal alloys can be modulated from 4.16 eV to 5.05 eV continuously. The resistivity of Pt–Ta alloy is high and thermal stress of thick Ta–Pt alloy may generate oxide charges. Therefore, stack structure with a low resistivity and low stress layer as main conducting layer and the proposed alloy layer as work function control layer, for example W/Ta–Pt, is preferred for actual application.

To implement metal gate into CMOS process is tough not only for alloy gates. Metal gates for NMOS and PMOS can be patterned separately [19]. Using metal ion implantation to form various alloys is another choice; it depends on the maturity of metal ion implantation technology. However, gate electrode with work function near mid-gap of Si should be used for FD-SOI. The proposed alloy system shows the advantage of precise work function control in this aspect.

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