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Innovative devices for integrated circuits – A design perspective

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ABSTRACT

MOS devices go 3D, new quantum effect devices appear in the research labs. This paper discusses the impact of various innovative device architectures on circuit design. Examples of circuits with FinFETs or Multi-Gate-FETs are shown and their performance is compared with classically scaled CMOS circuits both for digital and analog applications. As an example for novel quantum effect devices beyond CMOS we discuss circuits with Tunneling Field Effect Transistors and their combination with classical MOSFETs and MuGFETs. Finally the potential of more substantial paradigm changes in circuit design will be exploited for the example of magnetic quantum cellular automata using a novel integrated magnetic field clocking scheme.

1. Introduction

As CMOS scaling proceeds closer and closer towards its limits we have seen many new physical effects, most of them degrading the MOSFET behaviour compared to ideal long channel devices. However, the basic CMOS circuits have remained more or less the same over all the years, and many digital circuit designers are just used to the fact that every year they get more transistors on their chips for the same cost, and all they have to do is to use a new version of the BSIM MOSFET model, of the design and layout tools, and to rely on device and process development for the rest. It can be predicted that for the next CMOS generations to come the changes on the device and technology side will be so substantial that designers of digital circuits definitely will experience a number of new challenges and can no longer delegate all the effort to the guys in device technology development.

In addition, the MOSFET as an all-rounder is found in memories and analog blocks within integrated systems on chip (SoC). There the transistors are not regarded as mere complimentary switches but as voltage controlled current sources. Therefore additional figures of merit get significant like the intrinsic gain (quotient of gain g_m and output conductance g_{DS}) and the matching of transistor pairs in analog circuits. Also in static memory, the transistors are not only switches, but must have well-controlled on-current ratios to enable readability as well as writability of the memory cell. Matching requirements are not so stringent as in analog, but have to be fulfilled for minimum sized devices.

Already now, different types of MOSFETs are provided for diverse requirements. In future we may find completely different devices for various tasks within one SoC. Several grades of innovation that can be expected for the near and for the far future will be discussed in this paper.

In Section 2 we will describe scaled and novel CMOS devices known as FinFETs, Multi-Gate-FETs, TriGate MOSFETs, etc. and their impact on circuit design. There are, e.g. new design strategies for high performance and high yield or increasing design constraints such as width quantization, layout constraints, leakage and voltage limits.

In Section 3 we will consider novel devices different from the CMOS architecture with digital switching capability employing the field effect, such as Carbon Nanotube Transistors or Tunneling Field Effect Transistors. These devices show other quantitative characteristics, but from the circuit point of view they do not imply much difference in principle. In Section 4 we will finally discuss completely novel principles which also mean a new paradigm for the circuit designer, such as crossbar switches and magnetic computing.

2. Scaled and novel CMOS devices

In the last public ITRS meeting in Matuhari (December 2007) it was predicted that after 2010 the conventional bulk MOSFETs will be replaced by the three dimensional MuGFET structure or the

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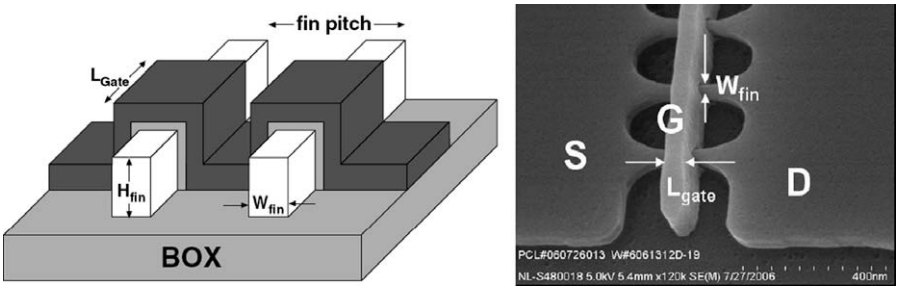

Fig. 1. Schematic view (left) and SEM picture of MuGFET [8].

UTB-FDSOI device [1]. A lot of work is currently under way in Europe, US, and the Far East to develop and optimize these new devices, which are also called FinFETs, Trigate MOSFETs, or Multi-Gate MOSFETs [2–9]. A typical structure is shown in Fig. 1 and consists of one or more thin undoped silicon fins surrounded on three sides by the gate electrode. This geometry allows a much better gate control for very short channel lengths than the conventional planar MOSFET geometry.

2.1. Digital circuits with MuGFETs

In Fig. 2 we compare measured current vs. voltage characteristics and delay-leakage performance of CMOS inverters for MuGFETs and for planar devices with fully silicided gate [8]. The curves are normalized to equal I_{on} and I_{off} currents. MuGFET inverters clearly benefit from steeper sub-VT slope and lower DIBL during switching operation. The low sub-VT slope results in higher overdrive voltage (see Fig. 2a, regions I, III), whereas the low DIBL results in higher current in the saturation regime (regions II, IV). This results in higher circuit speed, especially for the performance relevant NAND/NOR type gates.

Fig. 2b clearly shows the benefit of the MuGFET inverter leading either to a lower leakage power at the same speed or to a higher speed at the same leakage as a conventional MOSFET.

The additional dynamic performance benefit of MuGFETs results from excellent stacked device performance as it is determined by the ID–VDS output characteristics in region IV shown in Fig. 2a). A detailed comparison of NANDs and NORs delays with different stack heights (fan-in) for metal gate based MuGFETs is shown in Fig. 3 [11]. The delay penalty of complex CMOS gates is significantly lower than for typical 130 and 65 nm CMOS technologies. As a result, the delay penalty of a MuGFET NAND5 is lower than for a NAND3 in 65 nm bulk CMOS.

If all the other technology tricks that have been developed for bulk CMOS will be also utilized in the MuGFET (e.g. high-*k* dielectrics, metal gate, strained silicon) the ambitious goals of the ITRS roadmap seem achievable with the MuGFET structure [7–9]. However, parasitic resistance and capacitance values at the fin contacts will be higher than for bulk MOSFETs and the MuGFET width can only be adapted in integer fin numbers, which will lead to additional restrictions in circuit design.

In addition, several drawbacks that are already being experienced in today's bulk MOSFETs will continue to grow with each technology node also for the MuGFETs. Within-Die and Die-to-Die variations of technology parameters will increase in a comparable extent [2,5,10] and the problem of leakage current will turn out to be the number one challenge of digital circuit design. New design strategies have to be used such as adaptive voltage scaling [12], in situ speed control [13,14] and the use of sleep transistors to separate parts of the circuit temporarily from the supply lines [15].

In Fig. 4 we compare the impact of voltage scaling on the performance of timing paths for MuGFETs and three conventional CMOS generations. The MuGFET path outperforms the planar implementations for low voltage operation, which can be explained with the normalized ID–VDS characteristics in Fig. 2a. At equal leakage current, MuGFETs show lower DIBL and steeper sub-VT slope, resulting in larger switching currents in the four relevant operating regions of CMOS logic gates. The performance gain in high VDD operation is limited for MuGFETs by the high parasitic source/drain resistance. Further technology development should be directed towards lowering these parasitics.

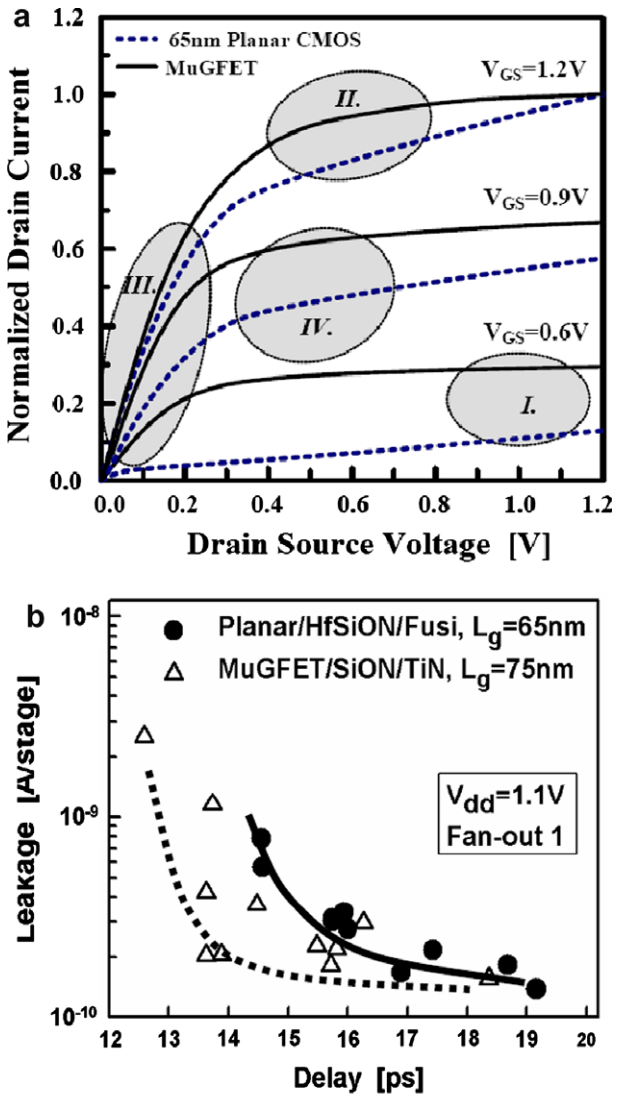

Fig. 2. MuGFET and planar MOSFET characteristics: (a) drain current and (b) inverter delay-leakage trade-off (from [8]).

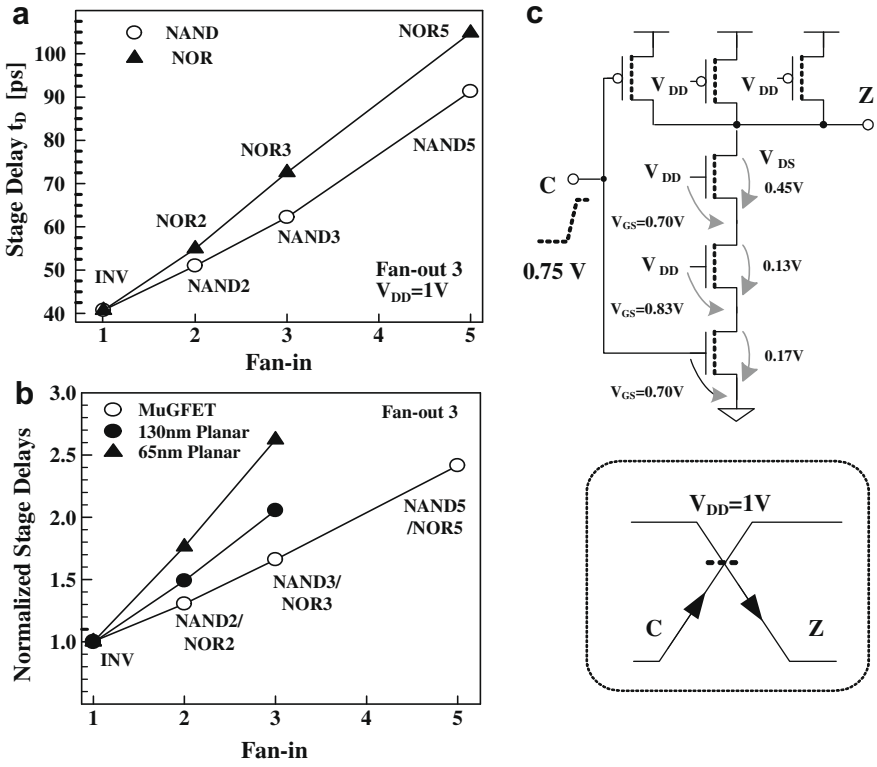

Fig. 3. Stage delays of complex MuGFET CMOS gates (a) and comparison of average stage delays to planar CMOS gates (b) for increasing fan-in. MuGFETs are based on single-midgap metal gate with symmetric threshold voltages. A snapshot of a NAND3 operation during the rising input transition is shown in (c) (from [11]).

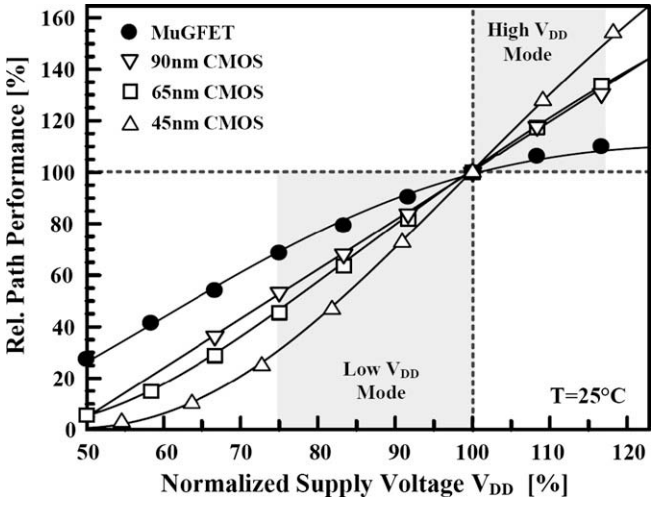

Fig. 4. Comparison of voltage scaling efficiency in planar and MuGFET technologies (after ([8]).

2.2. Analog circuit behaviour

The ongoing technology scaling causes some severe challenges for analog and RF circuit design when standard planar digital CMOS technologies are used. While transistors are getting faster, their analog properties degrade from node to node. One of the most critical issues is the degrading intrinsic gain of the devices due to strong pocket implants and growing impact of short channel effects. In addition, increasing flicker noise, variability and mismatch represent serious issues.

MuGFETs outperform planar bulk devices in terms of matching behaviour and intrinsic gain due to the undoped body and the excellent short channel control. This can again be seen from Fig. 2a, where regions I and IV are most significant for analog circuits. In [18] it has been shown that the figure of merit for an operational amplifier can be improved by 30% with MuGFETs. Matching behaviour as it is required, e.g. in current mirrors can be improved by 25–50% with undoped, metal-gate based MuGFETs. In addition to static mismatch transient current variations due to charge trapping and self-heating may impact the performance of analog and mixed-signal circuits [16].

Flicker noise increase has been observed for narrow fins due to the high density of states at the non-perfect surface (110 crystal orientation and roughness) of the fin sidewalls. The introduction of high-*k* dielectrics will further degrade noise performance. The noise level in a MuGFET can be about 2.5 times above that in planar MOSFETs. For the design of an operational amplifier with MUGFETs this would require about 70% more area and power to keep the input referred noise at the same level than for planar MOSFET technology [18]. In [17] a comparison has been made for analog circuit blocks in the frequency range of 2–60 GHz realized with either bulk MOSFETs or MuGFETs in 45 nm technology. It has been shown that for these cases an additional improvement of parasitic resistances and fringe capacitances in the MuGFET technology is required in order to achieve the same performance as in bulk CMOS.

3. Novel devices beyond CMOS

3.1. Tunneling Field Effect Transistors

The TFET (Tunneling Field Effect Transistor) is a device which acts as field-effect transistor, where a change in the gate voltage turns the current ON and OFF, but which uses band-to-band tunneling in the transition between the source region and the channel. The simplest version of a TFET is produced by inverting the *n*-type

source region of a NMOSFET into p-type as shown in Fig. 5 [19]. Besides that also vertical TFETs have been presented [21].

These devices have the potential for extremely low OFF-current and offer the possibility to lower the subthreshold swing below the 60 mV/dec limit of conventional MOSFETs. They offer the opportunity for a drastic reduction of subthreshold leakage compared to conventional CMOS technology, without the need to develop any new technology processes. However, the experimentally shown ON-currents are significantly below the values achieved with state of the art MOSFETs.

To overcome these challenges a number of improvements have been suggested in recent publications, such as introducing a high-k dielectric or a double gate geometry [20] pretty much in a similar way as it is done for conventional CMOS. Another possibility is to adjust the tunneling barrier by introduction of Si/Ge mixtures with reduced bandgap [21] to maximize the lateral doping gradient at the tunnel junction. It has also been tried to utilize the impact ionization effect to enhance the ON-current, but in this case the long term reliability of the devices might be a challenge [22].

Moreover, as the impact ionization effect needs at least a drain voltage above the bandgap of silicon, the ON-current enhancement occurs only for Vdd above 1.1 V.

Very recently we have also produced a tunneling MuGFET [23]. In Fig. 6a we show the dependence of on- and off-current for different gate lengths. Increasing L_{gate} from 65 nm to 500 nm degrades I_{ON} by about 40%. Applying the same L_{gate} increment to a standard nFET in the same technology results in a current degradation of more than 70%. This indicates that the current of the Multi-Gate tunneling FET is rather limited by the non-ideal tunneling junction than by the channel resistance.

The output characteristics of a 65 nm pTFET are shown in Fig. 6b. The drain current saturates as expected. Similar to a MOSFET the saturation voltage depends on VGS. A kind of threshold is observed for the drain current for low VDS values, which is also attributed to the non-ideal tunneling junction.

An interesting combination of TFET and MOSFET is the "Butted Source Contact" MOSFET [24] where a lightly doped shallow *n*-type source region is combined with a heavily doped p-type region (Fig. 7). Due to its reduced drain induced barrier lowering (DIBL) this device shows an improved OFF-current compared to conventional MOSFETs, but without the drastic deterioration of the ON-current as seen in today's TFETs.

3.2. Circuit design with tunneling FETs

Since the TFET technology is compatible with CMOS, circuits containing both standard MOSFETs and TFETs can be produced.

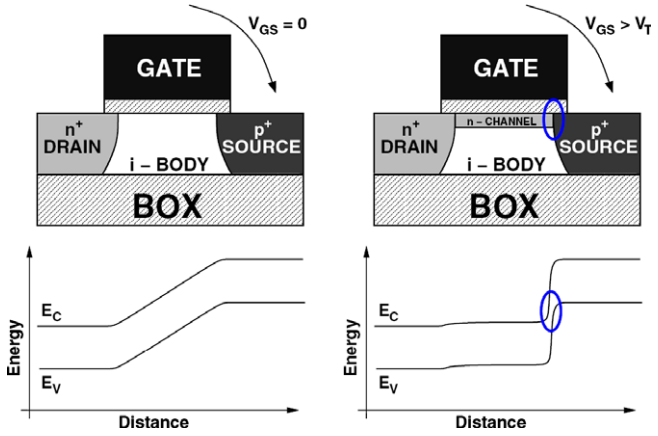

Fig. 5. 2D Cross-section of an SOI Tunneling Field Effect Transistor and band diagrams for OFF and ON states [23].

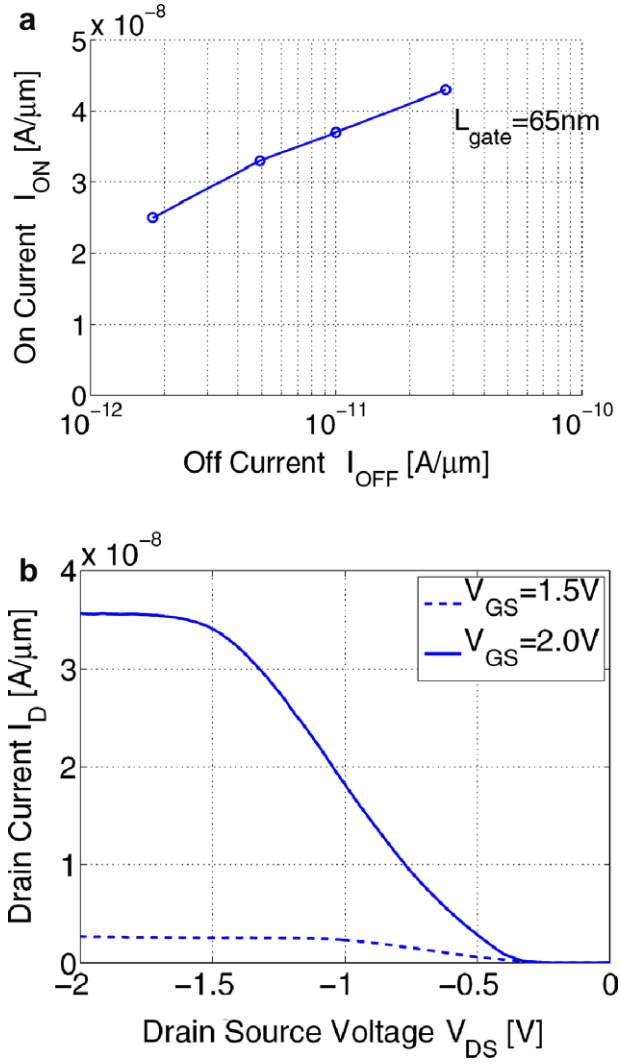

Fig. 6. On- versus off-current for different channel lengths (L_{gate} = 65 nm, 80 nm, 120 nm, 500 nm) (a) and ID–VGS characteristics of 65 nm p-type MuGTFET (b) (from [23]).

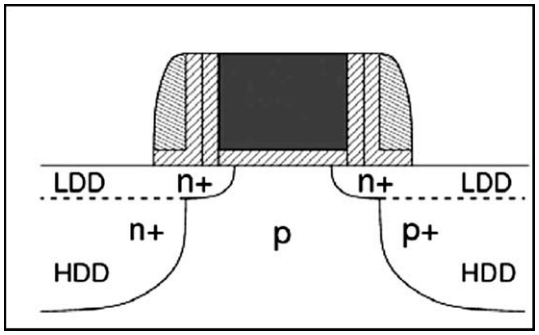

Fig. 7. Butted source contact MOSFET.

This allows utilization of TFETs for special purposes, even if full replacement of CMOS cannot be achieved. This is of special interest in novel SOI technologies, which can no longer make use of bipolar devices as in bulk CMOS, and could instead make use of TFETs.

As an example we present in Fig. 8a voltage reference circuit as possible application for the tunneling MuGFET. Standard MuGFETs M1–M5 and a tunneling MuGFET T1 are combined in this circuit.

Because of the opposite temperature dependence of tunneling and MOSFET currents, the gate-source voltage of M5 can be held independent of supply voltage and temperature variations and can be used as reference voltage.

In [19] we have presented several logic gate structures and an SRAM cell containing a mixture of bulk MOSFETs and planar TFETs. In Fig. 9 we see a six transistor SRAM cell where the two NMOS transistors with the source connected to GND have been replaced by TFETs [25]. Note that in planar bulk TFETs the two word line transistors cannot be replaced, since their source potential is different from GND and would require an additional well. On the other hand, the substrate contact inherent in the TFET source region offers an area advantage in bulk technologies. We determined the butterfly curve by simulations based on measured *I–V* characteristics to characterize the signal to noise margin of the cell, and it was found that the inclusion of tunnel FETs slightly enhances the noise margin of the cell, as it is shown in Fig. 10.

3.3. Carbon Nanotube Field Effect Transistors

A somewhat larger step away from the CMOS mainstream is given by the Carbon Nanotube Field Effect Transistor (CNTFET). In [26] both n-channel and p-channel CNTFETs have been produced using different gate metals and Schottky Barrier source–drain regions. Inverters, ring oscillators, and simple logic gates have been fabricated already [27], but switching speed and ON-current seem still a large step below what is achievable with state-of-the-art CMOS devices [28,29]. However, since the intrinsic capacities are very low, and the device scalability is rather good, CNTFETs could nevertheless develop a high potential in the future when architectures with low interconnect capacitance can be developed [30].

4. Paradigm changes

In the past many suggestions for more substantial paradigm changes in circuit design have been investigated, particularly since the classical CMOS scaling becomes more and more challenging with each technology generation – regarding power, reliability, yield, as well as manufacturing costs.

At the 2007 ITRS meeting the "Emerging Devices Research Group" has published the following six emerging device classes besides classical CMOS [31]:

(a) 1D structures like Carbon Nanotube FETs, Nanowire FETs, Nanowire Heterostructures, and crossbar nanostructures.
(b) Resonant tunneling devices – either as field effect or as tunneling transistors.
(c) Single electron transistors, which use the Coulomb blockade effect.
(d) Molecular devices.
(e) Ferromagnetic devices.
(f) Spin-based devices as candidates for a new spin-based logic.

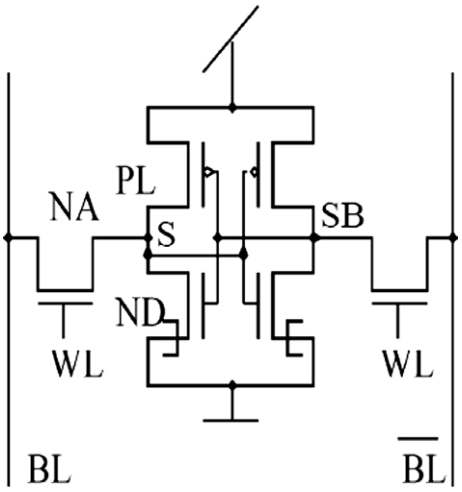

Fig. 9. Static memory cell with two NMOS, two PMOS and two TFET transistors.

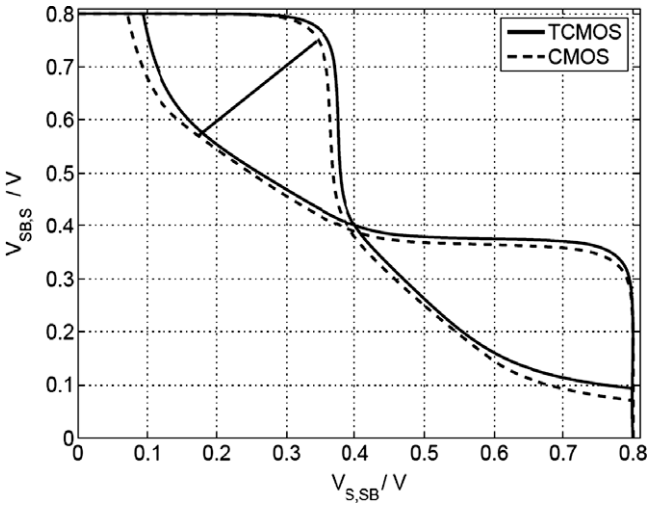

Fig. 10. Comparison of static noise margin of SRAM cells with conventional CMOS transistors and TFETs as pull down devices.

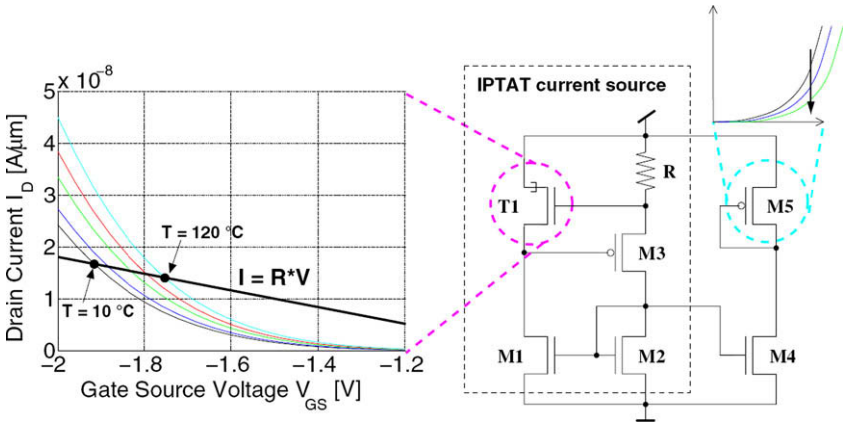

Fig. 8. Schematic of proposed voltage reference circuit combining a TMuGFET T1 with five MuGFETs M1–M5 [23].

Besides that also purely optical switching devices are discussed as candidates for a photon-based logic. Many of these approaches seem appealing in some single aspect such as power dissipation, switching speed or area consumption, but nevertheless at the moment they all do not appear to be really competitive to the evolutionary CMOS scaling path.

The ITRS Emerging Devices Research Group has published a critical evaluation table for these device classes, regarding various aspects like scalability, performance, energy efficiency, gain, reliability, and compatibility with CMOS technology and architecture. In this evaluation the 1D structures (Carbon Nanotubes and Nanowires) clearly outperform the other five approaches in nearly all categories.

But even these devices are not really considered as a future replacement for CMOS. Nevertheless it is predicted that these novel devices will be used as a supplement to CMOS for certain functions, e.g. image recognition and associative processing, which may be more efficiently done in networks of non-linear devices rather than with Boolean logic gates.

4.1. 1D crossbar switches

Regarding future circuit architecture approaches a combined technology of one or more cores of nanostructured 1D devices combined with classical CMOS at the periphery seems the most promising direction because this could utilize the highly developed CMOS technology to counteract several shortcomings of the 1D nanodevices. A variety of interesting examples have been published in recent years [32–35], which utilize programmable architectures based on nanowires together with CMOS logic for programming and decoding as well as for input/output modules.

The basic logic structure is based on crossed sets of parallel semiconductor nanowires (Fig. 11) connected by programmable switches fabricated from molecules, nanocrystals or Carbon Nanotubes. A decoder fabricated in CMOS technology on the same chip allows individual nanowires to be addressed for testing and programming.

Completely new categories of architectural problems will arise with these approaches due to the very high defect density of self-assembled nano structures, such as a dedicated place-and-route procedure for each individual sample [33] or a fault tolerant connection process between lithographically produced CMOS circuits and self-assembled nano switches [35].

Moreover, a recent study has also shown that the output signal of such architectures might be rather small for larger crossbar structures and will require quite challenging I_{on}/I_{off} ratios of the crossbar switches [36].

4.2. Field coupled magnetic circuits

Another very interesting approach are magnetic quantum cellular automata (M-QCA) [37]. This architecture progresses a drastic step away from the conventional CMOS approach replacing the transistors by ferromagnetic quantum-dot cells where the information is stored in the magnetic orientation of an "output" magnetic dot. The information propagates through a patterned network of dots which are locally arranged in various special patterns that determine the logic function to be performed. The dots interact only with their nearest neighbours by magnetic field coupling, and no metallic wires are needed.

Fig. 12 shows simulation results for a logic gate where two of the three inputs have an upward magnetization and pull the output dot from upward to downward magnetization within one clock cycle.

We have recently produced vertically magnetized ferromagnetic quantum dots in multi-layered Co/Pt films [38]. The films were patterned into 48 × 48 dot arrays of 200 nm × 200 nm sized dots using a focused ion beam microscope. By this patterning process we accomplished a locally reduced magnetic coercitivity at the boundaries between adjacent nanodots without actually removing any magnetic material from the surface. These dots allow vertical magnetization either upward or downward. Each nanodot consists of a single magnetic domain and is separated from the neighbouring dots by a paramagnetic boundary. It interacts with its neighbours via magnetic fields. The vertical orientation of the magnetization is particularly suitable to form multi-dot arrangements for complex logic functions.

The main shortcoming of dipole magnetic quantum cellular automata is their relatively low operation speed – larger arrays of dots need long time to relax into their ground state [39]. To address this problem, in [40] we proposed an integrated clocking scheme. A fast changing clocking field is applied that is provided by metallic wires buried under the magnetic layers as illustrated in Fig. 13. These wires can be fabricated with state of the art CMOS technology.

The wires can be pumped by a sinusoidally varying current with a phase shifted by, e.g. $\pi/15$ between neighbouring wires. Inside the magnetic nanodots the clocking field points predominantly in the horizontal direction. During each clock cycle the magnetization is temporarily forced into the lateral direction when the clock current assumes its maximum value and automatically relaxes to its computational ground state when the clocking field decreases. As the 'switching wave' propagates along the line of magnets from input to output the information from the magnetization of the input dots propagates to the output nanodot as can be seen in Fig. 14.

It is obvious that these devices will require a drastic paradigm change in circuit design, power supply, and clock signal distribution. It still seems quite a long way to working circuits with a higher number of logic gates. Yet it can be foreseen that they will offer the possibility of highly parallel logic operation and signal processing, and corresponding architectures have to be investigated.

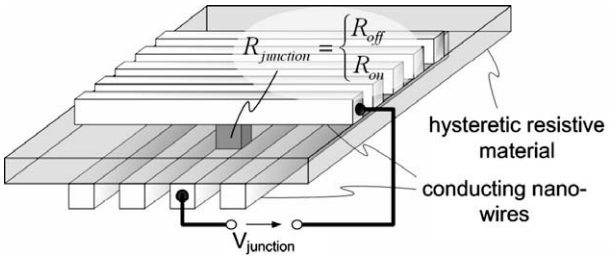

Fig. 11. Crossbar architecture of programmable nanodevices connected by nanowires (reprinted from [36]).

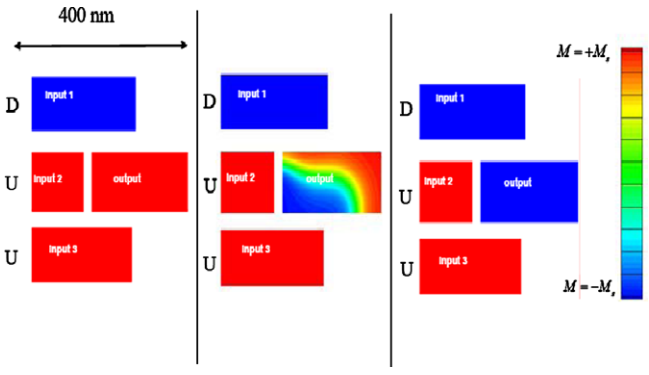

Fig. 12. Simulation results for the magnetic switching behaviour of a quantum cellular automata majority gate [38].

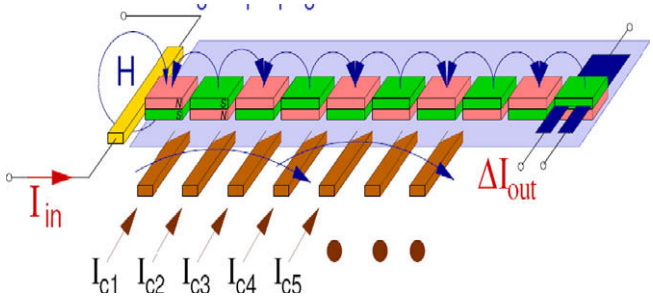

Fig. 13. A sketch showing multiphase clocking wires underneath the field-coupled inverter structure [40].

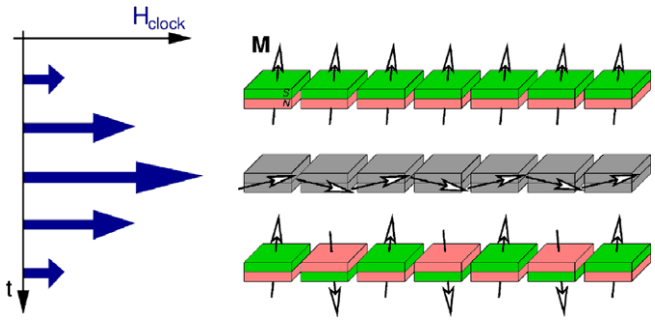

Fig. 14. Magnetization distribution in a ferromagnetic quantum cellular inverter gate at three different points in time (from [40]).

5. Conclusions

The impact of various novel device concepts on digital and analog circuits has been reviewed. For 3D FinFETs the evolutionary CMOS scaling path is more or less pursued. Circuit design will have to cope with enhanced leakage power and large process variability. Using Tunneling FETs or Carbon Nanotube transistors instead of MOSFETs could drastically reduce the leakage power, but the maximum ON-currents and the switching speed of full circuits represent still severe challenges. The use of nanodot switches or quantum cellular automata would bring dramatic paradigm changes to circuit design, requiring fault tolerant designs, new families of logic gates or new clocking concepts, respectively.

Finally, regarding that Mother Nature shows us how signal processing can be performed with very low power, low speed devices operating quite different from today's integrated CMOS, we should never stop to look into completely new and unconventional approaches.

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