Electronics – Basic CMOS digital circuits

Prof. Márta Rencz, Gergely Nagy

BME DED

October 29, 2012
The topics covered today:

- The **inverter**: the simplest logic circuit.
  - The other gates are based on the inverter.
- **Simple gates.**
- **Complex gates.**
The inverter
CMOS circuits – structure and properties
CMOS gates

The output is the negated value of the input.

The transfer characteristic curve shows the output voltage as a function of the input voltage:

\[ V_{out} = f(V_{in}) \]

The proximity of the supply voltage \( V_{CC} \) is logic 1 or HIGH,

and the proximity of the ground potential is logic 0 or LOW.

The characteristic curve of the ideal (blue) and a real (red) inverter.
The same output value is given for large input ranges.

This means that even if the input is noisy and its value diverges from the logic levels, the output is left unaffected for relatively large amplitudes.

Thus, instead of exact input potentials, there are wide input ranges which are converted securely into the right logic levels.
Signal regeneration 1.

- The noise tolerance of inverter makes it possible to regenerate signals, i.e. to **reduce the noise of a signal**.

![Diagram](image)

- The $V_1$ is noisy, its value is close to $V_{CC}/2$.
- $V_2$ is a much better logic signal and $V_3$ is almost perfect.
- Usually 3-4 inverters are enough to regenerate signals.
Signal regeneration II.

- The regeneration process can be seen in a simulation result below.

- Both the waveform and the levels of $V_3$ are correct.
**Threshold voltage**

- **Threshold voltage** is the input value above which the output is a logic 0, while below it we get a logic 1.

- At $V_{in} = V_{th}$:
  
  $$V_{out} = V_{in},$$

  i.e. it’s the cross-section of the transfer characteristic curve and the $y = x$ line.

- In real gates the threshold level might vary.

- The output for input of $V_{th}$ is indefinite.
The inverter CMOS circuits – structure and properties CMOS gates

Logic level ranges

- The ranges where, for a given noise level, the operation of the inverter is secure.
- If the maximum amplitude of noise appearing at every inverter’s input is $V_{NM}$ then the conditions

$$f (V_{LM} + V_{NM}) \geq V_{Hm}$$

$$f (V_{Hm} - V_{NM}) \leq V_{LM}$$

need to be satisfied for correct signal regeneration.

$V_{LM}$: maximum level of logic 0
$V_{Hm}$: minimum level of logic 1
Propagation delay

- **Propagation delay** \((t_{pd})\): the time it takes for the inverter to cover the distance between \(V_{LM}\) and \(V_{Hm}\).

- The length of the positive and negative edge can be different.
Pair delay I.

- When a signal is propagated through a serial connection of inverters, the propagation delay of the path is mainly dependent on the inner properties of the inverters.
- The logic value is the same after every inverter pair, and the delay is $t_{pdp}$. 
Pair delay II.

- The pair delay can be measured with a **ring oscillator**: an odd number ($N$) of inverters connected in series with the output connected to the input.

- This circuit has no stable states, it oscillates – the frequency of the oscillation is a function of the propagation delay:

\[
T = N \cdot t_{pdp}
\]
Introduction

- **Complementary MOS**
  - they consist of two MOS FETs: an n-type and a p-type – hence the name.
  - Every logic circuit is CMOS nowadays.

- **Advantages:**
  - **rail-to-rail levels:** the logic levels are exactly equal to the supply levels ($V_H = V_{DD}$, $V_L = 0$ V),
  - static (steady state) **current consumption is very low** (almost zero),
  - the **propagation delay of positive and negative edges are equal**, 
  - **very fast** operation, 
  - **very low sensitivity to supply voltage ripple**.
A CMOS inverter: an n-MOS and a p-MOS.

At any time only one of them is open.
A well needs to be fabricated for one of the transistors (here: p-type).

The substrate of all n-types is shorted to the most negative potential.

All the wells are connected to $V_{DD}$.

There is a closed pn-junction between every well and the substrate.
The transfer characteristic curve of the inverter I.

Two scenarios are possible depending on the threshold voltage and the supply voltage:

**Small supply voltage**

\[ V_{DD} < V_{Tn} + |V_{Tp}| \]

only one transistor is open at any time

**Larger supply voltage**

\[ V_{DD} > V_{Tn} + |V_{Tp}| \]

during transition both transistors are open
When the supply voltage is a large value: \( V_{DD} > V_{Tn} + |V_{Tp}| \), both transistors are open during the transition between logic levels:
The sizing of an inverter I.

- At the threshold voltage: \( V_{in} = V_{out} = V_{th} \):
  \[
  V_{GSn} = V_{th} \\
  V_{GSp} = V_{DD} - V_{th}
  \]
- This happens when the currents of the transistors are equal:
  \[
  \frac{K_n}{2} \frac{W_n}{L_n} (V_{th} - V_{tn})^2 = \frac{K_p}{2} \frac{W_p}{L_p} (V_{DD} - V_{th} - |V_{tp}|)^2
  \]
  \[
  V_{th} = \frac{V_{DD} - |V_{tp}| + V_{tn} \sqrt{D}}{1 + \sqrt{D}}
  \]
  where
  \[
  D = \frac{K_n \cdot \frac{W_n}{L_n}}{K_p \cdot \frac{W_p}{L_p}}
  \]
is the ratio of current factors of the MOS FET's.
The threshold voltage is a function of the current ratios.

- Usually the threshold voltage of the inverters is set to $V_{CC}/2$.
- If $V_{Tn} = |V_{Tp}|$ then $D$ needs to be 1 in order to have $V_{th} = V_{CC}/2$.

- Due to the difference in the mobility of electrons and holes:

$$\left(\frac{W}{L}\right)_p = 1.5 \ldots 2.5 \cdot \left(\frac{W}{L}\right)_n$$
The parasitic capacitances in a CMOS logic circuit:

1. the substrate capacitances of the transistors \( C_{DB1}, C_{DB2} \)
2. the input capacitance of the next stage \( C_{G3}, C_{G4} \)
3. the capacitance of the wire in between the stages \( C_W \).

The first two can be calculated using the sizes of the MOS transistors, but the third depends on the actual position of the elements. The design is iterative: the transistors might need to be resized after placing, which may lead to replacement.
Switching times in inverters I.

- If the transistor sizing is correct, the duration of the positive and negative edges will be equal.

- E.g. a $1 \rightarrow 0$ transition:

$$t_l = \int_{V_{DD}}^{V_{LM}} \frac{C_L}{I_C} \, dV$$
Switching times in inverters II.

If

$$I_c \approx \frac{K W}{2 L} (V_{DD} - V_T)^2$$

then

$$t_l = \frac{C_L (V_{DD} - V_{LM})}{\frac{K W}{2 L} (V_{DD} - V_T)^2}$$

Thus $t_l$ can be reduced by increasing $V_{DD}$ or the $W/L$ ratio.
The current consumption of CMOS circuits

- **Dynamic consumption** – at every switching event:
  1. the current that flows during transition,
  2. charge pumping.

- It is proportional to the clock frequency and the activity of the circuit.

- **Parasitic phenomena:**
  1. sub-threshold currents,
  2. leakage currents of the pn-junctions,
  3. tunnel current through the gates.
The dynamic current consumption is the sum of two factors:

1. **Transition current:** both transistors are open during the transition between logic states when $V_{tn} < V_{in} < V_{DD} - V_{tp}$

2. **Charge pumping:** during a positive edge the load capacitance is charged to logic 1 by the p-MOS, during a negative edge the load capacitor is discharged through the n-MOS.

   This means that the charge that is fed into the capacitor and then taken out of it, flows from the supply to the ground in two steps. This is an unwanted current that adds to the consumption of the inverter.
The transition current $I$. 

- Both transistors are open during the transition between logic states when $V_{tn} < V_{in} < V_{DD} - V_{tp}$:

\[
I_{MAX} = \frac{K}{2} \frac{W}{L} \left( \frac{V_{DD}}{2} - V_T \right)^2, \text{ the charge that flows through the transistors: } \Delta Q = b \cdot t_{UD} \cdot I_{MAX}, \text{ where } t_{UD} \text{ is the width of the current spike and } b \text{ is a constant that is determined by the input signal’s waveform } (b \approx 0.1 - 0.2).
\]
The inverter CMOS circuits – structure and properties

The transition current $I_I$.

The power consumption:

$$P_t = f \cdot \Delta Q \cdot V_{DD} = f \cdot V_{DD} \cdot b \cdot t_{UD} \cdot \frac{K W}{2L} \left( \frac{V_{DD}}{2} - V_T \right)^2$$

which means that

$$P_t \sim f \cdot V_{DD}^3$$
Charge pumping

During transitions charge is pumped into and out of the load capacitance, i.e. charge is pumped from the supply to the ground:

$$\Delta Q_L = C_L \cdot V_{DD}$$

$$P_{cp} = f \cdot C_L \cdot V_{DD}^2$$

as $I = dQ/dt$ and $f = 1/T$.

The overall power consumption:

$$P = P_t + P_{cp}$$

so it is proportional to $f$ and to $V_{DD}^3, V_{DD}^2$. 
Introduction

- Every CMOS logic gate comprises a **pull-up network** (PUN) consisting of p-MOS transistors and a **pull-down network** (PDN) consisting of n-MOS transistors.

- The number of transistors in the PUN and PDN is equal to the number of inputs.

  For the input combinations that yield a logic 0 output, the PDN shorts the output node to the ground while the PUN is an open circuit.

  For logic 1 outputs the PUN connects the output to $V_{DD}$ and the PDN is an open circuit.

- The PUN and the PDN are dual networks.

  This means that when two transistors are connected in series in one of the networks, their counterparts will be connected in parallel in the other one and vice versa.
CMOS NOR gate

\[ Q = \overline{A + B} = \overline{A} \cdot \overline{B} \]

- The PDN is two n-MOS connected in parallel, the PUN is two p-MOS connected in series.
- When any of the inputs is logic 1, at least one of the n-MOS transistors is open, and at least one of the p-MOS transistors is closed: the output is connected to the ground.
- If both inputs are low, both n-MOS transistors are closed and both p-MOS transistors are open, so the output is high.
CMOS NAND gate

When both inputs are high, both n-MOS transistors are open so they connect the output to the ground, while both p-MOS transistors are closed.

When any of the inputs is low, one of the n-MOS transistors are closed, so there is an open circuit between the output and the ground, but at least one of the p-MOS transistors is open so the output is connected to $V_{DD}$.

If a CMOS gate has $n$ inputs, it consists of $2 \cdot n$ transistors.

$$Q = \overline{A} \cdot \overline{B} = \overline{A} + \overline{B}$$
The transfer gate

A transfer gate is an electronically controlled switch in a signal path.

- It consists an n-MOS and a p-MOS transistor.
- The control signal of the n-MOS is fed to the p-MOS through an inverter.
- At least one of the transistors is always open throughout the entire input voltage range.

Logic gates can be simplified using transfer gates.