Compact modeling approach for microchannel cooling aimed at high-level thermal analysis of 3D packaged ICs

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***Abstract*—This paper presents a new compact modeling technique to describe the convective heat transfer realized by a flow of coolant in integrated microchannels used for thermal management of IC chips. This model works only in case of laminar flow and straight microchannels. The compact model represents the convective heat transfer with alternating resistors in the flow path. The implementation of this model in a successive node reduction (SUNRED) algorithm based thermal filed solver is also presented. A simulation example for a simplified geometry with one channel situated in the center of a pyramidal stack of silicon dice is presented, though, the final target application is in the thermal simulation engine of a logi-thermal simulation system. The errors have been calculated as the difference of the results of the alternating resistor and modified SUNRED model and the result of a detailed CFD simulation. The error of our new compact model was below 2 % for both modeling techniques.**

***Index Terms*—Microfluidics, chip cooling, compact modeling**

	Nomenclature
A_i	Surface area with normal vector directed i $[m^2]$
c_V	Volumetric specific heat $[J/m^3K]$
d	Diameter of the microchannel $[m]$
dx	Size of the simulation grid cell of the model $[m]$
G_{Th}	Thermal conductance $[W/K]$
I_{Th}	Nodal heat flow $[W]$
I_{conv}	Convective heat flow $[W]$
λ	Thermal conductivity $[W/m \cdot K]$
$\dot{q}'$	Heat generation rate $[W/m^3]$
R_{Th}	Thermal resistance $[K/W]$
ρ	Density $[kg/m^3]$
T	Temperature or nodal temperature $[K]$
t	Time $[s]$
$\vec{v}$	Vector of velocity $[m/s]$
v	Average velocity $[m/s]$
V	Volume $[m^3]$

I. Introduction

3D ICs are examples for "more than Moore" solutions to further increase integration density of modern digital electronics, providing higher interconnect bandwidth and lower overall power consumption. The total power dissipation of single chips and the hot spots represent bottlenecks in 3D IC design, basically due to limitations of the overall thermal management solutions. Therefore system architects and manufacturers of 3D integrated ICs must consider using various advanced cooling solutions [1] [2]. Besides applying TSVs (through-silicon vias) barely for thermal purposes, microfluidic cooling [3] gained significant importance.

Many researchers investigated microchannel cooling, mainly from the point of view of the features of the flow (pressure drop, velocity profile, fluid temperature), using CFD tools with the ultimate goal of assessing the overall heat transfer from the active regions of the chips towards the ambient. Detailed CFD models of the microchannels impose excessive computational requirement. Using a compact models of the microchannels instead results in significant performance increase during numerical analysis, especially when fast electrical field solvers are used to calculate the temperature distribution. Such compact models have been introduced in [4] and in [5]. In these papers the authors used current generators for modelling the convective heat transfer, resulting in an overall accuracy below 4%, with a huge (three orders of magnitude), reduction in simulation run-time. In [6] a full resistance network is proposed, with which a 2% error was achieved.

The motivation of our work is to create a compact model of microchannels, which can be built into the thermal simulation engine of a so called *logi-thermal simulation* system [7], [8]. Logi-thermal simulation is a high abstraction level electro-thermal simulation approach which allows to co-simulate the electrical functionality (logic operation) and thermal behavior of digital ICs realized in any physical arrangement. Different abstraction levels such as gate-level description [9] or high level description provided in SystemC [10] can be used to represent the circuit behavior. The dissipation map provided as input for the thermal simulation engine is calculated from the event density of the circuit, obtained as a result of logic simulation. The temperature map provided by the thermal simulation is used to update the temperature dependent properties of the models of circuit elements used in the logic simulation engine. Timár and Rencz used this simulation principle for conventional 2D digital ICs. In our recent works [11], [10] the assumed physical arrangement was a 3D stack of chips using TSVs as thermal vias to improve the heat transfer from the chips towards the ambient.

The goal of the present work is describe a new compact model of microchannels for logi-thermal simulation purposes. The solver of the thermal engine of the target logi-thermal simulation setup is based on the Successive Network Reduction

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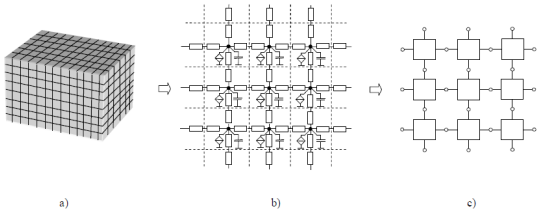

Figure 1: SUNRED algorithm a) 3D rectangular field b) SUNRED version of Finite Differences model in 2D b) Reduced to first level cells [15]

(SUNRED) algorithm originally developed by V. Székely [12], [13]. The main steps of the SUNRED algorithm are shown in Figure 1. Since in log-thermal simulation the temperature distribution of the components of the investigated digital IC is the main target, the compact model applied for the microchannels concentrates on the accurate calculation of the heat removal properties of the coolant rather than on its flow properties. The ultimate goal is to support thermal driven 3D placement of microchannel cooled digital 3D ICs (such as described in [14]) with the help of logi-thermal simulation with which actual circuit operation is considered.

This differentiates our work from the aforementioned compact models also in the method of the modeling of the convective heat transfer. Our approach is based on *time variant resistors* which can be easily implemented in our thermal field solver.

II. Modeling

This section provides the main equations which are basis of our proposed compact model. Using the method of finite differences as a discretization scheme an electrical circuit corresponding to the resulting algebraic equations is created. The actual parameters of the circuit elements depend on the mesh resolution and on the material properties, which are summarized in Table I.

A. Governing equations

The applied modeling approach is based on the suggestion of Sridhar *et al* [4]. Here we summarize the most essential parts of their work.
The equation of heat conduction is:

$$c_V \frac{\partial T}{\partial t} - \nabla(-\lambda \nabla T) = \dot{q}'(\underline{r}, t) \tag{1}$$

Material	**Density** kgm^{-3}	**Thermal cond.** $Wm^{-1}K^{-1}$	**Specific heat cap.** $Jm^{-3}K^{-1}$
Air at 20^oC	1.205	0.024	1232
Silicon at 20^oC	2330	148	$1.76 \cdot 10^6$

Table I: Summary of material properties used in simulations

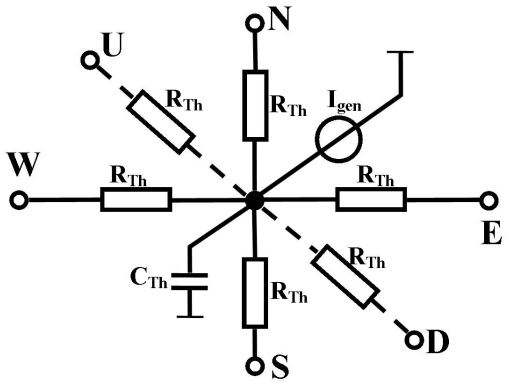

Figure 2: The elements of the thermal compact model in 3D

Considering the convective heat transfer the expanded equation is:

$$c_V \frac{\partial T}{\partial t} + \nabla(-\lambda \nabla T) + c_V \vec{v} \nabla T = \dot{q}' \tag{2}$$

The convection term can be calculated by using *convective resistances*. The convective heat transfer rate on node i is:

$$I_{conv,i} = c_V v_i A_i (T_i - T_{i-1}). \tag{3}$$

So the convective heat transfer rate depends on the temperature difference of the neighboring nodes.

B. Identifying the elements of the equivalent electrical network

The elements of the compact model for the conductive part are shown in Figure 2. The conductive thermal resistance for a node which represents a cube shaped cell of material with sidelength of dx can be calculated as:

$$R_{Th} = \frac{L}{A\lambda} = \frac{1}{\lambda dx} \tag{4}$$

The thermal capacitance of this object is:

$$c_{Th} = c_V dx^3 \tag{5}$$

The current of the source indicated in Figure 2 is the heat generation rate:

$$I_{gen} = \dot{q}' \tag{6}$$

The convective resistance can be derived from Eq. (3):

$$R_{conv,i} = \frac{\Delta T}{I_{conv}} = \frac{1}{c_V dx^2 v_i} \tag{7}$$

The main problem in modeling the convective heat transfer by a set of resistors is that the resistors are so called *reciprocal* circuit elements, thus they equally conduct the flow between their terminals in any direction with a heat-flow depending only on the sign of the temperature gradient across them, therefore their heat conduction capability cannot be associated with the flow direction.

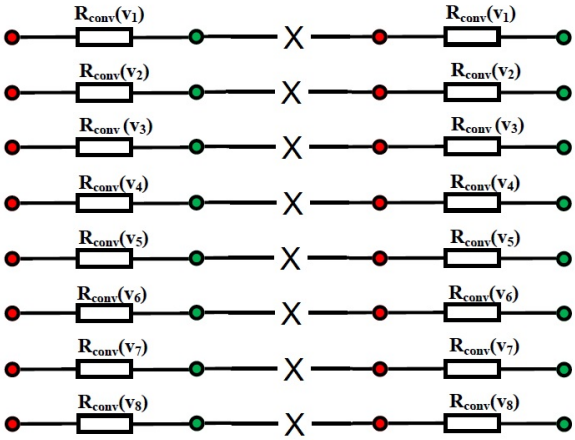

Figure 3: Time variant resistor model – first phase.

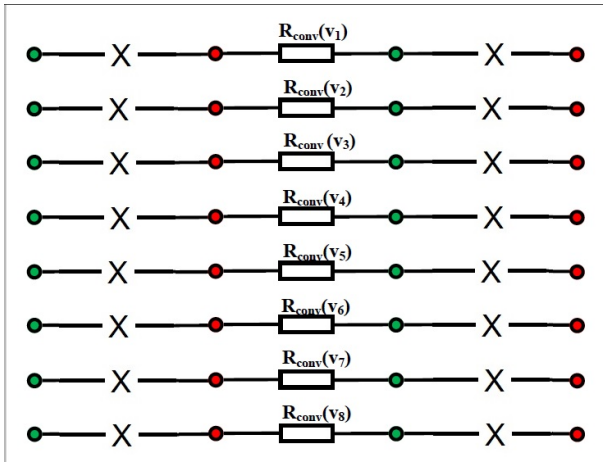

Figure 4: Time variant resistor model – second phase

C. Time variant resistor model

The convective resistances can be used to model the convective heat transfer between two nodes in the flow direction, but the non-reciprical nature of heat transfer represented by the flow of a coolant (fluid) needs to be modelled as well. The problem is that if a simple resistor is inserted into the model, through such a resistor there may be a backwards heat flux in the direction opposite to the flow direction in the microchannel. A "thermal rectifying element" or a "thermal diode" has to be represented. As a workaround to this problem we suggest using *time variant resistors* in the direction corresponding to the flow direction. We define pairs of nodes which are connected with R_{conv} resistors to determine the convective heat transfer in the flow direction correctly and we split the simulation into two phases. In phase one we have resistors between nodes (i-1, j) and (i, j) which are equal to R_{conv} and infinite resistors ("open circuits") between nodes (i, j) and (i+1, j) – scanning the flow direction with index i running along a microchannel, as illustrated in Figure 3. In the subsequent phase of the simulation we impose "open circuit" between nodes (i-1, j) and (i, j) and R_{conv} resistance between nodes (i, j) and (i+1, j) – as illustrated in Figure 4.

The main steps of the simulation are the following:

- Set up the network model for the conductive part such as shown in Figure 2
- Set up the compact model for the convective part such as shown Figure 3 and 4
- Advance the simulation of the conductive part of the model by dt. The resulting 3D temperature map is denoted by $T_0(i,j,k,t+dt)$
- Apply the result of the third step to the convective part of the compact model of the flow (phase one, Figure 3); the resulting temperature distribution is $T_1(i,j,k,t+dt)$
- Apply the result of the third step to the convective part of the compact model of the flow (phase two, Figure 4) the resulting temperature distribution is $T_2(i,j,k,t+dt)$
- Interpolate the results form $T_1(i,j,k,t+dt)$ and $T_2(i,j,k,t+dt)$ to get the final result.

Once the model circuits are established for a steady-state flow, the SUNRED shame can be applied to them.

D. Model implementation in the SUNRED algorithm

The SUNRED algorithm is centred around the admittance matrix of the whole electrical equivalent circuit derived from the discretized form of Eq. (2):

$$\frac{\lambda}{res^2}\left(T_{i+1,j,k}+T_{i-1,j,k}+T_{i,j+1,k}+T_{i,j-1,k} +T_{i,j,k+1}+T_{i,j,k-1}-6T_{ijk}\right)=P+c_V\frac{T_{ijk}(t)+T_{ijk}(t-dt)}{dt} \quad (8)$$

with the help of the *thermal conductances* defined as reciprocals of the thermal resistances (Eq.: 4), the admittance matrix can be written as follows:

$$\underline{\underline{Y}}=\begin{matrix} -6G_{Th} & G_{Th} & G_{Th} & G_{Th} & 0\cdots 0 \\ G_{Th} & -6G_{Th} & G_{Th} & \ddots & \vdots \\ G_{Th} & G_{Th} & -6G_{Th} & \ddots & \vdots \\ \vdots & \ddots & \ddots & \ddots & \vdots \\ \vdots & \ddots & \ddots & \ddots & \vdots \\ \vdots & \ddots & G_{Th} & -6G_{Th} & G_{Th} \\ G_{Th} & 0\cdots 0 & G_{Th} & G_{Th} & -6G_{Th} \end{matrix} \quad (9)$$

where G_{Th} appears in the ith row jth column, if the node (i,j,k), which belongs to the row i in the matrix, is connected to another node (i.e. $i,j,k-1$) which is represented by column j. The other elements of the matrix are zero indicating the lack of direct connection between the represented nodes. This matrix can be used to determine the heat fluxes between nodes by applying Kirchhoff's laws:

$$\underline{I}_{Th}=\underline{\underline{Y}}\underline{T}+\underline{I}_{gen} \quad (10)$$

where $\underline{I}_{Th}$ $\underline{T}$ and $\underline{I}_{gen}$ are vectors with N element that represent each node. The steady-state thermal solution can be derived from Eq. (10) with the assumption of $\underline{I}_{Th}=0$:

$$\underline{T}=-\underline{\underline{Y}}^{-1}\underline{I}_{gen}. \quad (11)$$

The admittance matrix can be reduced by merging the neighboring nodes with the so-called *successive node reduction* (SUNRED) algorithm. To implement the resistive equivalent model of the convective heat transfer in the SUNRED algorithm, first of all one has to determine the appropriate admittance matrix of such systems. The basic building block in the SUNRED algorithm (representing a cube shaped is simulation grid cell) is a circuit cell with six external points (see Figure 1. Such an elementary building block is used to represent an original node with connecting points to other similar building blocks. The elements of the admittance matrix can be calculated as shown in Figure 5. Without the convective conductance, all of the nodes are connected to each other by G_{Th}, thus the admittance matrix of a basic building block can be written as:

$$\underline{\underline{Y}} = \begin{matrix} -5G_{Th} & G_{Th} & G_{Th} & G_{Th} & G_{Th} \\ G_{Th} & -5G_{Th} & G_{Th} & G_{Th} & G_{Th} \\ G_{Th} & G_{Th} & -5G_{Th} & G_{Th} & G_{Th} \\ G_{Th} & G_{Th} & G_{Th} & -5G_{Th} & G_{Th} \\ G_{Th} & G_{Th} & G_{Th} & G_{Th} & -5G_{Th} \end{matrix} \tag{12}$$

This matrix can be modified to model the convective heat transfer by adding a parallel directed conductance as illustrated in Figure 5.:

$$\underline{\underline{Y}} = \begin{matrix} -5G_{Th} & G_{Th} & G_{Th} & G_{Th} & G_{Th} \\ G_{Th} & -5G_{Th} & G_{Th} & G_{Th} & G_{Th} \\ G_{Th} & G_{Th} & -5G_{Th} & G_{Th} & G_{Th} \\ G_{Th} & G_{Th} & G_{Th} & -5G_{Th}-G_{conv} & G_{Th}+G_{conv} \\ G_{Th} & G_{Th} & G_{Th} & G_{Th} & -5G_{Th} \end{matrix} \tag{13}$$

The given matrix is dissymmetric, hence the fast algorithms developed for symmetrical matrices can not be used here.
We can create a new object with the concatenation of two basic admittance matrices. This way the original SUNRED algorithm halves the number of blocks in every step, but for demonstration purposes we have used a simplified algorithm which concatenates only one basic block to reduced node count set of blocks in a single node reduction step as shown in Figure 6. In contrast to the the original SUNRED method which enables only a block system with $2^N \times 2^M \times 2^L$ nodes and halfs the number of internal nodes in a single node reduction step this simplified method enables any number of blocks to be concatenated. In the simplified model, it is easy to follow basic building blocks which was a major advantage during the debugging of the software code in which the method was implemented. The price paied for this was the longer execution runtime, but to in the phase of the evaluation of the modeling method it was acceptable.

E. Boundary and initial conditions

Our modeling approach was tested and compared to a detailed flow model of a simple geometry: a silicon blocl with dimensions of 1 mm x 1 mm x 10 mm and a microchannel with a square shaped cross-section inside with $d = 300\mu$m side, see Figure 7. The channel was positioned to the center of the silicon block. The characteristic sizes of this test case are close to the dimensions of the test case mentioned in [14]. For testing our model, we set up Dirichlet-type boundary conditions for the sidewalls of the silicon block with $T = 300K$ and with a $T_{init} = 300K$ initial temperature for the whole model. The assumed coolant was air with $280K$ temperature

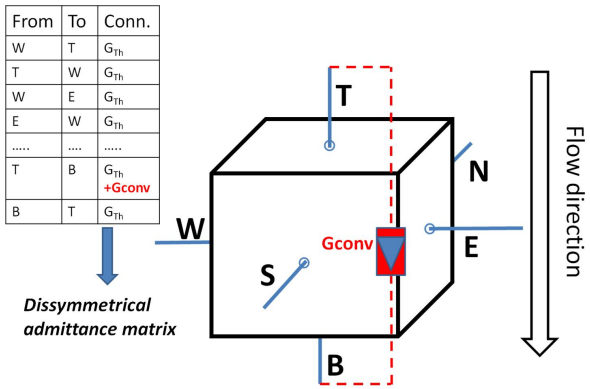

Figure 5: Building block of SUNRED with convective transfer

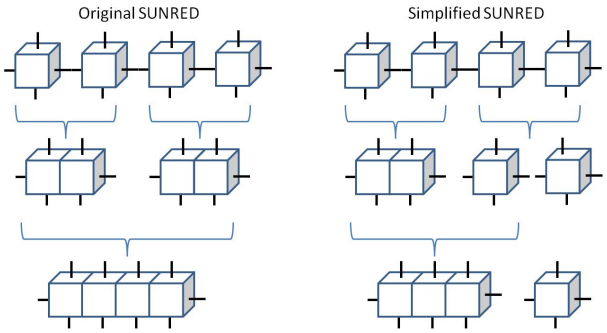

Figure 6: Original and simplified SUNRED method

and the inlet velocity was constant $5m/s$ in Ansys Fluent. In the compact model we used a pre-defined velocity profile with:

$$v(x,y) = \gamma((d/2)^2 - x^2)((d/2)^2 - y^2) \tag{14}$$

which is the velocity profile of the fully developed laminar flow in a tube with square shaped cross-section. The coefficient γ can be calculated from the assumption of the equality of the volume flux obtained by initial condition for Ansys Fluent and the pre-defined velocity profile. Both in the compact and its SUNRED implementation the resolution of the applied simulation mesh was 50 μm, so the whole velocity-profile was investigated in 6 points in a row, therefore the nodal velocity must be modelled as the average of velocity profile near the point and not as the actual value of Eq. (14). The mean value can be calculated as:

$$\frac{1}{dx^2} \int_{x_0-dx/2}^{x_0+dx/2} \int_{x_0-dx/2}^{x_0+dx/2} v(x,y)dxdy \tag{15}$$

The conductances can be calculated from the mean velocity values with Eq. (7).

III. Results

The temperature profile at the center of the channel was compared since this is the segment which is most dependent on the modeling technique used to describe the forced heat convection. In the SUNRED implementation the convective

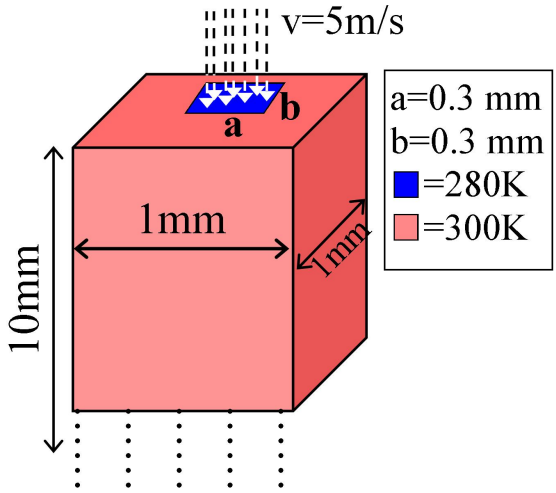

Figure 7: Geometry and boundary conditions for Ansys Fluent

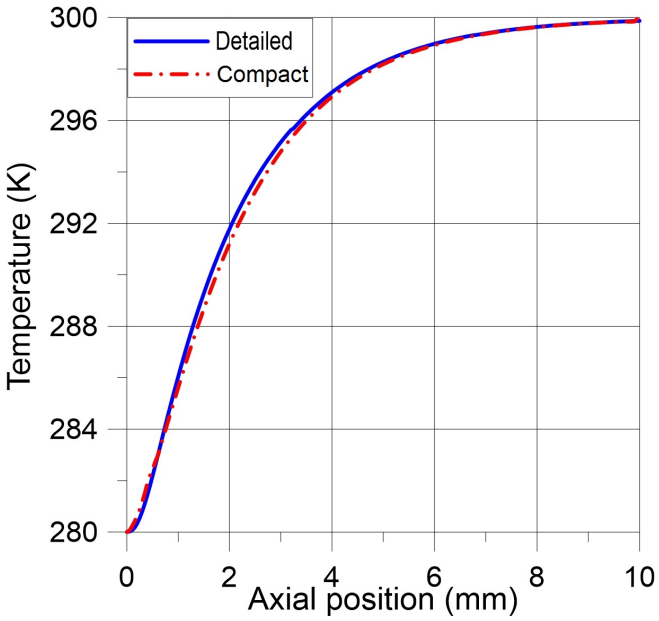

Figure 8: The temperature profile in the center of the microchannel along the axis, obtained by Ansys Fluent (blue, solid line) and by our new compact model (red dashed-dotted line)

conductances are shifted from the center of mesh cell by a half resolution, therefore it is more informative to compare the temperature profiles of the SUNRED and CFD simulations on that line. The obtained results are shown in Figure 8 and 9. We can find the most difference between the results of CFD and compact models at the front of the profile since the Ansys Fluent model calculates the transitory (entrance region) of the velocity profile, while in our compact model we calculate with the fully developed velocity profile in the whole range.

The accuracy of the compact model and its SUNRED

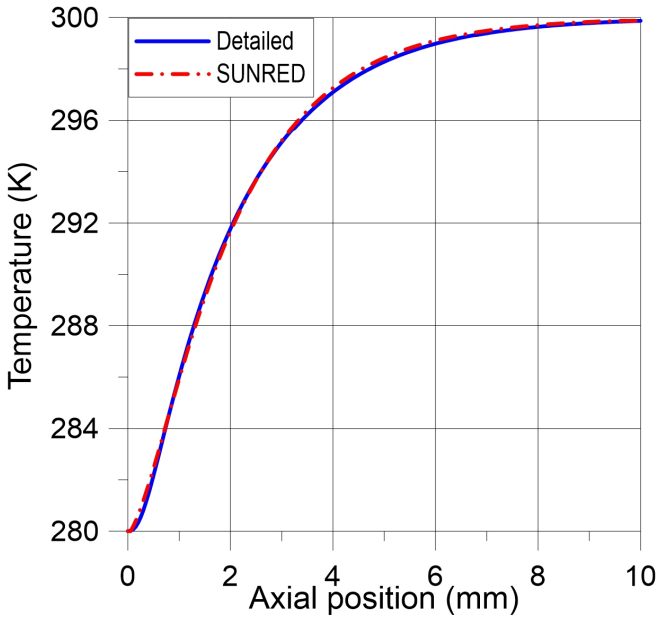

Figure 9: The temperature profile next to the center of the microchannel along the axis, obtained by Ansys Fluent (blue, solid line) and by the new SUNRED model (red dashed-dotted line)

implementation was calculated as the variance between the temperature profiles resulted from the novel models and detailed CFD simulation. The *variances* (σ^2) were calculated as follows:

$$\sigma^2 = \frac{1}{N}\sum_{i=1}^{N}\left(T_{\text{FLT}}(x_i) - T_{\text{Com/SUN}}(x_i)\right)^2, \qquad (16)$$

where N is the number of nodes to sum (here 200). To calculate the relative error the variance was compared to the average temperature rise:

$$Err_\sigma = \frac{\sigma}{\sum_{i=1}^{N}\left(\Delta T_{\text{FLT}}(x_i)/N\right)} \qquad (17)$$

The variation was $\sigma^2 = 0.097K^2$ for the time variant resistor approach, and $\sigma^2 = 0.017K^2$ for SUNRED implementation. It means that the relative errors were $Err_{COM} = 0.0198$ and $Err_{SUN} = 0.0082$.

The CFD simulation was realized in Ansys Fluent. The mesh contained 640000 nodes, the transient simulation to reach $t = 0.47s$ lasted 4400 seconds. The alternating resistor model was implemented in Matlab, the number of nodes was 80000. The implementation did not contain any speed-up or parallel method and the runtime was 64000 seconds. The prototype of the simplified SUNRED model was also implemented in Matlab, without any parallelization or speed-up technique. The order reduction lasted for 921 seconds, the transient simulation was 103 seconds, that is overall 1024 seconds. Further work is required to implement the SUNRED model in C++ as part of our in-house thermal field-solver tool.

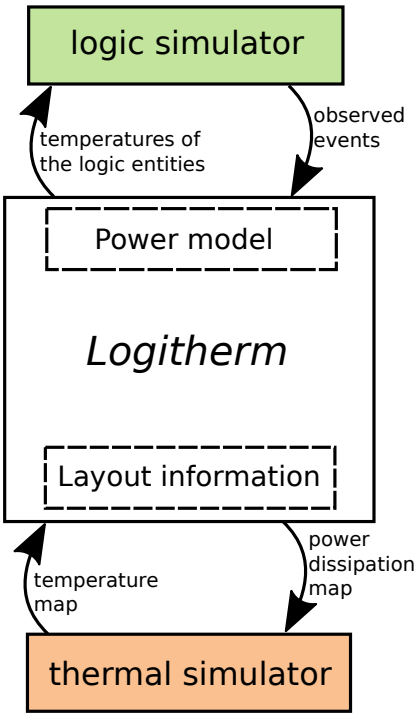

Figure 10: The scheme of the co-simulation of the logic and thermal behavior of digital ICs

IV. Further application

As it was mentioned in the introduction, our ultimate goal is to set up a SUNRED based logi-thermal model which can handle the thermal effect of microfuidic cooling. The logi-thermal simulation paradigm of the combined model is based on the relaxation method: the logic engine controls the simulation process, and at pre-defined time intervals, it determines the dissipated power based on the activity of the circuit and passes the power dissipation distribution to the thermal simulation engine, which calculates a temperature map. This information is then back annotated to the logic engine, thus the functional units are aware of their temperatures. A new logi-thermal simulation framework were introduced [10], which incorporates logic and thermal simulation engines that work in conjunction to perform the co-simulation of the logic and thermal behavior (see Figure 10.). Currently our standard SUNRED thermal field solver is integrated into the framework as thermal simulation engine and SystemC, an event-driven logic simulator, is used as logic simulation engine. In our future work we are planning to use the SUNRED engine extended with the above described model of the convective heat transfer to considered the effect of integrated microchannel based cooling soltions during logi-thermal simulation.

V. Conclusion

We proposed a new compact model to describe the convective heat transfer in microchannels for implementation in conduction mode thermal field solvers. This model is based on the time variant resistor approach. The model was also tailored to SUNRED algorithm and was tested with a simple geometrical arrangement. The results was compared with the help of an Ansys Fluent simulation for a demonstration set. The results showed good agreement, the calculated errors were below 2% for both cases. The ultimate goal of this work to allow using such a model in logi-thermal simulation of larger digital circuits physically realized as microchannel cooled 3D ICs. The next steps of the research are to speed-up the SUNRED algorithm for dissymmetrical case [16] which is the basis of the thermal engine used also in our latest logi-thermal simulation setup [10].

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