Electronics – A/D and D/A converters

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Introduction

- The world is analog, signal processing nowadays is digital.
- The transition between the two domains is done using analog-to-digital (A/D) and digital-to-analog (D/A) converters:
  1. the input signal is first processed (amplified and filtered),
  2. converted to a digital form (A/D conversion),
  3. the digital signal is processed
  4. and converted back to analog at the output (D/A conversion).
Resolution, bandwidth and energy

The higher the bandwidth or the resolution of a signal, the more energy it takes to convert it.
Sampling

In the course of the A/D conversion of an analog signal, samples are taken at a $T_s$ interval.

The proximity of the digital function to the original analog one is a function of the sampling frequency:

$$f_s = \frac{1}{T_s}$$

Nyquist-Shannon sampling theorem

If highest frequency in the spectrum of the input signal is $f_{max}$ then it is completely determined by sampling its values at:

$$f_s \geq 2 \cdot f_{max}$$
Digital sampling introduces **quantization error**. It manifests as a low-level noise added to the reconstructed signal.

**Signal-to-noise ratio (SNR)**

\[ SNR_{dB} = 1.76 + 6.02 \cdot N \text{ dB} \approx 6N \text{ dB} \]

E.g., the theoretical SNR of a CD recording (16 bit):

\[ SNR_{CD} > 96 \text{ dB} \]
The basic concepts of A/D and D/A converters

D/A converter architectures

A/D conversion and ADC architectures

D/A conversion

\[ V_{out} = \frac{V_{ref}}{2^N} \cdot B = V_{LSB} \cdot B \]

where

- \( V_{ref} \) is the reference voltage,
- \( N \) is the resolution of the conversion,
- \( B \) is the binary value,
- \( V_{LSB} \) is the voltage that corresponds to the LSB value.
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The ideal D/A converter

Full scale (FS)

\[ V_{out,max} = \frac{V_{ref}}{2^N} (2^N - 1) = FS \]

\[ V_{out,min} = 0 \]

The LSB voltage

\[ V_{LSB} = \frac{V_{ref}}{2^N} \]
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The properties of a non-ideal D/A converter

Errors of D/A converters:
- offset error,
- gain error,
- nonlinearity error,
- monotonicity error.
The reference voltage is divided into $2^N$ parts.

The **bits of the binary value control switches** that connect the right analog value to the output.

This is an **analog multiplexer**.

An analog switch can be realized using a **CMOS transfer gate**.

It requires **identical resistors**.

It is monotonic per construction.

For $N$ bits $2^N$ resistors are needed.
It can be proven using the theorem of superposition that the voltage connected to the output when a switch is on corresponds to the binary weight.

The advantage of this solution is that although accurate resistors are hard to realize in ICs, accurate resistance ratios can be very accurate.

It contains resistors of value $R$ merely ($2R$ is realized with two $Rs$).

For $N$ bits $3N + 1$ resistors are needed.
Weighted capacitor D/A converter

- In $\varphi_1$ phase every capacitor is discharged.
- In the $\varphi_2$ phase, if the input is
  - logic 1, the reference voltage,
  - logic 0, ground potential

  is connected to the corresponding capacitor.
- The capacitance of capacitors connected in parallel adds up.
Current switched D/A converter

If the transistors are identical:

\[ I_{D1} = I_{D2} \]

The **currents are switched** using current mirrors connected in parallel **according to the binary weight**.
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The process of A/D conversion

1. **Anti aliasing filter**: a low-pass filter used to filter out components above $f_{max}$
2. Sampling
3. Quantization
4. Digital encoding
LSB: is the voltage corresponding to least significant bit.
Errors of non-ideal A/D converters

The error types are similar to those of D/A converters.
The sample and hold (S/H) circuit

- **When switched on**, the output copies the input voltage.

- **When switched off**, the last input value is held while an A/D conversion is performed.

  The value is held in the capacitor:
  - by the time the switch is turned off, the **capacitor is charged to** $V_{in}$,
  - a voltage follower at the output ensures that the voltage of the capacitor is constant during the conversion.
A comparator’s output is
- logic 1, if $V_+ > V_-$,
- logic 0, if $V_+ < V_-$. 

It’s symbol is the same as the operational amplifier’s, but they are not the same.
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Flash A/D converter

- The reference voltage is divided into $2^N$ parts.
- Comparators are used to compare each value in the divider with the input.
- The output of the comparators is a **thermometric code**:
  - the bits below the input value are logic 0,
  - the bits above it are logic 1.
- This code needs to be converted to binary.
- For a resolution of $N$ bits $2^N$ resistors are needed, thus these converters need a very large chip area – they are fabricated with a resolution of 8 – 9 bits at most.
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**D/A converter architectures**

**A/D conversion and ADC architectures**

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**Cascaded flash A/D converter**

1. the **high bits are converted**,
2. this value is **subtracted from the input**,  
3. the **rest is converted using the other converter**.

- The resolution is \( N = N_1 + N_2 \) bits.
- The length of the conversion:
  \[
  t_{A/D} + t_{D/A} + t_{subtraction} + t_{A/D}
  \]
- \( 2^{N_1} + 2^{N_2} - 2 \) converters needed instead of \( 2^{N_1+N_2} - 1 \)
- This is a **trade-off between speed and chip area**.
High-speed A/D conversion

- \( M \) slow converters work in turns.
- The overall sampling frequency can be increased \( M \) times.
Successive approximation D/A conversion I.

$N$ bits are calculated in $N$ steps.
Successive approximation D/A conversion II.

- **At the beginning of the conversion** the MSB bit is 1, the rest is 0.
- The **input value is compared to the binary value** converted to analog by the D/A converter. ˝u
- **If the DAC’s output is bigger, the bit is set to zero,** the one below it is set to 1.
- This is **done for every bit.**
- The length of the conversion: \( N \cdot T_{\text{step}} \).
Dual-slope A/D conversion I.

- Sampling is very slow.
- Accuracy is high: 20 – 24 bits.
The input **signal is connected to the input of the S/H**, the output of the integrator is set to zero.

2. The **conversion begins**: the signal is integrated for a length of $N_{\text{ref}}$ clock cycles.

3. The **negative reference voltage is connected to the input** and the number of steps it takes ($N_x$) to discharge the capacitor is counted:

\[
V_{\text{in}} = \frac{N_x}{N_{\text{ref}}} \cdot V_{\text{ref}}
\]
Sigma-Delta ($\Sigma - \Delta$) A/D converters I.

- This is a first order $\Sigma - \Delta$ ADC.
- **Oversampling:** it samples at a much higher frequency than it is required by the Shannon-Nyquist theorem. The quantization noise is spread in a much larger frequency range this way.
- It is less sensitive to devices inaccuracies – easier to realize in an IC.
- An example: 24-bit ADC for sound input (0 – 20 kHz): 5$^{th}$ order, 64$\times$ oversampling.
Sigma-Delta ($\Sigma-\Delta$) A/D converters II.

Typical waveforms of a 1\textsuperscript{st} order $\Sigma-\Delta$ ADC