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News Fact Sheet

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Intel Developer Forum 22nm News Facts

Sept. 22, 2009 — Intel Corporation is holding its Intel Developer Forum in San Francisco from Sept. 22-24. Paul Otellini, Intel president and CEO, today displayed the world's first working chips built on 22nm process technology. Intel continues to relentlessly pursue Moore's Law and provide its benefits to end users. Marking the third generation of high-k metal gate transistors, this event comes 2 years after Intel demonstrated working test circuits on the previous 32nm generation, and validates that Moore's Law continues well past the point when experts had predicted that the industry would hit a scaling wall.

- SRAMs are used as test vehicles to demonstrate technology performance, process yield and chip reliability prior to ramping processors and other logic chips that will use the given manufacturing process.
- Intel is now in full development mode on 22nm and on pace to continue the company's "tick- tock" model into the next generation.
- The 22nm test circuits include both SRAM memory and logic circuits to be used on 22nm microprocessors.
- SRAM cells of 0.108 and 0.092 square microns function in an array totaling 364 million bits. The 0.108 square micron cell is optimized for low voltage operation. The .092 square micron cell is optimized for high density and is the smallest SRAM cell in working circuits reported to date.
- The test chip packs 2.9 billion transistors, at approximately double the density of the previous 32nm generation, in an area as small as a fingernail.
- The 22nm dimensions are patterned with exposure tools using light with a wavelength of 193nm, a remarkable testament to the ingenuity of Intel's lithography engineers.
- This 22nm technology continues to deliver the promise of Moore's Law: smaller transistors, improved performance/watt and lower cost per transistor.