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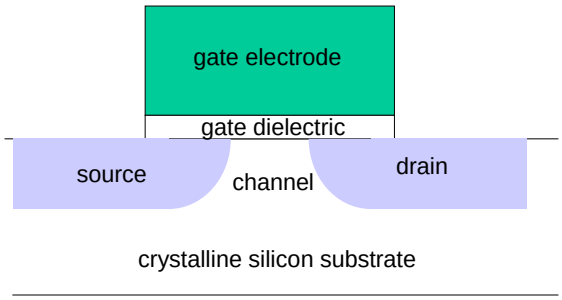
Glossary

INTEL HIGH-K, METAL GATE TRANSISTOR GLOSSARY OF TERMS



Basic CMOS transistor

Transistor – A simple on/off switch that processes the ones and zeroes of electrical data. Digital chips, such as microprocessors, consist of millions of such transistors connected together by copper wires in a specific pattern. The current Intel® Core™2 quad-core processor has more than 500 million tiny transistors. As technology advances, the objective is to make these transistors smaller, faster, cheaper and less energy-hungry, all of which leads to more powerful chips. Current flow from the source to the drain is determined by whether the gate is at high or low voltage, much as a light switch's state (up or down) controls whether or not current flows to a light bulb.

Source – The part of the transistor from which the current flows. It consists of doped silicon – meaning silicon containing impurities that lower resistance.

Drain – The part of the transistor to which the current flows. It is doped with impurities in the same way as the source. A transistor is completely symmetrical, meaning current can flow from source to drain, or drain to source.

Gate (also known as gate electrode) – A region at the top of the transistor whose electrical state determines whether the transistor is on or off. Traditionally, the gate is made of polycrystalline silicon (polysilicon) – or silicon whose atoms are randomly placed and are not in a grid-like structure.

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Channel – The region between the source and drain, where current flows when the transistor is in the 'on' state. It consists of silicon in the crystalline state, that is, silicon in an orderly grid-like (lattice) structure.

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Gate dielectric – A thin layer underneath the gate that isolates the gate from the channel. In today's chips, it consists of silicon dioxide.

Silicon dioxide – Molecules consisting of one silicon and two oxygen atoms, which form a good insulator (non-conductor of electricity). For a gate dielectric, a thin silicon dioxide layer is desirable for high performance. The problem is that the thinner the layer, the higher the leakage through it – hence the effort to replace it with new materials that preserve its properties but don't need to be so thin.

High-k material – A material that can replace silicon dioxide as a gate dielectric. It has good insulating properties and creates high-field effect (hence the term "high-k") between the gate and channel. Both are desirable properties for high-performance transistors. "k" (actually the Greek letter kappa) is an engineering term for the ability of a material to hold electric charge. Think of a sponge: it can hold a lot of water. Wood can hold some, but not as much. Glass can't hold any at all. Similarly, some materials can store charge better than others, and hence have a higher "k" value. Also, because high-k materials can be thicker than silicon dioxide – while retaining the same desirable properties – they greatly reduce leakage.

Leakage – Current flowing through the gate dielectric. In an ideal situation, the gate dielectric acts as a perfect insulator, but as it is made ever thinner (in Intel's 65nm process, it is a mere 5 atomic layers thick!), current leaks through it. This leads to undesirable results. The transistor doesn't behave as it should, and it consumes more power than it should. In comparison, think of the waste caused by a leaky faucet.

NMOS transistor (also known as n-type transistor) – A transistor that is on when its gate is at high voltage, and off when its gate is at low voltage.

PMOS transistor (also known as p-type transistor) – A transistor that is opposite to an NMOS transistor, meaning it is off when its gate is at high voltage and on when its gate is at low voltage.

CMOS transistor (complementary metal oxide semiconductor) – A process technology in which both NMOS and PMOS transistors exist. All modern logic chips such as microprocessors and chipsets use CMOS due to its ability to deliver a combination of high performance and low power, all at a low cost.

Threshold voltage – The voltage level between high and low that distinguishes whether a transistor is on or off. For an NMOS transistor, if its gate is above the threshold voltage, it is "on." If it is below the threshold voltage, it is "off." A PMOS transistor exhibits complementary behavior. Transistors are designed to have a low threshold voltage, as this leads to high performance (think of a racing car with a low center of gravity).

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Threshold voltage pinning (also known as Fermi level pinning) – One of two undesirable effects when a high-k gate dielectric is combined with a polysilicon gate electrode. Due to some defects that arise at the gate dielectric/gate electrode boundary, it becomes difficult to adjust the threshold voltage to a low value, which is needed for high performance. The problem goes away when the gate electrode is a specific metal, rather than polysilicon. The choice of metal is different for NMOS and for PMOS transistors.

Phonon scattering – The second undesirable effect when a high-k gate dielectric is combined with a polysilicon gate electrode. This phenomenon limits electron mobility and hence degrades performance. The problem goes away when a gate made from a specific metal replaces the polysilicon gate, and the right process recipe is applied.

Related terms

Moore's Law – A prediction (not truly a law) made by Intel co-founder Gordon Moore that the number of transistors on a chip double every two years. Intel's microprocessors have followed this law very closely, beginning with the 4004 in 1971, with just over 2,000 transistors, and leading up to today's Itanium® 2 processor that has 410 million transistors. In general, transistor density is roughly doubled with each new process generation, which occurs every two years.

Strained silicon – A technique for speeding up transistors. As described above, the silicon atoms in the channel are packed neatly in a grid-like (lattice) structure. It has been known for decades that stretching the grid so the silicon atoms are slightly farther apart than in their natural state makes NMOS transistors switch faster (similarly, compressing the lattice slightly speeds up PMOS transistors). This stretching/compressing is known as straining. Intel uses special techniques to strain its 90nm process NMOS and PMOS transistors to improve their performance.

Low-k dielectric – Low-k dieletrics are used to insulate on-chip interconnects and should not be confused with the high-k dielectrics. In transistor gate dielectrics, high-k is desirable as it gives high performance with low leakage. In interconnects, low-k is desirable as it leads to faster signal transmission times.

Silicon-on-insulator (SOI) – SOI refers to the use of a layered silicon-insulator-silicon substrate on which transistors are built, rather than a simple (bulk) silicon substrate. Some companies claim to get some performance and/or power benefits from SOI over bulk silicon. Intel's analysis shows that such benefits, if any, are marginal, and do not justify the substantial cost increase of SOI wafers. Intel has never used, nor does it plan to use, partially depleted SOI (PD-SOI) that others are using. There is another type, however, called fully-depleted SOI (FD-SOI) that is under investigation at Intel and is not being used by any chip makers today.

Tri-gate transistor – A new type of transistor that Intel has designated a potential candidate for its future process technology generations. The transistors described earlier in this document are planar transistors. That is, they have a single flat gate that is parallel to the surface of the silicon substrate. A tri-gate transistor employs a novel three-dimensional structure where the gate wraps around three sides of the silicon channel. A traditional planar transistor could be likened to a highway on top of a mesa (a flat-top mountain with vertical sides) with the electronic signals

traveling like cars across the flat surface of the mountaintop. With the new, elevated 3D design, the signals travel not only across the flat top, but along both vertical sidewalls as well. Hence, the 'tri-gate' name.

Static Random Access Memory (SRAM) – SRAM is a type of memory that is faster and more reliable than the more common DRAM (dynamic RAM). The term static is derived from the fact that it doesn't need to be refreshed like dynamic RAM. While DRAM supports access times of about 60 nanoseconds, SRAM can give access times as low as 10 nanoseconds. In addition, its cycle time is much shorter than that of DRAM because it does not need to pause between accesses.

45nm (45 nanometer) – The next milestone in semiconductor technology. The 45nm process enables chip circuitry with higher performance-per-watt than the most advanced processes in production today. In the future, using the 45nm process will allow chips to be made with twice as many transistors in a given area. Forty-five nm technology will enable more than 20 percent improvement in transistor switching speed and more than a five-fold reduction in transistor current leakage. Intel will use its 45nm process technology to manufacture the next generation of its leading Intel® Core™ 2 Duo and Intel Xeon™ processor families.

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