# RAPID THERMAL PROCESSING OF HIGH EFFICIENCY N-TYPE SILICON SOLAR CELLS WITH AL BACK JUNCTION

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## ABSTRACT

In this paper we report on the design, fabrication and modeling of 49 $cm^2$, 200-$\mu$m thick, 1-5 $\Omega$-cm, n- and p-type <111> and <100> screen-printed silicon solar cells. A simple process involving RTP front surface phosphorus diffusion, low frequency PECVD silicon nitride deposition, screen-printing of Al metal and Ag front grid followed by co-firing of front and back contacts produced cell efficiencies of 15.4% on n-type <111> Si, 15.1% on n-type <100> Si, 15.8% on p-type <111> Si and 16.1% on p-type <100> Si. Open circuit voltage was comparable for n and p type cells and was also independent of wafer orientation. High fill factor values (0.771-0.783) for all the devices ruled out appreciable shunting which has been a problem for the development of co-fired n-type <100> silicon solar cells with Al back junction. Model calculations were performed using PC1D to support the experimental results and provide guidelines for achieving >17% n-type silicon solar cells by rapid firing of Al back junction.

## INTRODUCTION

Most commercial solar cells are fabricated on p-type silicon with screen-printed contacts that are formed by a rapid co-firing process. However, the n-type solar cells are not yet common even though the n-type silicon is quite abundant and generally has superior bulk lifetime. The n-type cells require either boron diffusion or two-step firing using Al emitter to avoid Al spiking or shunting of the p-n junction. In 2000, we demonstrated >14%-efficienct 4-$cm^2$ n-type dendritic web silicon solar cells [1]. The cell was fabricated using IR belt furnace to form the front surface field and back Al p-n junction. Ebara Solar reported 13.5%-efficienct [2] 25 $cm^2$ and 14.1%-efficienct 33 $cm^2$, n-type dendritic web solar cells [3]. Cuevas et al used two-step $POCl_3$ diffusion, evaporated Al and photolithography contacts to demonstrate 15% efficiency on 4-$cm^2$, n-type mc-Si solar cell [4]. Buck et al [5] used $POCl_3$ diffusion and etch back of the rear diffused region, deposition of silicon nitride on the front, screen-printed front silver grid and back Al, followed by co-firing to form the Al alloyed back junction and the front contacts. To avoid the etch back step, in this study we used spin-on phosphorus in conjunction with rapid thermal processing (RTP) to form the front surface field on n-type silicon.

Rapid thermal processing (RTP) is capable of reducing the fabrication time and processing steps, while increasing the cell performance and throughput of a manufacturing line. RTP has been used [6-10] for silicon solar cell fabrication including the formation of emitter and Al back surface field and firing of screen-printed Ag front grid. While RTP has been studied in the laboratory, its principle has been extended to high throughput belt furnaces heated with infrared lamps to improve device performance. With fast belt speeds and appropriate temperature settings, firing profiles close to those generated with RTP systems have been achieved. In this study, we report on the merit of infrared belt line co-firing process to form the Al back junction and Ag front grid on <111> and <100> n-type silicon in conjunction with (a) $POCl_3$ diffused front surface field (FSF) or (b) RTP diffused FSF. Since the Al-doped p-n junction is critical in the cell performance, we also investigated several Al pastes to identify suitable one for the rapid co-firing process. A model is proposed to explain the shunting often observed in cells formed with a $POCl_3$ diffused FSF which also dopes the back side which is later over compensated by Al.

## CELL FABRICATION

Al back junction cells were fabricated on 1-5 $\Omega$-cm <111> and (100) n-type, FZ silicon. The cell fabrication included cleaning the samples followed by front-surface field formation by (a) $POCl_3$ diffusion at 842$^o$C for 20 minutes or (b) spin-on phosphorus, bake, and a 3-min RTP diffusion at 865$^o$C. This resulted in 75-80 $\Omega$/sq. front surface field with a junction depth of about 0.20 $\mu$m for the RTP FSF with peak concentration of $1.68x10^{20}$ $cm^{-3}$ and ~0.45 $\mu$m for the $POCl_3$ FSF. After the phosphorus glass removal and DI water rinse, a low frequency PECVD SiN anti-reflection coating was deposited on the front. This was followed by screen-printing of Al on the back and paste drying at 200$^o$C. A silver grid was screen-printed on top of SiN and dried at 200$^o$C. Both contacts were co-fired in a belt furnace after which the cells were isolated and annealed in forming gas at 400$^o$C for 20 minutes before characterization.

## RESULTS AND DISCUSSION

### Model calculations of Al back junction solar cells

Model calculations in Fig. 1 show that 200-$\mu$m-thick, n-type Al back junction cell with >6 $\Omega$-cm resistivity and $1.72x10^5$ cm/s FSRV can produce cell efficiency greater

than 16%. In addition, efficiency becomes relatively insensitive to base resistivity above 6.1 Ω-cm for this cell design. The model calculations indicate that an FSRV of $1x10^4$ cm/s above the $n^+$ surface would be sufficient to achieve an efficiency >17% on 6.1-40 Ω-cm substrates. To achieve a front surface recombination velocity of $1.72x10^4$ cm/s or less may require a combination of superior dielectric passivation and high sheet resistance emitter. However, cell efficiency can also be improved if the SRV on the $p^+$ emitter surface can be reduced from $1x10^6$ cm/s by employing new cell designs, such as gridded Al doped emitter or boron diffused emitter.

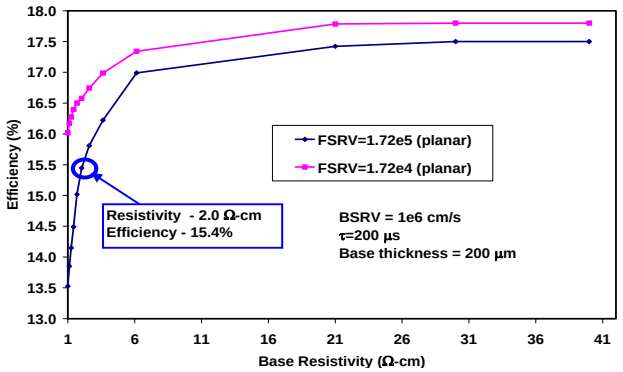


**Fig. 1**: PC1D model calculation showing efficiency of Al back junction cells as a function of base resistivity and front surface recombination velocity.

### Effect of gaps in $p^+$ layer in Al back junction cell

Table 1: Electrical parameters for 49-$cm^2$ cells fabricated with $POCl_3$ diffused wafers

| Cell ID | Orientation & Type | $V_{oc}$ (mV) | $J_{sc}$ (mA/$cm^2$) | FF (%) | η (%) |
|---|---|---|---|---|---|
| 1-6 | (111) n-type | 617 | 31.0 | 68.9 | 13.2 |
| 0-6 | (100) n-type | 575 | 22.9 | 34.0 | 4.5 |
| 1-8 | (111) n-type | 613 | 30.8 | 70.1 | 13.3 |
| 0-8 | (100) n-type | 608 | 16.2 | 35.5 | 3.5 |
| P-6 | (100) p-type | 620 | 33.6 | 78.4 | 16.3 |
| P-9 | (111) p-type | 621 | 33.5 | 75.5 | 15.7 |

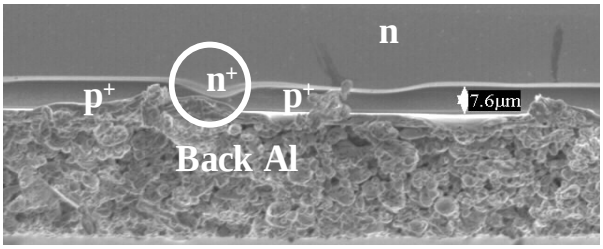


**Fig. 2**: Structure of Al back junction solar cell with a non p-n junction region.

The screen-printed Al is preferred over the evaporated because it consistently results in higher open-circuit voltages and it is faster and more economical. However, non-uniformity in the screen-printed $p^+$ region can sometimes result in a narrow $p^+$ region or even a complete gap in the $p^+$ emitter layer. Such regions are often hard to find or detect. Cross section SEM in Fig. A shows an example of that. In the extreme case, when there is n+ diffusion on the rear, the gap can lead to a direct contact between Al and the $n^+$ region. This could give rise to a resistive shunt.

Table 1 summarizes the cell results on both n and p-type silicon, <100> and <111> silicon fabricated using $POCl_3$ as the source for front surface field or p-n junction formation. The results show that p-base cells produced higher efficiency than the n-base. The open circuit voltage difference between the two types of cells ranged from 4-46 mV. The fill factors were worse for the n-type <100> cells compared to the rest of the cells. Dark I-V analysis performed on these cells revealed that low shunt resistance dominates the fill factor of the n-base cells. The $J_{o2}$ values for the n-base cells are two orders of magnitude higher than the p-base counterparts. The low shunt resistance and high reverse saturation current density was attributed to a combination of gaps in the screen-printed Al-doped $p^+$ emitter resulting in un-compensated phosphorus layer underneath in contact with Al metal. In our process we did not mask the rear surface of the wafers during the $POCl_3$ diffusion or etch back the $n^+$-diffused region.

A resistive shunt across the device shown as an insert in Fig. 3. Model calculations in Fig. 3 show that the resistive shunt value controls both the open circuit voltage and short circuit current density of the Al back junction cells. The higher the resistive shunt, the better the open circuit voltage and the short circuit current density. An open circuit voltage of 625 mV and a short circuit current density of 31.6 mA/$cm^2$ corresponds to a resistive shunt value of greater than 1000 Ω-$cm^2$.

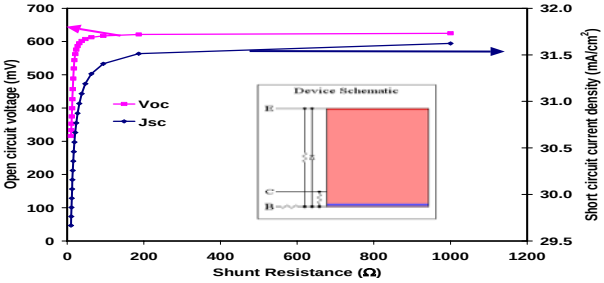


Fig. 3: PC1D model calculations and equivalent circuit for modeling low shunt resistance in n-base cells.

From Table 1, it is noted that cells fabricated on <100> n-type silicon are inferior to the <111> orientation. The dark I-V analysis showed that the shunt resistance in these cells is ≤ 40 Ω-$cm^2$. The measured open circuit voltage matches the modeled value in Fig. 3 for a shunt resistance value of 40 Ω-$cm^2$. This suggests that the gaps in the Al-doped $p^+$ emitter may be more prevalent in the <100> n-type cells than the <111> counterparts.

To investigate the gaps in Al-doped $p^+$ emitter, the SEM analysis was carried out on some of the samples, printed with fritless and fritted Al pastes, after the co-firing step. Figs 4a to 4d show the SEM micrographs of

the Al p-n junction formed on <111> and <100> n-type silicon for two Al pastes after the co-firing process. The depth of p-n junction formed by the screen-printed Al in <100> silicon varied from 6.6-10.9 μm and is ~7.6 μm in <111> silicon. This suggests that there was a higher probability of finding gaps or pinched off regions in the p+ region in the <100> Si because of higher non-uniformity. This is also supported by much lower fill factors in Table 1 for the <100> cells. Furthermore, we observed that irrespective of the Al paste, fritted or frittless, the Al back junction cells, with phosphorus-diffused layer on the emitter side, exhibited low shunt resistance.

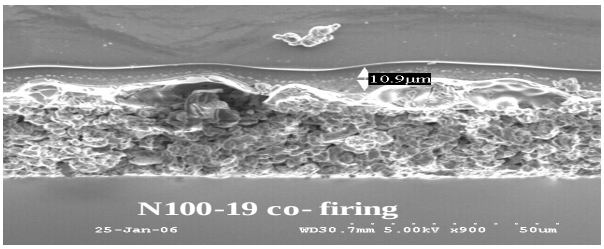

Fig. 4a: SEM micrograph of Al/Si interface in Al back junction cell on <100> (Frittless Al paste)

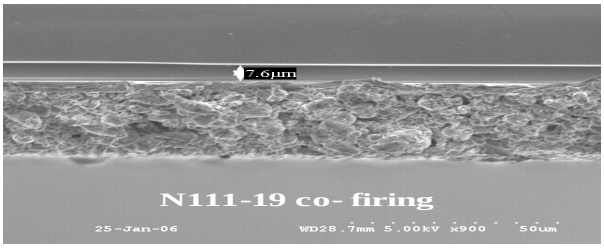

Fig. 4b: SEM micrograph of Al/Si interface in Al back junction cell on <111> (Frittless Al paste)

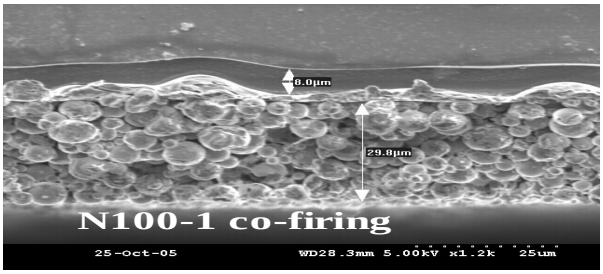

Fig. 4c: SEM micrograph of Al/Si interface in Al back junction cell on <100> (Fritted Al paste)

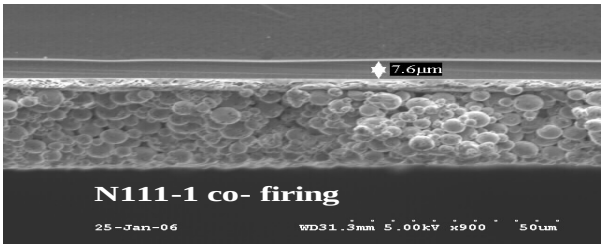

Fig. 4d: Fritted Al paste SEM on <111> Al back cell

**Characterization of RTP Al back junction solar cells**

The resistive shunt, which degrades the Al back junction cells, can either be eliminated by removing the rear phosphorus doped region before screen-printing of Al or by forming a simple sided $n^+$ layer by spin-on/spray-on phosphorus dopant followed by drive-in in RTP. The later was adopted in this study.

Table 2: 49 $cm^2$ RTP n-type <100>, <111> and p-type solar cells measured under standard conditions.

| Cell ID | Orientation & Type | $V_{oc}$ (mV) | $J_{sc}$ ($mA/cm^2$) | FF (%) | η (%) |
|---|---|---|---|---|---|
| 1-18 | <111> n-type | 625 | 31.6 | 77.7 | 15.4 |
| 0-18 | <100> n-type | 623 | 31.4 | 77.1 | 15.1 |
| 1-4 | <111> p-type | 617 | 32.8 | 78.3 | 15.8 |
| 0-2 | <100> p-type | 623 | 33.4 | 77.2 | 16.1 |

Table 3: Diode characteristics of Al back junction solar cells

| Cell ID | $J_{01}$ ($pA/cm^2$) | $J_{o2}$ ($nA/cm^2$) | Rsh ($\Omega$-$cm^2$) | Rs ($\Omega/cm^2$) |
|---|---|---|---|---|
| 1-18 | 0.27 | 15.1 | 23093 | 0.66 |
| 0-18 | 0.15 | 39.1 | 2545 | 0.40 |
| 1-4 | 0.40 | 32.1 | 14310 | 0.66 |
| 0-2 | 0.83 | 9.5 | 2056 | 0.75 |

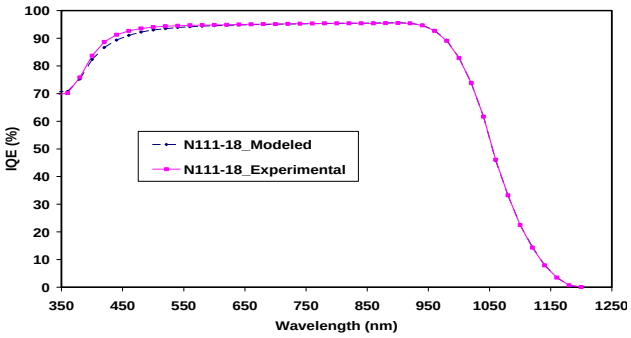

Fig. 5: Measured and simulated Internal quantum efficiency over the entire wavelength for the <111> n-type Al back junction solar cells.

Tables 2 and 3 summarize the light and dark I-V measurements for the RTP screen-printed cells. A simple process involving RTP front surface phosphorus diffusion, low frequency PECVD silicon nitride deposition, screen-printing of full Al back, screen-printing of Ag grid on the front, followed by co-firing of contacts produced cell efficiencies of 15.4% on n-type <111> Si, 15.1% on n-type <100> Si, 15.8% on p-type <111> Si and 16.1% on p-type <100> Si. Open circuit voltage was comparable for n and p type cells regardless of wafer orientation. The excellent fill factor values (0.771-0.783) for all the devices ruled out appreciable shunting which has often plagued the development of co-fired n-type <100>silicon solar cells. The dark I-V analysis (Table 3) revealed shunt resistance values of >2000 $\Omega$-$cm^2$ and series resistance of <0.8 $\Omega$-$cm^2$ for all four types of cells. These high shunt resistances indicate that the pinched off regions in the Al-doped $p^+$ emitter do not appreciably degrade the Al back junction cells unless there is an $n^+$ layer underneath to cause the shunt. To produce high efficiency Al back junction solar cells; the formation of a rear phosphorus-doped layer must be avoided or it must

be removed before the screen-printed Al is applied to avoid the formation of resistive shunt.

Table 4 shows the results of modeling and characterization of the Al back junction cells on <111> silicon, where measured and extracted input parameters are listed along with the modeled cell efficiencies. FSRV of $1.72x10^5$ cm/s and BSRV of $1x10^6$ cm/s were extracted by matching the measured IQE with the simulated IQE in the short and long wavelength range using PC1D simulation program. The bulk lifetime was measured to be ~200 μs in cell after the co-firing step. The junction leakage current of 15.1 nA/cm$^2$ was determined by dark I-V analysis. The back surface reflectance (BSR) was found to 54%. With all the above input parameters, PC1D predicted a cell efficiency of 15.4% with $V_{oc}$ of 625 mV, $J_{sc}$ of 31.6 mA/cm$^2$, and FF of 0.779, which agreed fairly well with the measured values shown in Table 2.

Table 4: Modeling parameters for the n-type <100> Al back junction solar cells.

| **Cell Parameters** | **N111-18** | **>17% cell** |
|---|---|---|
| Base Resistivity (Ω-cm) | 1-5 | >6.1 |
| $R_s$ (Ω-cm$^2$) | 0.66 | 0.66 |
| $R_{sh}$ (Ω-cm$^2$) | 23,093 | 23,093 |
| $n_2$ | 2 | 2 |
| $J_{o2}$ (nA/cm$^2$) | 15.1 | 15.1 |
| Emitter sheet resistance (Ω/sq) | 80 | 100 |
| Surface concentration (cm$^{-3}$) | $1.68x10^{20}$ | $1.65x10^{20}$ |
| Type & Orientation | n (111) | n (111) |
| $\tau_{bulk}$ (μs) | 200 | 200 |
| BSRV (cm/s) | $1x10^6$ | $1x10^6$ |
| BSR (%) | 54 | 54 |
| FSRV (cm/s) | $1.72x10^5$ | $1.72x10^4$ |
| Grid shading (%) | 7.6 | 7.6 |
| Modeled $V_{oc}$ (mV) | 625 | 632 |
| Modeled $J_{sc}$ (mA/cm$^2$) | 31.6 | 36.6 |
| Modeled FF (%) | 77.9 | 77.1 |
| Modeled Efficiency (%) | 15.4 | 17.8 |

Fig. 5 also shows a good match between measured and simulated IQE over the entire range. From this analysis it is evident that by improving the FSF and FSRV greater than 17% efficiency can be achieved. The third column in Table 4 indicates that we need to lower the FSRV to 17,420 cm/s. This can be achieved by reducing the front grid coverage and application of high-quality dielectric surface passivation. The BSRV can be reduced from $10^6$ cm/s if we employ bifacial and interdigitated back contact structures.

## CONCLUSIONS

The process used in fabricating a solar cell should be simple and independent of the substrate type and orientation. $POCl_3$ is widely used for p-based cells. However, the use of $POCl_3$ for n-type Si requires either masking the rear side or removing the $n^+$ region from the rear prior to screen-printing of Al for emitter formation. This is because screen-printed Al junction may become pinched in very few selected areas, bringing the uncompensated $n^+$ region in contact with Al. This causes a shunt, which can severely degrade fill factor. <100> Si is found to be more vulnerable because it shows more non-uniformity in the Al-doped $p^+$ emitter. The resistive shunt was characterized by dark J-V measurements and modeled in PC1D. Model calculations agreed well with the experimentally measured open circuit voltage, short circuit current density, fill factor and the efficiency. To support the model and avoid the extra step of removing the phosphorus or masking before phosphorus diffusion, we used spin-on dopant in conjunction with RTP. This produced Al back junction cells with efficiencies as high as 15.4% on a planar, 200-μm thick n-type <111> silicon. The identical process is applicable to p-substrates and resulted in >16% efficiency on <100> Si. The open circuit voltage and fill factor were comparable for both substrate types and orientations. FSRV of $1.72x10^5$ cm/s and BSRV of $1x10^6$ cm/s were extracted for the 15.4% Al back junction cell by matching the measured and simulated IQE using PC1D simulation. Model calculations were extended to support the experimental results and provide guidelines for achieving >17% n-type silicon solar cell using the rapid co-firing process with an Al back junction.

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