ARTICLE IN PRESS

Available online at www.sciencedirect.com

SCIENCE DIRECT®

PERGAMON

Materials Science in Semiconductor Processing ▮ (▮▮▮▮) ▮▮▮–▮▮▮

MATERIALS SCIENCE IN SEMICONDUCTOR PROCESSING

Future roadblocks and solutions in silicon technology as outlined by the ITRS roadmap ☆

Wolfgang Arden*

Infineon Technologies AG, St. Martin Strasse 76, D 81541 München, Germany

Abstract

The International Technology Roadmap for Semiconductors (ITRS) is a joint global effort of the semiconductor industry and research community to define the future development and requirements of the semiconductor technology for the next 15 years. The paper will review the major challenges, potential roadblocks and proposed solutions for the industry as outlined in the ITRS 2001. The major sections of the ITRS contain technical information about frontend processing and interconnect, device structures and memory concepts, lithography and metrology as well as factory integration and environmental issues. Specific emphasis is given to describe future requirements on new materials and material properties as well as topics related to silicon wafer sizes of 300 mm and beyond. Special issues will be addressed, for example new transistor gate materials, new solutions for interconnect beyond copper metals and low k dielectrics as well as new starting materials for wafer sizes beyond 300 mm.

Keywords: Silicon technology; Roadmap; Semiconductors; Devices; New materials

1. Introduction

The definition of a technology roadmap for the semiconductor industry has started as a national effort in the United States in 1992. Six years later this effort became an international activity with the major global regions participating in the definition of the roadmap, which is now called the International Technology Roadmap for Semiconductors (ITRS [1]). The mission of the ITRS is to define the near and long-term technology requirements for the semiconductor industry as well as to outline potential solutions to meet these needs, as described in Fig. 1. There are 12 International Technical Working Groups (ITWG) with over 800 experts dealing with key areas of the semiconductor technology as there are, e.g. Design and Test, Front End Processing, Interconnect, Lithography, Process Integration and others. The overall activity of the ITRS is coordinated by an International Roadmap Committee (IRC).

2. Hierarchy of IC Requirements

In order to define the technology demands of the IC industry, a hierarchy of requirements is established in the ITRS, as outlined in Fig. 2. This process starts with the definition of chip circuit requirements like cost, power, speed and density followed by overall device requirements given by the parameters supply voltage, leakage and drive currents, transistor sizes, threshold voltage control and others. Thereafter device scaling and device design issues are defined as for example gate length, gate dielectric, junction depth, channel engineering properties and finally process integration requirements are resulting, e.g. thermal budget, overall process flow and material properties. In order to define this sequence of technology needs, a very intensive cross-functional cooperation between the individual Technical Working Groups has become a common practice.

☆ This paper was presented as an invited paper in the 300 mm session of the 2002 spring conference of the European Materials Research Society (EMRS) in Strasbourg, 18–21 June.

*Tel.: +49-89-234-41480; fax: +49-89-234-717-959.
E-mail address: wolfgang.arden@infineon.com (W. Arden).

1369-8001/03/$ - see front matter
doi:10.1016/S1369-8001(02)00131-2

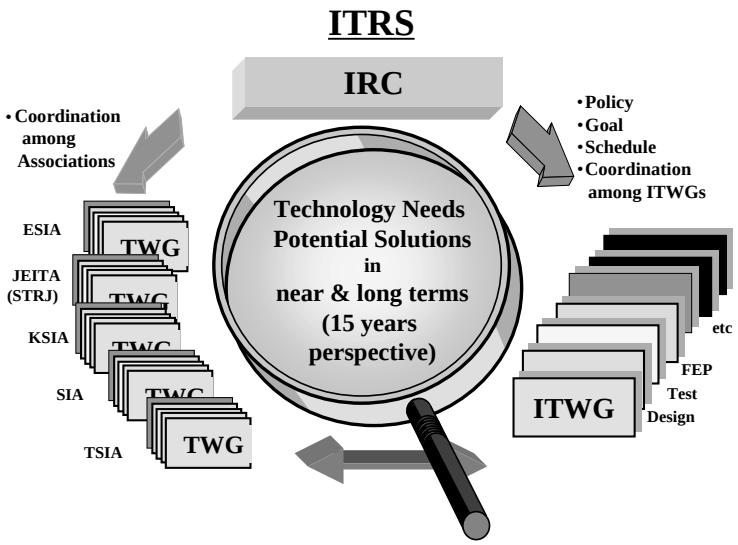


Fig. 1. Mission and definition process for ITRS.

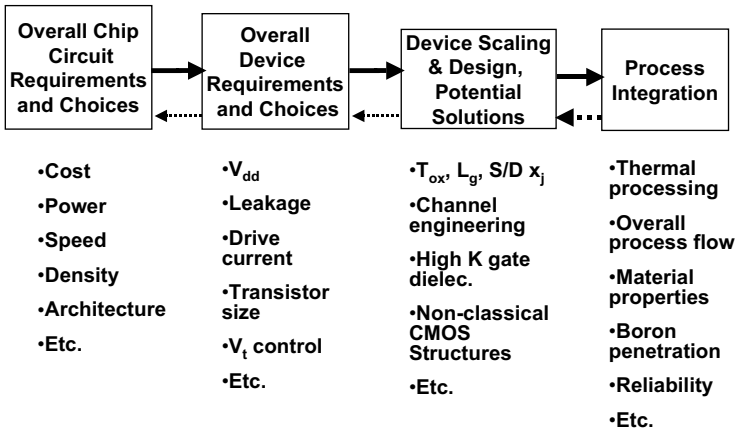
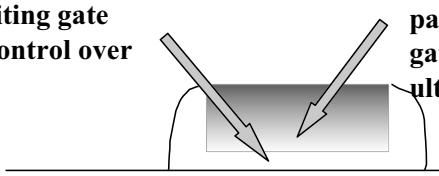


Fig. 2. Hierarchy of IC requirements and choices.

3. Challenges and solutions for device scaling

The continuous scaling of classical CMOS devices is building up key challenges for the design of the transistor. The down scaling of the supply voltage requires an accelerated shrink of the gate length in order to keep up with the demands for drive currents and speed; the scaling of the gate length however results in an increase of the gate resistance with the demand to introduce low resistivity/metal gates, e.g. SiGe gates, especially for RF applications. The scaling of the gate oxide thickness leads to an increase of tunneling currents which results in unacceptable leakage currents and requires the introduction of high k dielectrics as, e.g. oxinitrides or oxide-based compounds of Aluminum/Hafnium. The third area with device scaling leading to severe limitations, is the source/drain region where the continuous thickness reduction results in high series resistance and problems in silicidation with the demand for innovative solutions as, e.g. elevated source/drain. Some of these issues are highlighted in Fig. 3. The table depicts some values of gate stack requirements over time as there are gate lengths for MPUs and Low Power ASICs with the corresponding Equivalent Oxides Thicknesses (EOT) and the allowed gate leakage currents. The red-shaded numbers in the ITRS table indicate that there are no technical solutions yet available, whereas yellow-shaded numbers mean that technical solutions are known, but not yet manufacturable. Numbers in white fields denote the status of manufacturability for the respective required value.

Direct tunneling currents limit allowable gate oxide thickness reduction, thereby limiting gate capacitance and gate control over channel charge



Electrical depletion of doped polysilicon results in unwanted parasitic capacitance that limits gate control of channel charge, ultimately requiring metal gates

Year of Production	2001	2002	2003	2004	2005	2006	2007
Technology Node (nm) (also equals DRAM 1/2 Pitch)	130	115	100	90	80	70	65
MPU/ASIC High Performance Gate Length (nm)	65	53	45	37	32	28	25
Low Power Gate Length (nm)	90	80	65	53	45	37	32
Equivalent Physical Oxide Thickness, EOT, (nm)	1.3-1.6	1.2-1.5	1.1-1.5	0.9-1.4	0.8-1.3	0.7-1.2	0.6-1.1
Low Operating Power EOT (NM)	2.0-2.4	1.8-2.2	1.6-2.0	1.4-1.8	1.2-1.6	1.1-1.5	1.0-1.4
Low Standby Power EOT (NM)	2.4-2.8	2.2-2.6	2.0-2.4	1.8-2.2	1.6-2.0	1.4-1.8	1.2-1.6
High Performance Allowable Gate Leakage (A/cm^2)	15	57	156	270	938	2500	4000
Low Strandby Power Allowable Gate Leakage (A/cm^2)	0.0011	0.0013	0.0015	0.0019	0.0022	0.0027	0.0031
Active Gate Polysilicon Doping for 25% Depletion Allowance (cm^{-3})	9.2 E19	9.2 E19	1.14 E20	1.5 E20	1.66 E20	1.66 E20	1.87 E20

***"red wall"* for high performance results from reliability and thickness control**

***"red wall"* for low power results from lower allowed tunneling curents**

Fig. 3. Gate stack challenges.

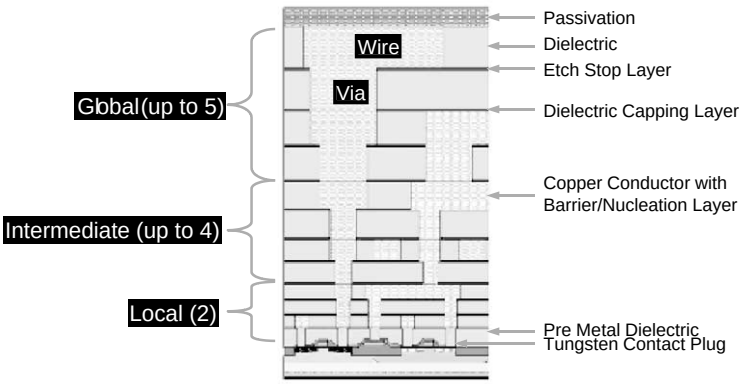


Fig. 4. Chip cross-section illustrating hierarchical interconnect scaling.

On the long term the device architecture for CMOS devices has to be modified in order to meet future device requirements. For example, non-standard double-gate MOSFET devices may have to be introduced as early as in the year 2007. This and other approaches of non-classical CMOS devices will be discussed in the 6th chapter.

Another issue concerning the frontend processing in general will be the introduction of silicon starting materials beyond 300 mm: For reasons of productivity enhancement, the introduction of the next generation wafer size of 450 mm is expected for the year 2014. Cost effective up-scaling of the incumbent Czochralzki crystal pulling and wafer slicing process is questionable and may need new solutions.

4. Interconnect issues

Fig. 4 depicts a typical chip cross-section with a metalization scheme illustrating the hierarchical scaling methodology with local wiring, intermediate wiring and global wiring resulting in up to 10 metalization levels in an advanced chip technology. The total interconnect length with active wiring excluding global levels will amount up to about 10.000 m/cm^2 chip area in the year 2005 and beyond. The increase in wiring length puts an enormous challenge to the constant reliability requirement in failures in time (FIT) values.

On the near term (next 5 years) the increasing effect of interconnect parasitic capacitances leads to the need for integrating interconnect dielectrics with low dielectric

YEAR TECHNOLOGY NODE	2010	2013	2016
DRAM ½ PITCH (nm) (SC. 2.0)	45	32	22
MPU/ASIC ½ PITCH (nm) (SC. 3.7)	45	32	22
MPU PRINTED GATE LENGTH (nm) (SC. 3.7)	25	18	13
MPU PHYSICAL GATE LENGTH (nm) (SC. 3.7)	18	13	9.0
Number of metal levels	**10**	**11**	**11**
Total interconnect length (m/cm^2) – active wiring only, excluding global levels (footnote for calculation)	**16063**	**22695**	**33508**
Local wiring pitch (nm)	**105**	**75**	**50**
Local A/R (for Cu)	**1.8**	**1.9**	**2.0**
Intermediate wiring pitch (nm)	**135**	**95**	**65**
Intermediate wiring dual damascene A/R (Cu wire/via)	**1.8/1.6**	**1.9/1.7**	**2.0/1.8**
Minimum global wiring pitch (nm)	**205**	**140**	**100**
Global wiring dual damascene A/R (Cu wire/via)	**2.3/2.1**	**2.4/2.2**	**2.5/2.3**
Cu thinning global wiring due to dishing (nm), 100 micron wide feature	**14**	**10**	**8**
Conductor effective resistivity (μΩ-cm) Cu intermediate wiring*	**2.2**	**2.2**	**2.2**
Barrier/cladding thickness (for Cu intermediate wiring) (nm)***	**5**	**3.5**	**2.5**
Interlevel metal insulator—effective dielectric constant (κ)	**2.1**	**1.9**	**1.8**
Interlevel metal insulator (minimum expected) —bulk dielectric constant (κ)	**<1.9**	**<1.7**	**<1.6**

Fig. 5. Long-term interconnect requirements for microprocessors.

constants. The corresponding k values will be decreasing from 3.6 today down to about 2 and below in the year 2007 and beyond. Due to severe material and integration problems the introduction of so-called low k dielectrics has been delayed in the ITRS 2001 edition as compared to the 1999 version. On the longer term the key challenges for interconnects will be the limited conductivity of the present conductor material copper. Fig. 5 highlights the requirements on wiring pitch, aspect ratio, conductor resistivity, barrier thickness and insulator dielectric value for microprocessors for the years 2010 to 2016. The numbers in red indicate that new solutions beyond the present technology have to be developed and introduced. Material innovation combined with traditional scaling will no longer satisfy the performance requirements. New innovative concepts in the areas of design, interconnect and packaging are needed to overcome the limited conductivity of the copper interconnect material in longer term. Alternative conductors may have to be introduced, as for example optical or RF conductors.

5. Material requirements

The future development of the IC industry puts forward major challenges to the material research scientists. Although silicon substrate materials will remain the dominant material in the IC industry for the next 15 years, both physical and technological limitations are demanding for the introduction of new materials both in the frontend as well as in the interconnect/backend processing area of the semiconductor technology. Fig. 6 highlights the key issues of new material requirements in silicon technology as outlined in the ITRS 2001. ASIC and microprocessor applications are pushing the material innovation in the gate stack and interconnect technology, whereas in the memory area the continuous scaling of memory cell sizes drives the introduction of high k dielectric materials for DRAMs and ferroelectric materials for Non-Volatile Memories. In lithography new materials will be required for imaging resists as well as for mask substrates and projection lens elements, as for example CaF_2 for 157 nm projection.

The silicon substrate itself has a variety of both mechanical and chemical requirements which get more demanding with further scaling of the semiconductor technology and the introduction of larger wafer sizes. Key numbers for those parameters are defined in the ITRS and summarized in Fig. 7. Mainly the defect specifications for layer structural defects, buried oxide defects and gate oxide integrity are getting very tight in future years, thereby challenging both the research scientist and the process engineer.

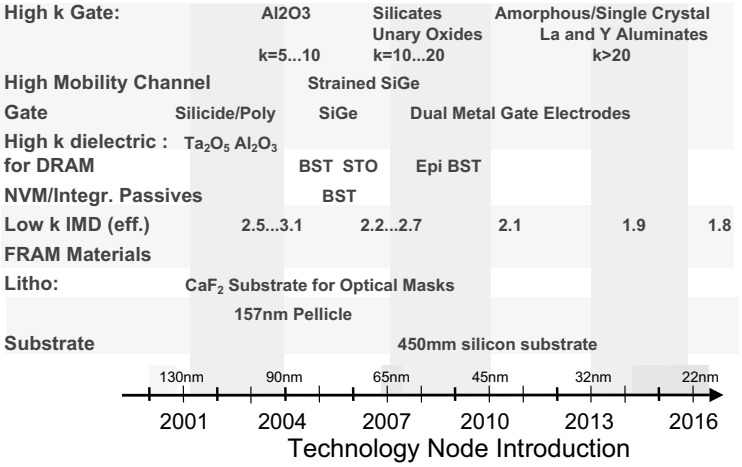


Fig. 6. Material requirements for front- and back-end processes.

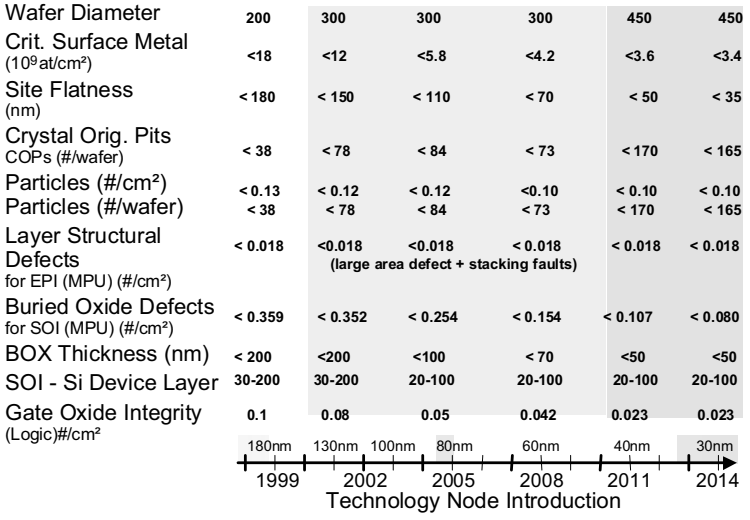


Fig. 7. Material requirements for silicon substrates.

6. Novel devices

The traditional scaling of classical CMOS devices leads to performance limitations which have to be overcome by introduction of new materials and improvements of the device design as has been mentioned in the 3rd chapter. However, planar conventional CMOS devices cannot be scaled to dimensions below 50 nm gate lengths without severely sacrificing performance. New, so-called "non-classical" device concepts are being developed for MOS devices to remove the barriers of conventional MOS transistor designs. An overview on some of these new-still CMOS-based-device concepts, their architectures, their advantages and challenges are described in Fig. 8. Whereas silicon-on-insulator (SOI) devices are already being introduced for high-performance applications, the implementation of less conventional MOS device architectures as for example vertical and double-gate transistors still need more engineering work for about 5–10 years, before all manufacturing issues will be solved.

7. Summary

The methodology and the hierarchical approach of the definition of future requirements of the IC industry in the ITRS have been described. Major limitations in overall chip performance as imposed by conventional CMOS scaling can be overcome by the introduction of new materials in both the frontend and interconnect processing area together with more sophisticated device

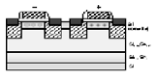
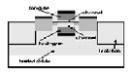
					
DEVICE	ULTRA-THIN BODY SOI	BAND-ENGINEERED TRANSISTOR	VERTICAL TRANSISTOR	FINFET	DOUBLE-GATE TRANSISTO
CONCEPT	Fully depleted SOI	SiGe or Strained Si channel; bulk Si or SOI	Double-gate or surround-gate structure (No specific temporal sequence forthese three structures is intended)		
APPLICATION/DRIVER	Higher performance, Higher transistor density, Lower power dissipation				
ADVANTAGES	-Improved subthreshold slope $-V_t$ controllability	-Higher drive current -Compatible with bulk and SOI CMOS	-Higher drive current Lithography independent L_g	-Higher drive current -Improved subthreshold slope -Improved short channel effect -Stacked NAND	-Higher drive current -Improved subthreshold slope -Improved short channel effect -Stacked NAND
SCALING ISSUES	-Si film thickness -Gate stack -Worse short channel effect than bulk CMOS	-High mobility film thickness, in case of SOI -Gate stack -Integration	-Si film thickness -Gate stack -Integrability -Process complexity -Accurate TCAD including QM	-Si film thickness -Gate stack -Process complexity -Accurate TCAD including QM effect	-Gate alignment -Si film thickness -Gate stack -Integrability -Process complexity -Accurate TCAD including QM effect
DESIGN CHALLENGES	-Device characterization -Compact model and parameter extraction	-Device characterization	-Device characterization -PD versus FD -Compact model and parameter extraction -Applicability to mixed signal applications		
MATURITY	Development				
TIMING	Near Future →				

Fig. 8. Cross sections and characteristics of non-classical CMOS devices.

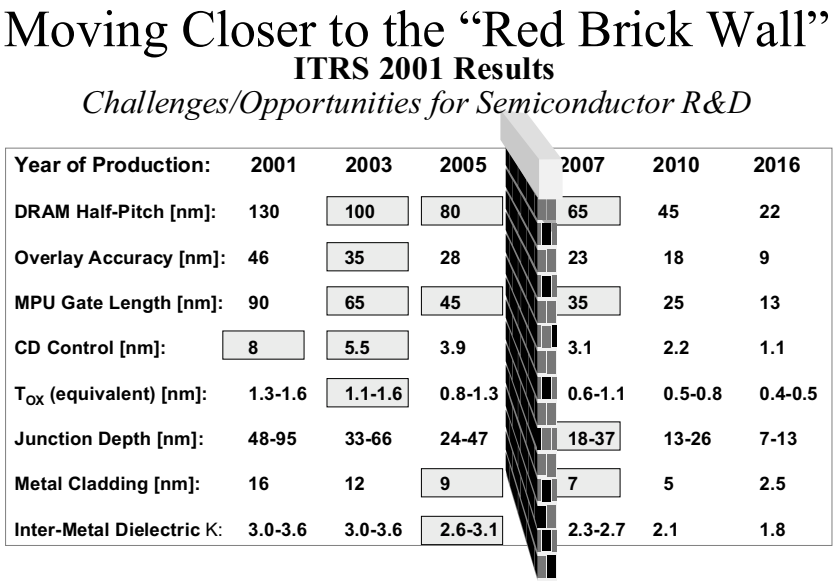


Fig. 9. "Red Brick Wall" illustrating key challenges in future silicon technology.

engineering. Some of the key challenges of the short- and long-term needs of the ITRS are summarized in Fig. 9. All major issues are being addressed in the research and development areas of the industry and of research consortia to meet these requirements. On the long term new non-classical CMOS-based devices will be

introduced to fulfil the continuous demand for performance increase and cost decrease of the IC industry. Silicon-based technology will be the mainstream semiconductor technology for at least the next 15 years.

Acknowledgements

The provision of some of the figures of this article by Toshitaka Fukushima, Fujitsu Corporation, Werner Klingenstein, Infineon Technologies, and the Semiconductor Industry Association, who has the copyright of the contents of the ITRS, is highly appreciated.

References

[1] ITRS Web-Site: http://public.itrs.net/