























































Inverter	Top-down	Bottom-up (Si nanowire)	Bottom-up (CNT)
Area	10R x 6R	3R x 3R	5R x 1R
Limited by	Wavelength	Assembly process	
Mask steps	6 mask process	1 mask process	2 mask process
Pros	Well established Simple structures and fabrication		
Cons	Complicated fabrication Low yield for assembly processes		
Future	Resolution can be 30 nm. ? (may be dominant under 10nm)		
ruluie	Nenewire		









•SEM image	oor deposition)
•SEM image	d PDMS stamp with combys reading b Catalysi transfer PDMS analysi transfer PDMS analysi transfer PDMS analysi transfer Catalysi transfer C
Cassell AM, et al. JACS 1999	cedure for CVD growth





Experimental procedure	
1) CNT	Case A
Growth	
Dispersion in surfactant by soni	cation and a second
2) Au lines	
Si wafer	1211110 (1211) (1211) (1211) (1211)
Oxidation	Statement Colored Statements
Au patterning	
Alkanethiol growth (SAM) in solu with evaporation	ution or
3) CNT assembly by self-assemb	oly and a second se
Single drop of CNT suspension	
Dry	Fig. 2, Electron micrographe of the nanotative attainguistics on octainant
4) Imaging	these encoding of dependent surfaces a network holding over their electronics com and a later dependent on key of year electronic lane (holding)
	Burghard M, et al. Advanced Materials. 1998.
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Comparison for assembly methods					
	Growth	Chemical patterning	E-field		
Purity demand	High	High	Low		
Patterning	Catalyst	Deposition area	Electrodes		
Temp./ time	>500∘C/ ~hrs.	room temp./ 1min	room temp./ 1min		
Sorting	Yes	No	Yes (electrical property & physical size)		
Potential for Waferscale fab.	Yes	Yes	Yes		
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