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Atom electronics: a proposal of atom/molecule switching devices

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Abstract

This paper proposes very fast (more than Tera (10^{12}) Hz) and very small (less than a few nm) devices, atom relay transistors (ART) and molecular single electron switching transistors (MOSES), which would supersede the MOSFET (metal-oxide-semiconductor field effect transistor) for future information processing. Their performances are evaluated on the basis of the characteristics necessary for integrated circuit devices and are found to be the most promising candidates among the nanoscale devices including quantum devices and superconductor devices. Atom/molecule manipulation technology by the scanning tunneling microscope (STM) would be the key factor to realize those devices. The basic technology developments toward the realization of ART and MOSES are reported, including the beam-assisted scanning tunneling microscope (BASTM) for insulator observation, needle formation and tip imaging (NFTI) for atomic-scale evaluation of the STM tip apex and micromachine STM (μ-STM) for single molecule manipulation and the atom wire fabrication technology development on a silicon (100) hydrogen terminated surface. © 1997 Elsevier Science B.V.

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1. Introduction

Advances in silicon ultra-large integrated circuit (ULSI) technology have been made possible by the downscaling of metal oxide semiconductor (MOS) transistors for higher performances [1]. The trend curves of MOS transistor downscaling and integration of large scale integrated circuits (LSIs) are shown in Fig. 1, in which device integration has increased by a factor of four every 3 years, while the minimum dimension has been reduced by a factor of 0.7 every 3 years. However, several physical and chemical limitations might prove to be obstacles to further microminiaturization beyond the 100 nm technology level [2]. Some of the major factors are listed below [3]:

(1) semiconductor limitation, i.e. p–n junction depletion region width of about 20–30 nm cannot be reduced;
(2) insulator limitation, i.e. insulator tunneling phenomena (below 4 nm for silicon dioxide) due to high electric field cannot be avoided;
(3) metal limitation, i.e. current density above 10^7 A cm^{-2} cannot be sustained by conventional metal materials;
(4) statistical error, i.e. a very small number of dopant would cause statistical fluctuation in a small doping area, such as a channel region and lead to the fatal variation in device characteristics;
(5) switching energy, i.e. as the device dimensions become smaller, the switching energy is also

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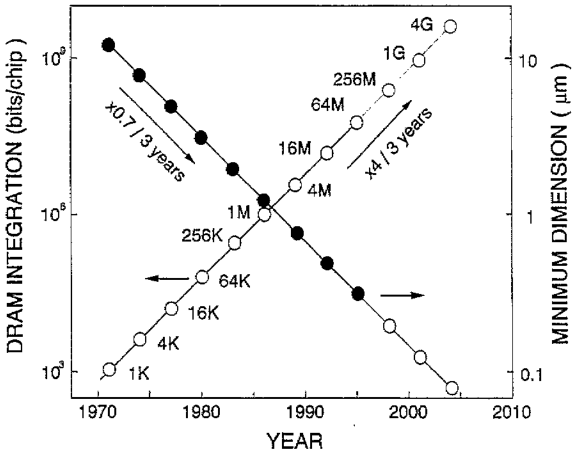


Fig. 1. Trend curves of MOS transistor and DRAM LSI integration: transistor size is shrunk 0.7 times every 3 years, whereas integration quadruples every 3 years.

reduced to reach the stage where quantum and thermal energy might cause errors in the device switching phenomena.

Innovative MOS transistor structures, it is claimed, make further downscaling possible [4], though the improvement would be by a factor of two at most. The trend curves shown in Fig. 1 also indicate that the minimum dimension of about 100 nm might be reached around the year of 2010. Therefore, nanoscale devices, such as quantum effect devices [5], have recently been attracting attention as candidates to replace silicon MOS transistors for future information processing integrated circuit devices. However, it is still uncertain whether those "quantum" devices will be able to replace MOS transistors because the characteristics of these devices are not necessarily be superior to those of MOS transistors, which are almost ideal as an information processing device, as will be shown later.

This paper proposes atom size switching devices, the atom relay transistor (ART) [3] and the molecular single electron switching transistor (MOSES) [6], as candidate devices to supersede MOS transistors with dimensions well below a few nm, and an operation speed of more than 10^{12} THz (T = Tera). Operation principles, simulated device characteristics and performance evaluation are shown as well as the technology development towards the realization of these devices.

2. Characteristics necessary for information processing devices

Generally, integrated circuit devices should fulfill the following requirements for high-performance information processing [3]. They are listed in the following:

(1) input and output (I/O) signal balance, i.e. the output of one device can directly drive the next device;
(2) I/O signal isolation, i.e. input and output are isolated, in other words, (more than) three terminal device;
(3) high switching speed, i.e. the switching speed of the device has to be much faster than that of the existing devices;
(4) dense integration capability, i.e. the separation between devices has to be very small, preferably the same dimension as the minimum device size;
(5) fabricability, i.e. devices should be very easily fabricated, in terms of process technologies.

Other factors, such as operation margin, noise immunity, power dissipation and reliability have to be taken into consideration in the integrated circuit design. Among these five factors, the high-switching speed has usually been the only criterion for evaluating newly proposed devices; however, it is essential to fulfill these five factors in a balanced manner. The reason why MOS transistors have been used in integrated circuits so far and are expected to be used down to their limit of around 100 nm is that they almost ideally fulfill the above five requirements. These requirements will be the basis of any future information processing devices, even if computer architecture is changed. For example, massively parallel computers will operate faster if the individual processor operates faster.

3. Atom/molecule switching devices – prospect for the future

This section explains the operation principles of ART and MOSES and considers whether the

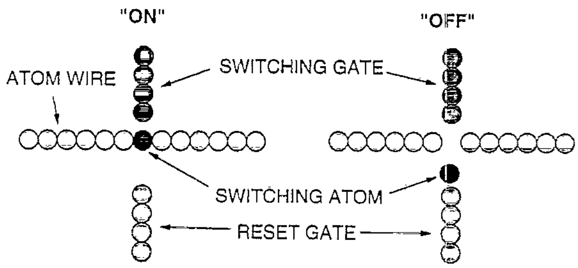


Fig. 2. Basic configuration of atom relay transistor (ART) [3].

proposed devices can fulfill the above mentioned five requirements.

3.1. *Atom relay transistor (ART)*

3.1.1. *Principle of operation*

The basic concept of ART [3] is schematically depicted in Fig. 2, in which an individual atom is represented by a circle. In the figure, ART is depicted as consisting of an atom wire, a switching atom, a switching gate and a reset gate. The operation principle is as follows. The atom wire is conductive (on) when the switching atom is set in the atom wire, and it is nonconductive (off) when the switching atom is removed from the atom wire [3]. The movement of the switching atom is made possible by the electric field supplied from the switching gate, and the first requirement of I/O balance for ART will be fulfilled. The on/off characteristics are simulated by the tight binding method and the results are depicted in Fig. 3 in which 250 atoms are arranged in a straight line with a separation of 0.2 nm. One electron is injected from the far left side of the atom wire

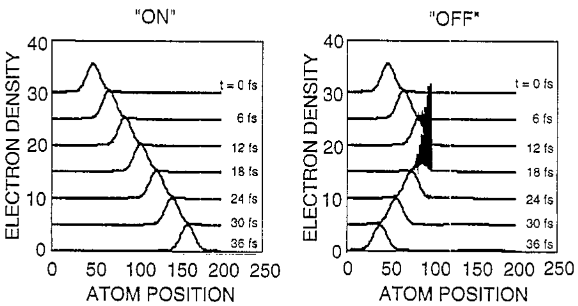


Fig. 3. Simulated "ON" "OFF" switching characteristics of ART [3].

with an electric field of 3×10^5 V cm^{-1}, and the electron density flowing in the atom wire is shown with a time interval of 6 fs. The results clearly indicate that ART exhibits on/off switching characteristics depending on the position of the switching atom. The second requirement, I/O signal isolation, is also fulfilled because ART is a three terminal device.

3.1.2. *Switching speed*

The switching speed of the switching atom from the "on" site to the "off" site, which corresponds to the switching frequency of ART, was simulated at around 30 THz by the first principle method [7]. The transmission velocity of the electric field also allows operation of ART at above 10 THz. Therefore the overall performance of ART should well exceed 10 THz. Thus the third condition, very high switching speed, has been fulfilled.

3.1.3. *Memory cell and logic circuits*

The basic configuration of ART shown in Fig. 2 suggests that ART can constitute a static memory cell by itself. In addition, ART offers dynamic operation using the self-relay configuration, in which the switching atom is removed from the atom wire by the electric field from the atom wire itself and electrons are trapped in the loop [8]. A dynamic memory cell uses only about 10^3 times the atom area, and a 10^9 bit occupies only about 200 μm square of area. The trapped electron might disappear through leakage passes such as insulator leakage, tunneling through the gap or radiation of light. A lifetime evaluation of the trapped electron would constitute a very interesting subject for scientific study. NAND and NOR gates are also designed [3], and a von Neumann-type computer can be constructed. Rule of thumb estimation of the area occupied by a 10^7 gate logic circuit and a 10^9 bit memory, which corresponds to almost the same integration as the state-of-the-art super-computers, results in a 20 μm square area and 200 μm square area, respectively. Therefore, the total area occupied by the ART supercomputer would be about 200 μm square, and even the longest signal delay on the chip would be well below the order of 10^{-12} s, which is short enough even for operation at more than 1 THz. Thus, the

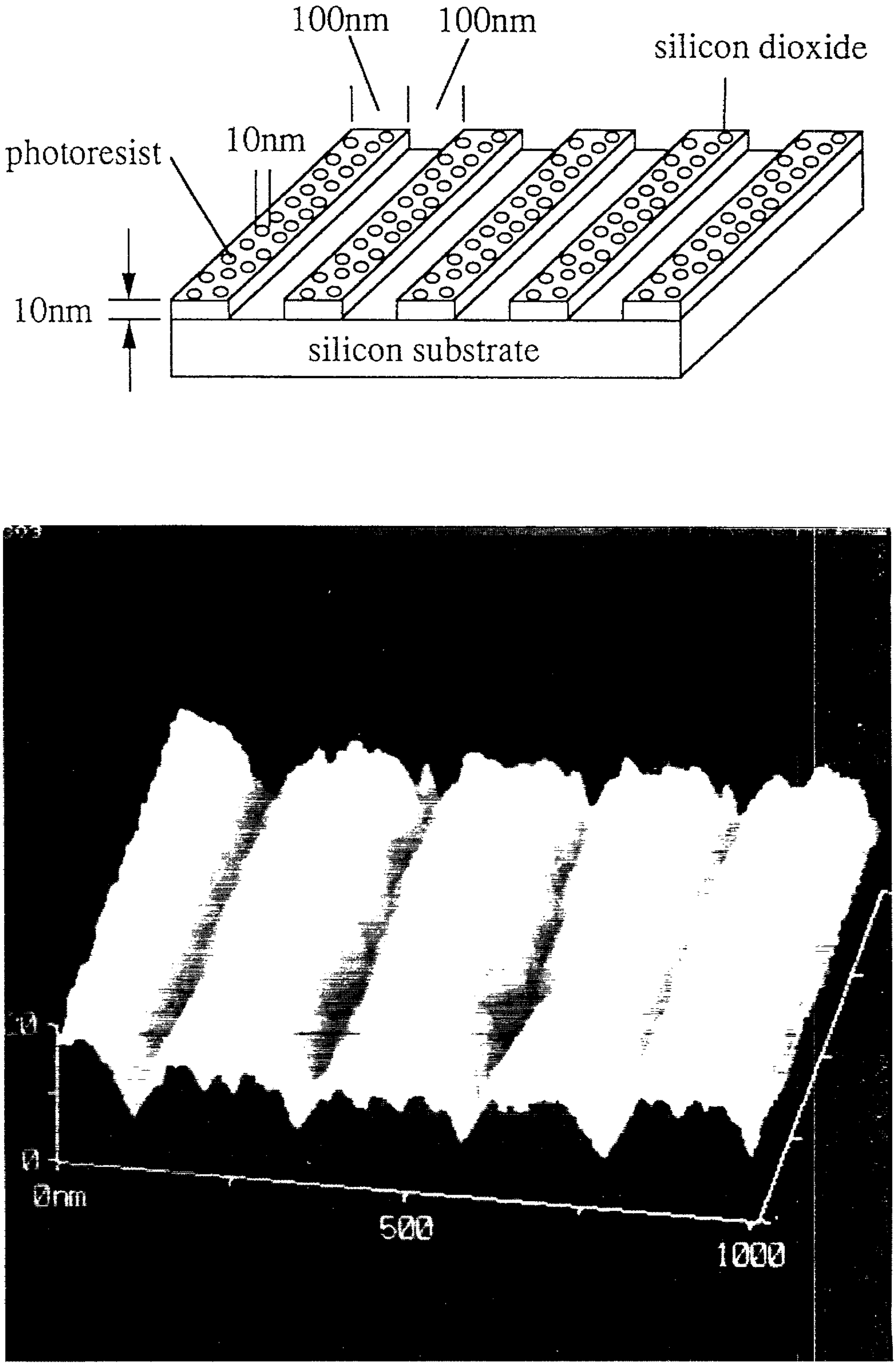


Fig. 4. BASTM observation of 100 nm wide and 10 nm thick silicon dioxide layers with 10 nm diameter resist dots on top.

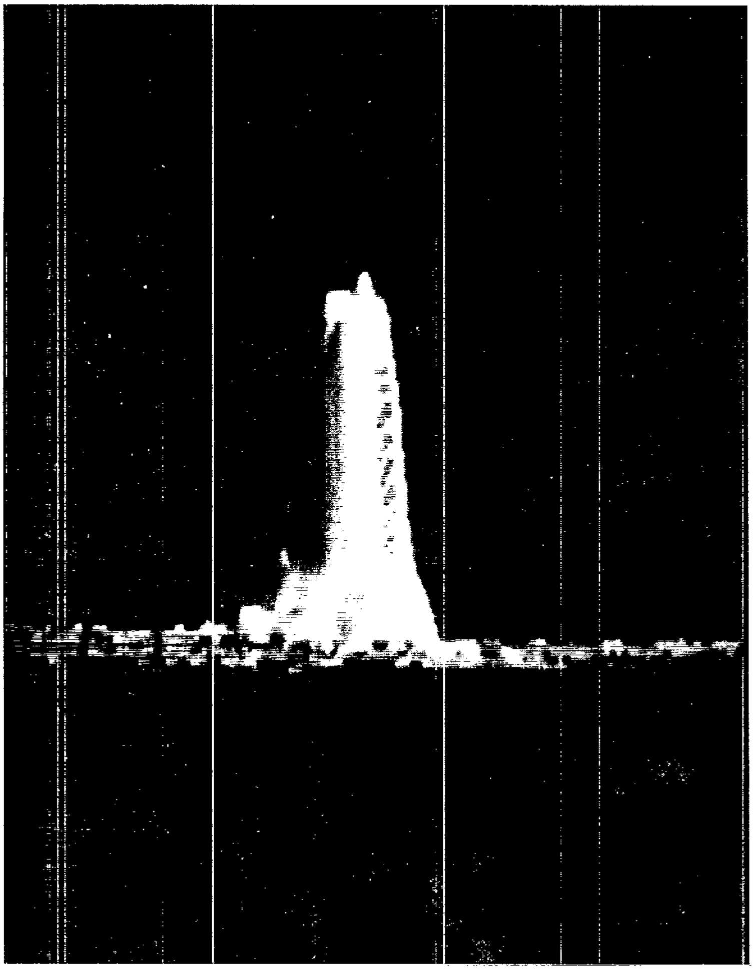


Fig. 5. Nano-needle structure formed by NFTI, the height and the diameter of which measure 9 and 1.5 nm, respectively.

fourth condition, dense integration, would be fulfilled.

3.1.4. Fabrication technologies of ART

Fabrication technologies of atom/molecule switching devices would be built on scanning probe technology such as a scanning tunneling microscope (STM) [9]. Here, the current fabrication technology development is described toward the materialization of atom electronics.

(1) *Beam-assisted STM (BASTM)*. In order to realize ART, it is necessary to manipulate individual atoms by, for example, STM. As already indicated in the literature, STM can manipulate the individual atom on a conducting solid surface [10]. Therefore, by using this technology, it should be possible to realize ART and the logic and memory circuits utilizing ART. However, ART has to be fabricated on an insulator substrate. STM can only observe and manipulate atoms on a conductor surface because it requires current flow between the tip and sample. The atomic force microscope (AFM) [11] was invented to overcome this problem; however, the resolution is not high enough to manipulate individual atoms. Beam-assisted STM (BASTM) [12] would be the most promising solution to this problem because of its capability for observation of insulators. A typical result is shown in Fig. 4, in which 100 nm wide and 10 nm thick silicon dioxide line and space

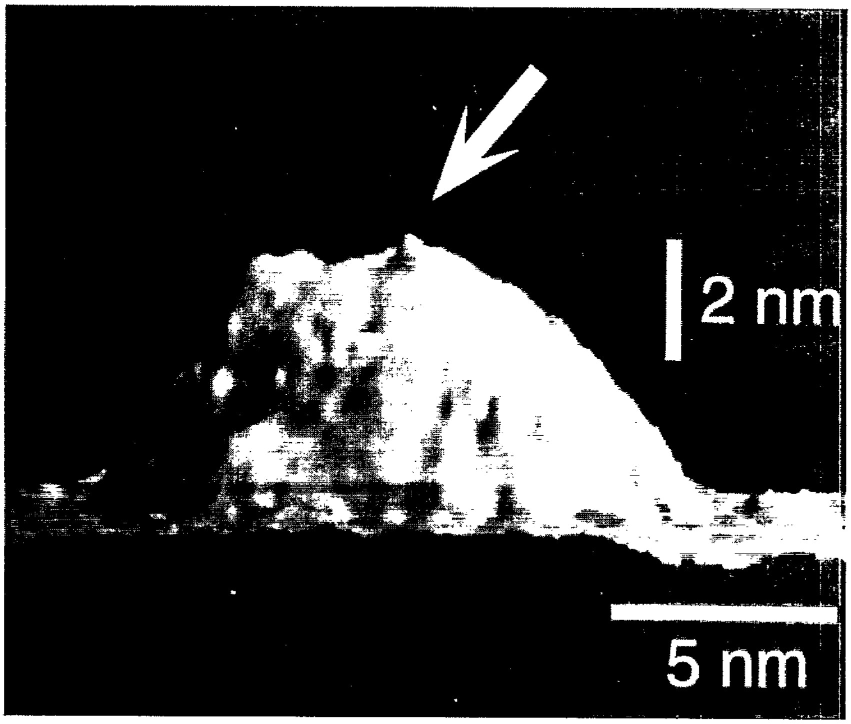


Fig. 6. Atomic resolution STM tip apex with an atomic protrusion on the tip apex, observed by NFTI.

patterns on a silicon substrate having about 10 nm-diameter organic resist dots are delineated. The operation principle is based on the activation of carriers in the insulator by an irradiating beam such as electron, ion and photon beams. Thermally grown silicon dioxide layers have been successfully evaluated by BASTM [13], which confirms the possibility of manipulating atoms on insulators.

(2) *Needle formation and tip imaging (NFTI).* In order to manipulate individual atoms by STM, it is necessary to use tips with a very controlled apex. The needle formation and tip imaging (NFTI) method [14,15] delineates the three-dimensional tip apex image and in-situ evaluation of the apex is made possible. The nano needle structure formed by NFTI is shown in Fig. 5, in which the diameter and height measure 1.5 and 9 nm, respectively. Using the nano needle as the probing tip, the STM tip apex structure was delineated, and the typical result is shown in Fig. 6. The atomic protrusion on the tip apex is clearly indicated, which made it possible to detect the surface structures at an atomic resolution [8]. The results shown in Fig. 6 are the first direct experimental evidence of the theoretical and experimental hypothesis that an atomic protuberance on the tip apex is indispensable to obtain an atomic resolution during STM observation of a surface.

(3) *Atom wire fabrication.* The first step to demonstrate the operation of ART would be to measure the conductance of an atom wire. The atom wire can be formed on a silicon (100) substrate by the following method [16]. The silicon (100) surface was cleaned by vacuum annealing and exposed to an atomic hydrogen stream generated by cracking hydrogen molecules by a hot ($\sim$2000 K) tungsten wire to form a hydrogen passivated surface as schematically shown in Fig. 7(a). One hydrogen row was removed by an STM modification method to construct a dangling bond wire as shown in Fig. 7(b). The dangling bond wire formed on the silicon (100) surface should be conductive because of the high electron density predicted by the first principle simulation [17] as shown in Fig. 8. In the figure, the high electron concentration region along the dangling

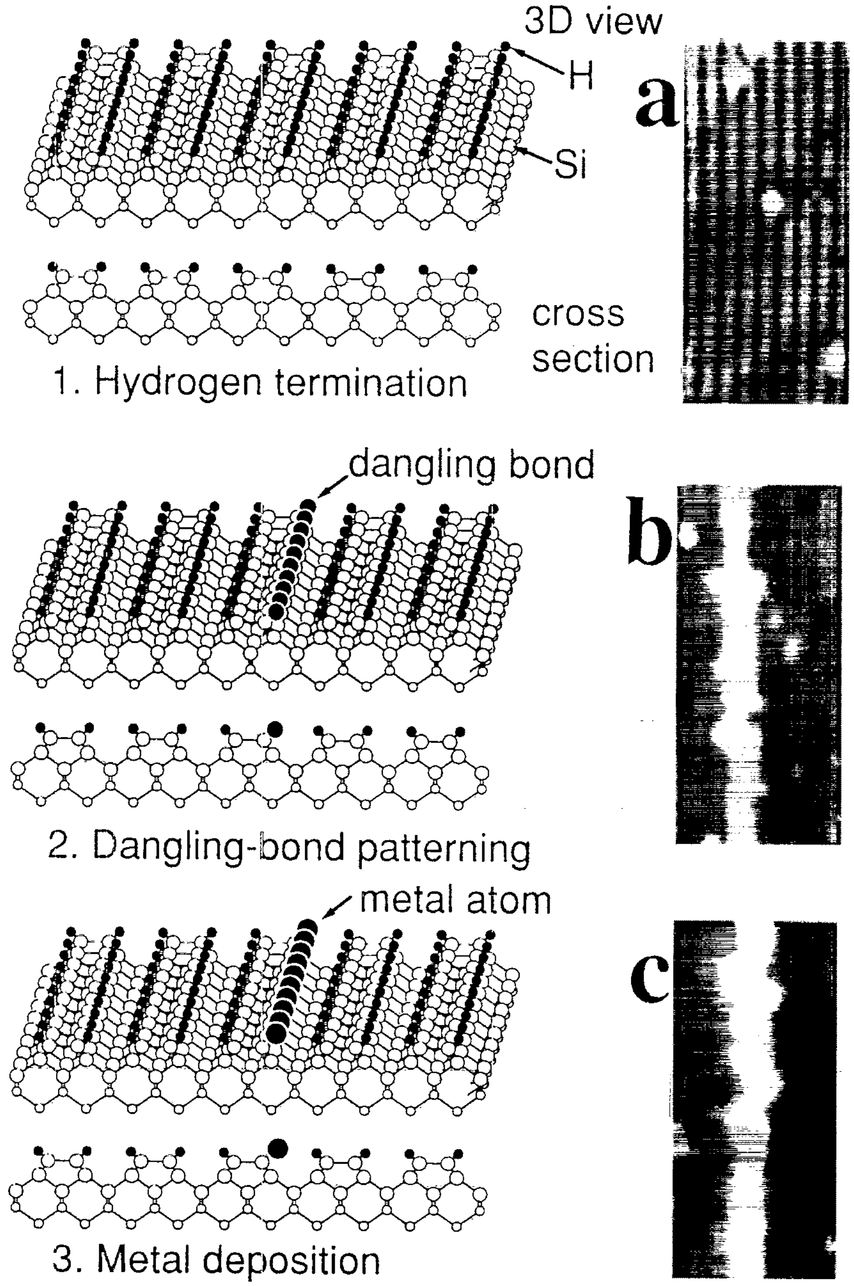


Fig. 7. Atom wire fabrication procedures on hydrogen passivated Si (100) surface: (a) hydrogen passivation; (b) dangling bond formation by STM; (c) metal line formation on the dangling bond wire.

bond wire and very sharp confinement of electron density across the wire are clearly depicted. Therefore, the wire can be conductive along the length direction, whereas it would be isolated from the adjacent wire perpendicular to the length direction. Tunneling spectroscopy (STS) of the dangling bond wire was experimentally verified as depicted in Fig. 9 [18]. In the figure, the dangling bond

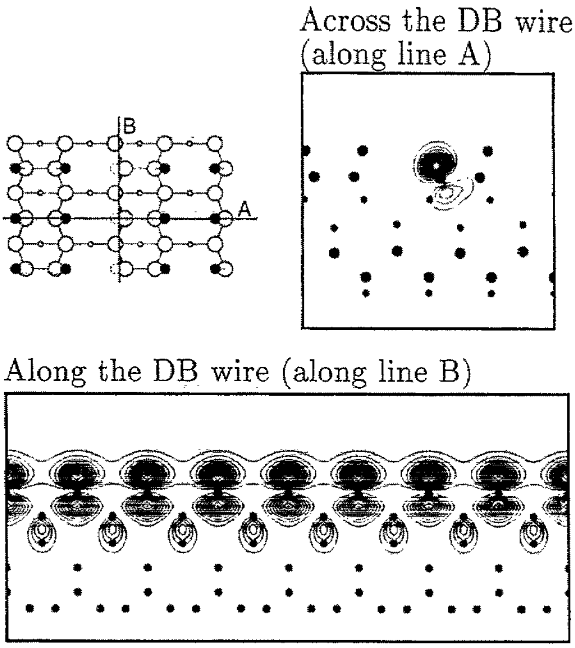


Fig. 8. Electron density distribution of a dangling bond wire formed on an Si(100)-H surface simulated by the first principle method.

wire was formed by removing the passivating hydrogen atoms one by one, thus forming an atomic wire indicated by the white dots in Fig. 9(a). The STS curve shown in Fig. 9(b) clearly depicts an metallic electron state in the dangling bond wire, whereas the hydrogen terminated region indicates insulating characteristics, thus confirming the theoretical prediction by the first principle method [17].

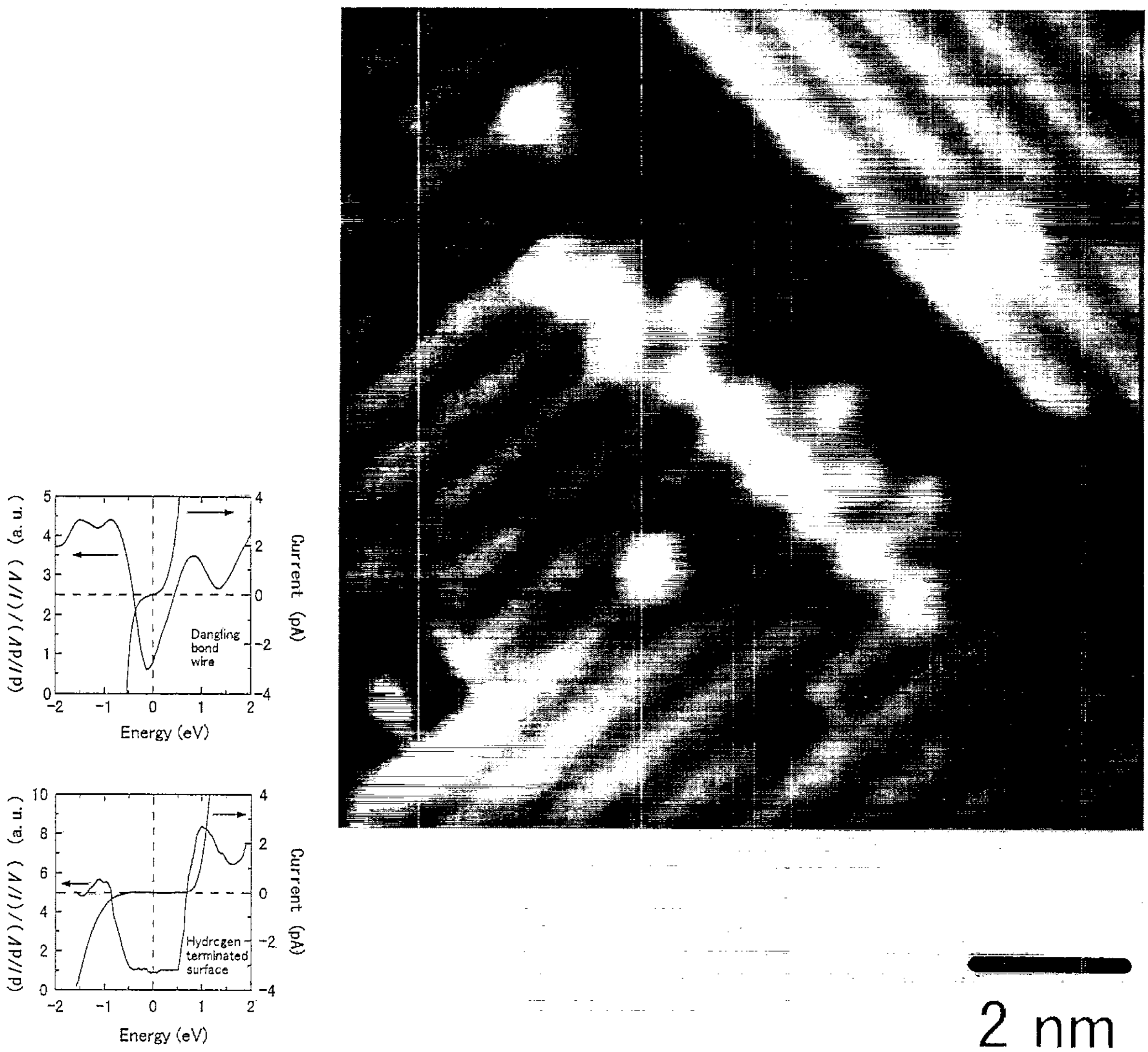
By applying metal atoms on the dangling bond structure and making the dangling bond wire into a metallic wire, the conducting wire would become more stable than the simple dangling bond wire. Therefore, the dangling bond wire shown in Fig. 7(b) was filled with gallium metal atoms by evaporating an appropriate amount of gallium atoms, as schematically indicated in Fig. 7(c). Because the activation energy for diffusion of gallium atoms on the hydrogen passivated silicon surface is very small, in the order of 100 meV [19], the gallium atoms stick to the dangling bonds selectively and spontaneously and form gallium wire. Thus, the conductance of a gallium single atom wire formed on dangling bonds can be measured if contact pads are formed on both ends of the wire [16].

3.2. *Molecular single electron switching transistor (MOSES)*

Molecular devices attracted much attention when they were proposed in 1980 by Carter [20]; however, the interest gradually faded due to several causes such as inaccessibility to individual molecules and the slow switching speed of molecules for an information processing device. Recent progress in single electron tunneling (SET) devices [21] attracts attention because of their potentially superior operation characteristics. The SET devices operate faster, if the quantum dot size is reduced to 1 nm [22]. However, fabrication as well as size control should become almost impossible by conventional fabrication technology in an nm regime. Molecular systems should realize much better dimensional control because the dimension of a molecule is determined by the number of bonds within the molecule.

3.2.1. *Principles of operation*

A molecular single electron switching transistor (MOSES) device consists of conducting polymer and insulating polymer, as schematically shown in Fig. 10 [6]. In the figure, polyacetylene and polyethylene molecules were chosen as typical conducting and insulating molecules, respectively. The insulator part acts as a tunnel barrier and the conducting polymer island as a quantum dot. The electron density of the polyacetylene–polyethylene –polyacetylene molecular structure was calculated by a molecular orbital (MO) method and the results are also demonstrated in Fig. 10. These results clearly indicate that the conduction electron density is negligible in the insulator (polyethylene) part while it is high in the conductor (polyacetylene) part of the molecule. Recently, a relatively solid and straight chain molecule has been proposed as a candidate for the conducting polymer [23]. Therefore, these molecules might be the candidates for realizing MOSES. In addition, three terminal MOSES devices should also be realizable



(a) (b)

Fig. 9. Tunneling spectrum (STS) (b) of the fabricated dangling bond wire (a), indicating a metallic electronic structure of the dangling bond wire.

by synthesizing an appropriate molecular structures [24] with branches, dots and gates.

3.2.2. Operation speed

The simulated ultimate operation speed of SET devices [22] indicates that the highest speed is in the order of 1 THz if the quantum dot size is less than 1 nm, and that the tunnel barrier width must also be very thin, i.e. less than 1 nm as shown in Fig. 11. For example, the size of a benzene ring, carbon double bond length and carbon single bond length measure about 0.242, 0.135 and 0.153 nm, respectively. Therefore, the size of MOSES can be controlled by selecting the appropriate molecular design, and molecules are likely to be the most appropriate material for realizing high-performance SET devices. The ultimate speed of a MOSES device should be of the order of 10 THz,

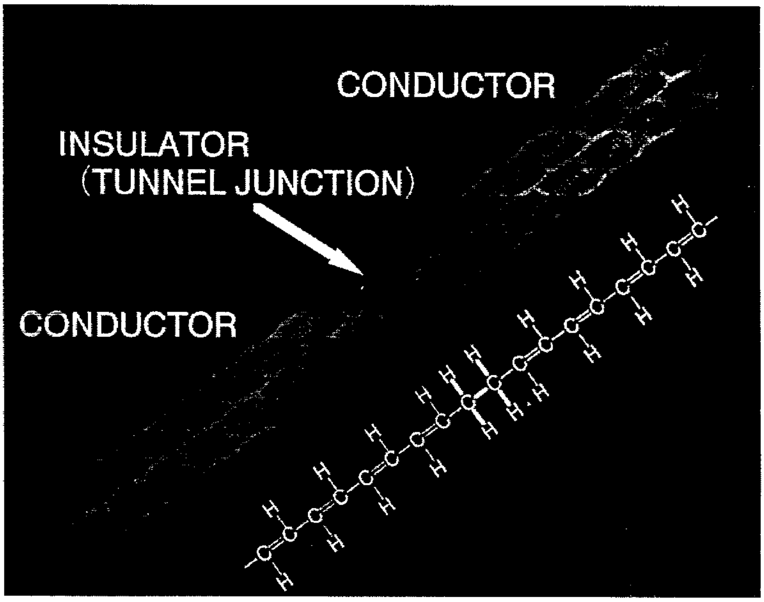


Fig. 10. Schematic figure and simulated electron density of an example of MOSES.

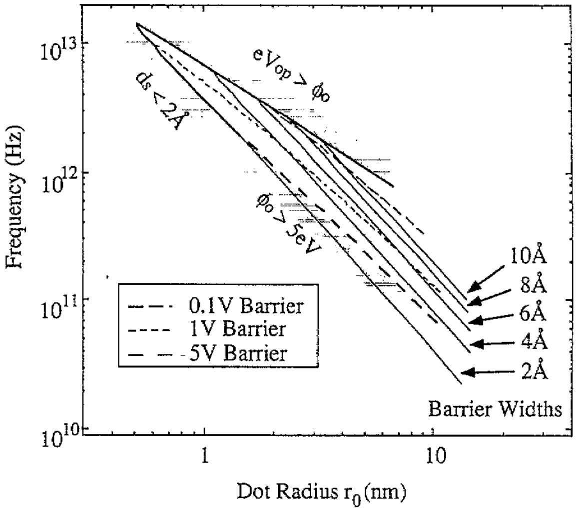


Fig. 11. Simulated ultimate operation speed of SET devices.

if the quantum dot size is reduced to about 0.3 nm, such as in the case of a benzene ring [22].

3.2.3. *Memory and logic circuits*

Memory and logic circuits can be formed by using MOSES devices, in which a conventional SET device and circuit design [25] can be applied. Therefore, no new circuit design should be necessary. Appropriate molecular design should achieve the necessary circuit characteristics, including multiple output wiring.

3.2.4. *Measurement technologies of MOSES devices*

The first major difficulty towards the realization of MOSES would be the access to individual molecules, as mentioned previously in this section. Recently, a novel micromachine scanning tunneling microscope (μ-STM) manipulation method was proposed, which is fabricated using a 0.4 μm ULSI fabrication technology [26]. A scanning electron microscope (SEM) micrograph of the fabricated μ-STM is shown in Fig. 12. The total size measures about 200 μm square, but the size can be made smaller by using smaller fabrication technologies. The vacuum tunneling gap between the μ-STM tip apex and the sample was successfully observed by a transmission electron microscope (TEM) as shown in Fig. 13 [26]. The two electrodes are made with gold, and thiol groups on both ends of the conducting molecule should easily make contacts to the gold electrodes. Therefore, the electrical conduction characteristics of the molecule should be reliably measurable and

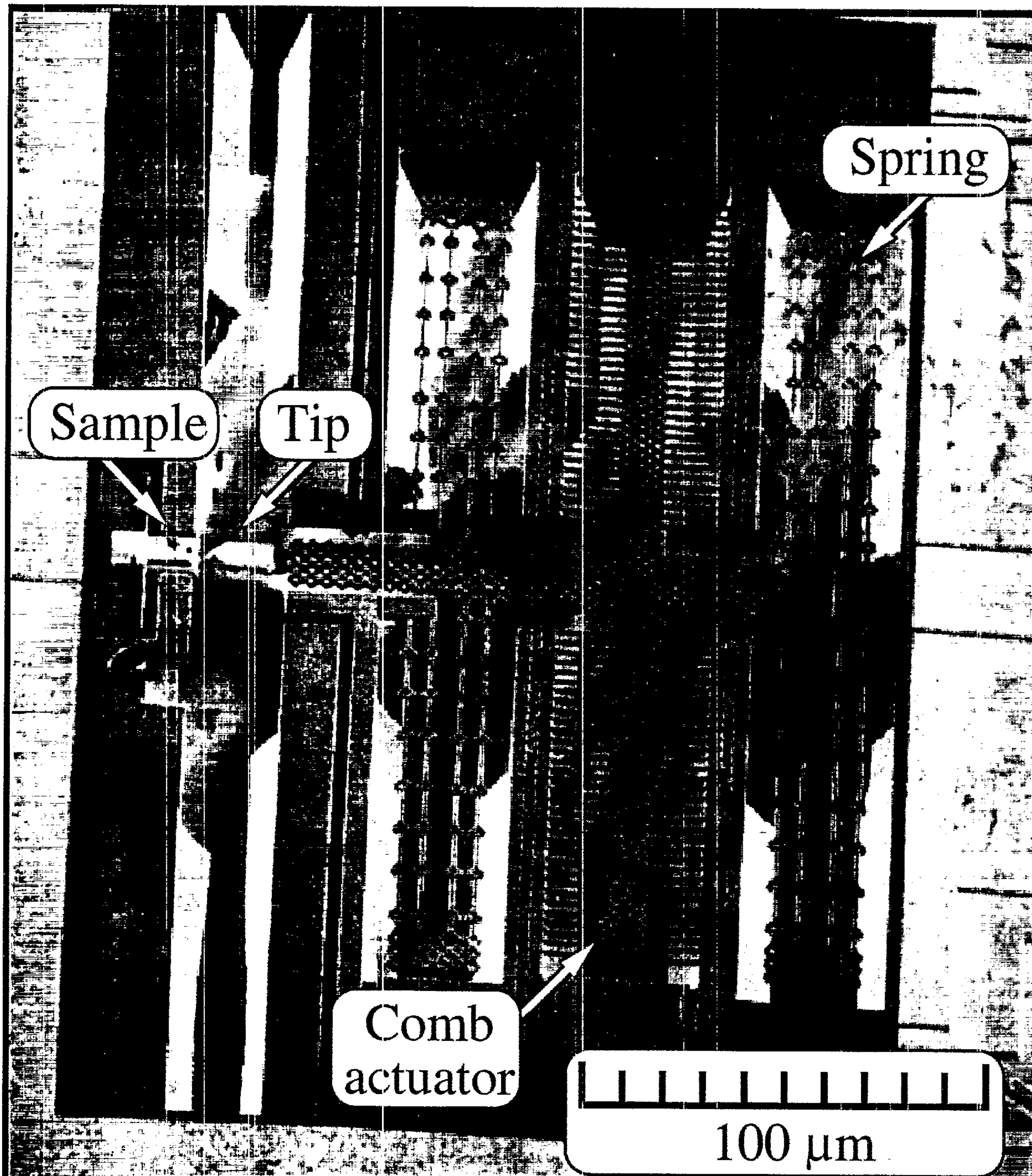


Fig. 12. SEM micrograph of the fabricated micromachine STM (μ-STM).

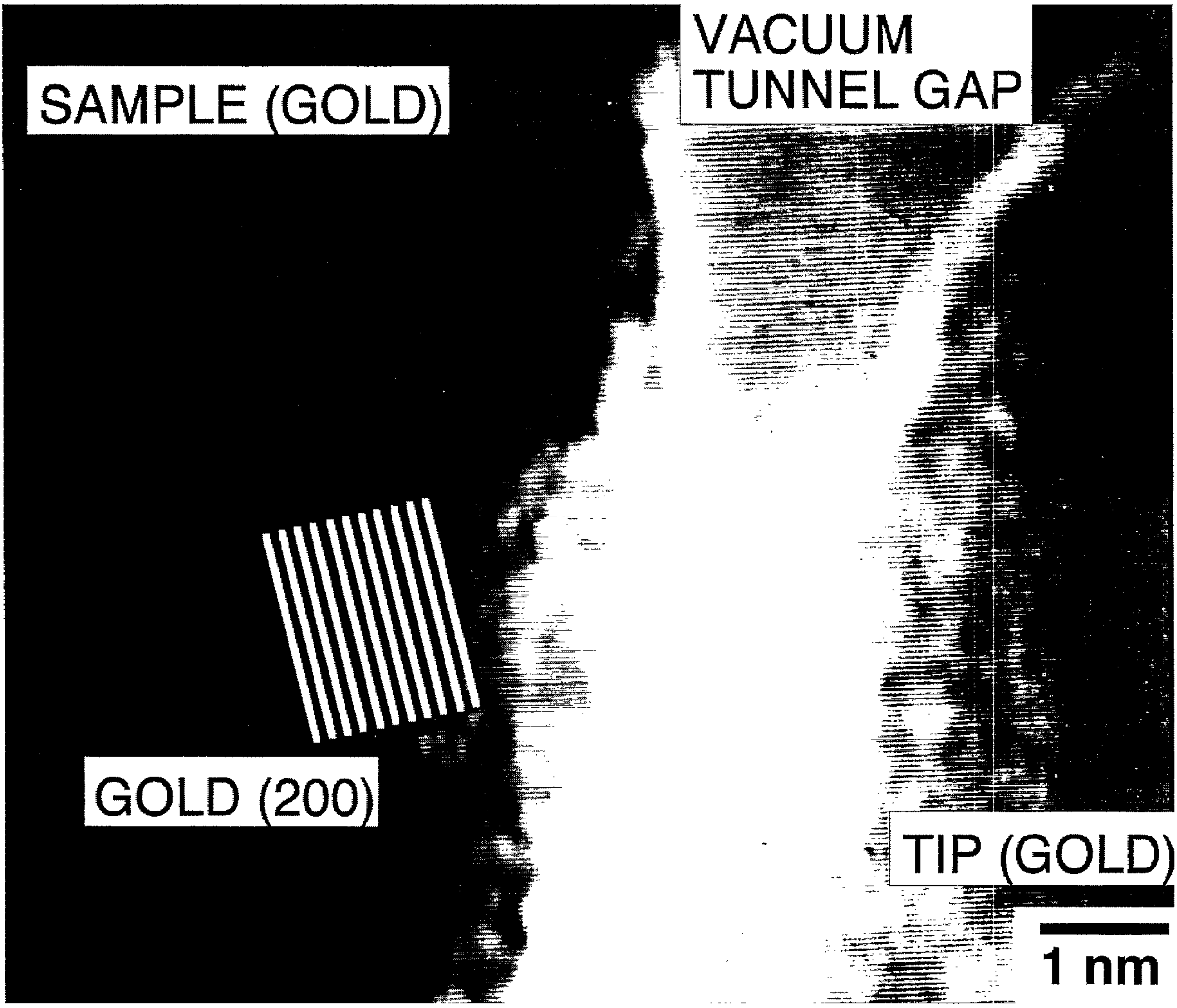


Fig. 13. TEM micrograph of the vacuum tunneling gap between the tip and sample of the μ-STM.

the high-performance operation of MOSES should be demonstrable.

4. Evaluation of candidate devices for the future

The candidate switching devices for the next decade, including quantum devices, conventional single electron devices, conventional molecular devices, ART and MOSES devices, were evaluated according to the five indispensable factors listed in Section 2, and the results are summarized in Table 1. It is indicated that MOS transistors almost ideally fulfill all the requirements, and that ART and MOSES are the most promising candidates to supersede them. The candidate nanoscale devices listed in Table 1, in addition to the historical information processing electron devices, were evaluated semi-quantitatively in terms of speed and integration capability, and the results are summarized in Fig. 14. Human beings started electronic information processing using a mechanical relay. The very slow and unreliable operation of the mechanical relay (mechanical electronics) was soon replaced by a vacuum tube [27] (vacuum electronics). Then the invention of transistors [28]

Table 1
Comparison of the performances of candidate information processing devices[a]

	MOS	Quantum device	Super conductor device	SET	Molecular device	ART	MOSES
I/O balance	○	▲	○	○	▲	○	○
I/O isolation	○	○	▲	○	▲	○	○
Speed	○	□	□	□	▲	□	□
Integration	○	○	○	○	□	□	□
Fabricability	○	▲	▲	▲	▲	▲	▲

[a] Key: □, excellent; ○, good; ▲, poor.

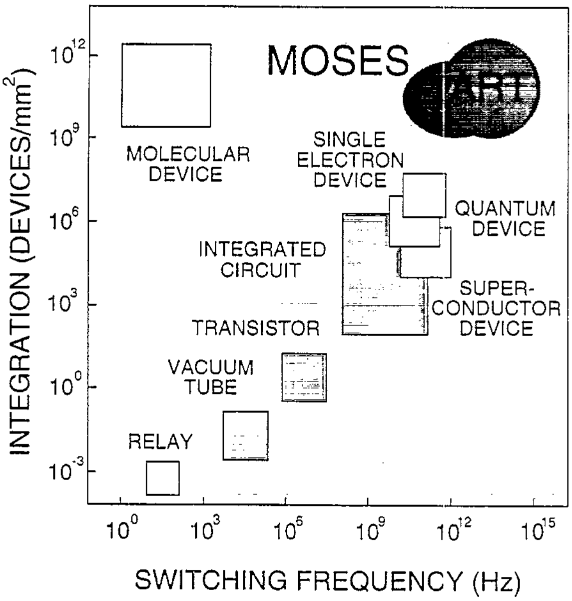


Fig. 14. Comparison of the switching speed and integration density of historical and candidate information processing devices after the MOS transistor era.

revolutionized the computer, and solid-state electronics devices, including integrated circuits [29] dominated electronic information processing. As indicated in Fig. 14, the innovation, or paradigm shift (e.g. from mechanical electronics to vacuum electronics to solid state electronics), has been accomplished because the performances of the latter devices are superior to those of preceding ones by at least two orders of magnitude.

Now that solid state electronics devices are approaching their limits, candidate devices are expected to supersede them. Conventional molecular devices exhibit very high integration density; however, their operating speed is extremely slow and they cannot be the prime candidates for future devices. Quantum devices demonstrate better characteristics in terms of integration and switching speed; however, they do not exhibit orders of magnitude higher switching speed or integration than the present silicon MOS transistors. Single-electron devices would have to be scaled down to less than 1 nm in order to obtain very high performance. Therefore ART and MOSES are likely to be the most promising candidate devices for future electronic information processing integrated circuits because of their potentially very fast operation speed and dense integration characteristics.

5. Conclusions

This paper proposed nanoscale switching devices, atom relay transistors (ART) and molecular single electron switching transistors (MOSES), for the next 20 years, with dimensions of only a few nm and an operational speed of more than 10 THz. The switching characteristics of ART were demonstrated by simulation. Fundamental logic circuits such as NAND and NOR gates and memory circuits were proposed, which can integrate a supercomputer in an area 200 μm square, with 10^7 gates of logic circuit and 10^9 bits of memory and operate at more than 1 THz. MOSES device structures were also demonstrated by simulation and very dense and fast operation characteristics were foreseen. New technologies, indispensable for the fabrication of these nanoscale devices, were demonstrated, including BASTM, NFTI and μ-STM. Experimental results to fabricate atom wire structures were also demonstrated. Various candidate nanoscale devices were evaluated on the basis of the characteristics necessary for future integrated circuit devices, and ART and MOSES devices were found to be the most promising devices for future information processing integrated circuits.

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