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# Conductive polymer interconnections for three-dimensional computing structures

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### Abstract

Research into 3D nanocomputing structures is important for the development of the next generation of computers. The main task in constructing a 3D chip stack is to vertically connect existing 2D chips. Hence we have developed molecular wiring technology which allows for high-density interconnections, and which will be appropriate for nanoelectronics. First we solve the problem of making wires between contact pads on two chips, but with no cross-talk between the pads. The chosen interconnect materials are conductive organic polymers, grown in the pores of insulating membranes. The growth of polymer in the membrane pores is investigated with the aim of achieving good conductivity through the pores, but with small cross-talk between them.

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### 1. Introduction

Three-dimensional architectures will be needed to provide the performance to implement computationally intensive tasks [1,2]. For example, the development of an image processing system with the abilities of the human visual cortex is now technically feasible, but it requires more than 10 teraflops of processing power. With present-day CMOS technology, the equipment would occupy more than 1 m<sup>3</sup> of volume, and dissipate several kW of power. The human visual cortex occupies 300 cm<sup>3</sup>, and dissipates about 2 W of power.

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Hence, this type of performance will only be achieved by advances in nanoelectronics and 3D structures, particularly by reducing interconnection lengths and increasing the bandwidth available between computational elements.

The first task on the road to the 3D chip stack is to have high-density, self-assembled molecular wires, which connect only the pads on two semiconductor chips or layers which are in vertical alignment, but with no 'diagonal' connectivity. In order to achieve this objective, we have examined the idea of developing a self-supporting insulating (macro)molecular based, 'charge transfer' layer, containing very many narrow conducting channels from one surface of the layer to the other, see Fig. 1. This would permit electrical contacts between pads on two chip layers. In particular, self-supporting polymer-based wiring layers were realized

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Fig. 1. (a) Two-chip stack with a polymerised membrane placed between the chips. (b) The cross-section showing the contacts. (c) The test rig (a multiple-axis translation/rotation system) allows the upper chip to be moved and positioned over the lower chip, which is mounted in a 40-pin chip carrier on a printed circuit board. Picture is not to scale. The membrane thickness is 10 μm.

in commercial filtration membranes. The conducting fibrils, formed by an organic polymer synthesized in the pores of the membranes, are not allowed to be interconnected, either inside the isolating material or along the surface. This would create short circuits between neighbouring signal channels. Therefore we investigated the growth of the polymer in porous membranes and developed strategies to produce high conductivity channels with low cross-talk.

### 2. Two-chip stack system

A possible way for functional modeling of complex structures with high-density 3D connections (such as the visual cortex) is a simple structure, with through-chip connections and molecular wires between the layers. Initial experimental work has focused on the formation of molecular wires to connect the layers vertically. We have designed a two-chip stack, see Fig. 1(a), which was fabricated (at TU Delft, [3]) and then specific molecular wiring materials were examined. Here we examine conductive polymers. Although we deal with simple chips incorporating electrode pads in the size range 300 µm down to 20 µm, the type of materials used allows for further downscaling for eventual use in nanoelectronic systems. Relatively large contact pads are used in order to achieve reliable measurements. Extrapolation of the results to much smaller electrode sizes is possible.

A special test rig has been designed and fabricated, Fig. 1(c), that allows the upper chip to be positioned over the lower chip and then pressed down onto the membrane, so that the molecular wires make contact with the metal pads on the chips. In order to reduce the contact resistance it was necessary to apply a high pressure on the upper chip. A possible solution to this could be to use a more elastic material instead of the polycarbonate membrane.

#### 3. Polymer wires

 $\pi$ -Conjugated polymers show promise as active materials in application areas such as microelectronics and photonics [4]. The conductive polymer material [5–7] used in this study was polypyrrole, which is a very stable and highly conductive material. The monomer pyrrole is a commercial product (Aldrich, 98%), which was pure and therefore not distilled prior to use. The synthesis of the polypyrrole can be realized either by electrochemical polymerisation (ECP) or by chemical polymerisation (CP).

For the ECP a metallic layer (Au) was first evaporated onto one side of the membrane with a thickness greater than the pore size to close the pores and to serve as an electrode in the ECP process. The ECP was performed at room temperature in a one-compartment cell with a Pt counter electrode and an Ag/AgCl reference electrode. The membrane was mounted on the cell so that the Au side was in contact with the flat cathode formed by a Si wafer. The solution contained 0.1 M pyrrole with 0.1 M LiClO<sub>4</sub> as an electrolyte. The polymer was grown potentiostatically at 0.8 V. To create a homogeneous growth over the whole membrane a short pulse of a higher voltage (2.5 V) was applied during the first 10 seconds. This pulse guaranteed that the polymer started to grow over the whole surface simultaneously. Without this additional process step the polymer grew only on those places where the membrane was in close contact with the cathode.

In the case of the CP, a membrane was used as a dividing wall in a two-compartment cell with one compartment containing an aqueous pyrrole solution and the other an oxidant reagent (FeCl<sub>3</sub>) solution. Purified water was used as the solvent for the polypyrrole (PPy) synthesis, and ferric chloride FeCl<sub>3</sub> was used as an oxidant. By diffusion of the monomer and the reagent through the membrane a polymer can be formed inside the membrane. The CP was performed at room temperature. The polymerisation time was varied between 3-11 min. After the polymerisation the membranes were removed from the cell and rinsed for several minutes with purified water. A number of tests were performed in the laboratory in order to obtain the best configuration for the two-compartment cell, and to achieve homogeneous polymerised membranes with the maximum number of pores filled with polypyrrole.

The membranes chosen for the experiments were 10  $\mu$ m thick polycarbonate membranes. We first used isopore membranes (Millipore) with different pore diameters (from 10  $\mu$ m down to 50 nm) to study the influence of the pore dimension on the conductivity, Fig. 2. However because these membranes have the intrinsic risk of pore interconnections, caused by a non-directional pore fabrication process, we also started to work with Nucleopore track-etch membranes from Whatman (same thickness and pore diameter of 100 nm). These membranes guaranteed a negligible amount of interconnections between the pores. However, the pore density of the membranes was quite low, between 6% and 9%.

The CP growth of the polymer through a membrane depends strongly on the pore size. In the large pores of 10 µm the polymer formed fibril networks which resembled polymer growth in a solution and give a relatively disordered aspect to the wires (Fig. 2(a)) with a small amount of polymer on the membrane surfaces for polymerisation times between 3-10 min. In the case of the 1.2 µm pores (Fig. 2(b)) a solid one phase polymer grew inside the pores, whereas for the 100 nm pores the polymer formed tubules which had varying diameters. As a consequence, the diffusion of the monomer and the reagent through the pores smaller than 10 µm was changed by the polymer which already existed in the pores and could easily create an interconnected polymer layer on the membrane surfaces for longer polymerisation times. Using an ECP process with a polymerisation time of 2–3 min, the growth was found to be non-uniform over a large area (Fig. 2(c)): polymer wires could be found sticking out of the membrane surface (4 on Fig. 2(c)) while other pores were either still unfilled (1-3 on Fig. 2(c)) or polymer wires had already formed interconnections (5 on Fig. 2(c)) over the surface. Fig. 2(d) shows details of interconnected wires for a process time of 4 min.

The conductivity and cross-talk measurements were carried out with the test system described in the previous section. The polymerised membranes were placed between the upper and lower chip (Fig. 1(a and b)) and by using I-V measurement the resistance of the membrane was obtained. A typical I-V measurement of the conductivity ( $\sigma_{\perp}$ ) and the cross-talk ( $\sigma_{\parallel}$ ) is shown in Fig. 3. The conductivity  $\sigma_{\perp}$  and  $\sigma_{\parallel}$  are calculated from the measured resistance (R) as

$$\sigma_{\perp,\parallel} = \frac{l}{RA},\tag{1}$$

where *l* is the membrane thickness for  $\sigma_{\perp}$  and the distances between the two pads for  $\sigma_{\parallel}$ , *A* is the surface area of the contact pads. In order to de-

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Fig. 2. SEM pictures of membranes filled with polypyrrole fibrils with pore size: (a)  $10 \mu$ m-view of one pore on the membrane surface, (b)  $1.2 \mu$ m-view of two pores on the membrane surface, (c)  $50 \mu$ commercies of a large membrane surface and (d)  $50 \mu$ m-view of interconnected wires on the membrane surface, (a) and (b) are CP processed membranes while (c) and (d) are ECP processed membranes.



Fig. 3. Typical *I–V* curves for the conductivity ( $\sigma_{\perp}$ —full squares) and cross-talk ( $\sigma_{\parallel}$ —open circles) measurements performed on the polypyrrole polymerised membranes, placed between upper and lower chip. Molecular wire length is 10 µm, and the membrane pore size is in the range from 10 µm down to 100 nm for different membranes (see Table 1).

termine  $\sigma_{\perp}$  and the cross-talk we used an insulating upper chip in the set up. In this configuration the current transport between two contact pads on the bottom chip can go only via interconnected conducting fibrils inside the membrane or via polymer depositions on the surface of the membrane. The cross-talk ratio is defined as:  $CTR = \sigma_{\perp}/\sigma_{\parallel}$ . The measurement results are shown in Fig. 3 and Table 1.

The origin of cross-talk in a polymerised membrane may be due to interconnected pores inside the membrane or to polymer deposits on the surface of the membrane which were created during the polymerisation process. The first problem could be solved by the use of track etched membranes, which have a negligible density of interconnected pores. Two possible ways to avoid polymer deposition on the surface were examined in our studies. The first was to control the growth of the polymer and the second was to use an ad-

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Conductivity values and the cross-talk ratio of CP (no. 1–3) and ECP (no. 4) processed membranes									
No.	$\sigma_{\perp}$ (S/cm)	$\sigma_{\parallel}$ (S/cm)	Cross-talk ratio	Remarks					
1a	$5  imes 10^{-1}$	$5.6  imes 10^{-3}$	98	$T_{\rm CP} = 3$ min, Millipore $d = 10 \ \mu {\rm m}$					
1b	$1  imes 10^{-2}$	$1.2 imes10^{-5}$	840	$T_{\rm CP} = 10 \text{ min}, \text{ Millipore } d = 10 \mu\text{m}$					
2a	$2.6  imes 10^{-2}$	$3.1  imes 10^{-3}$	9	$T_{\rm CP} = 11 \text{ min}, \text{ Millipore } d = 1.2 \ \mu \text{m}$					
2b	$1.4 imes10^{-3}$	$1.2 imes10^{-5}$	112	$T_{\rm CP} = 3$ min, Millipore $d = 1.2 \ \mu {\rm m}$					
3a	1	$1.8 imes10^{-2}$	55	$T_{\rm CP} = 8  {\rm min}$ , Whatman $d = 0.1  {\rm \mu m}$					
3b	$8 \times 10^{-2}$	$2  imes 10^{-4}$	400	$T_{\rm CP} = 2 \min$ , Whatman $d = 0.1 \ \mu m$					
4a	$5  imes 10^{-1}$	NA	NA	With Au film, Whatman $d = 100$ nm					
4b	$1 imes 10^{-4}$	$1 \times 10^{-5}$	10	As in 4a but Au film removed					
4c	$1.4 imes10^{-1}$	$3  imes 10^{-3}$	46	As in 4b + secondary ECP					

	Table I								
,	Conductivity	values and	the cross-talk	ratio of Cl	P (no. 1-3	) and ECP	(no. 4)	processed	membranes

 $T_{\rm CP}$  is the polymerisation time and d is the pore diameter.

ditional after treatment of the polymerised membranes. Polishing of the polymer filled membrane with diamond pastes or abrasive polyester films gave good results concerning the cross-talk ratio. Ultrasonic cleaning in an ethanol solution completely removed the polymer from the surface, which was verified by cross-talk measurements. As it is a 'soft' technique it should not damage the membrane and is therefore more suitable. However, cleaning the membrane surface causes the additional problem of poor contacts with the chip contact pads, which can be successfully treated by applying secondary ECP or by using specially designed contact pads [8].

#### 4. Conclusion

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Here we have tested an idea which would allow for 3D chip integration: to have self-assembled molecular wires, which connect only the pads on layers which are in vertical alignment, but with no diagonal connectivity. This was achieved experimentally and the concept was proved as viable.

Conducting channels were produced by polymerisation of pyrrole in the pores of commercial filtration membranes by ECP and CP techniques respectively. We investigated strategies to improve the performance towards an optimised self-supporting polymer-based wiring layer. The study of the polymer growth through the membrane gave interesting results towards a deeper understanding of the possibilities and limits for the design of conducting channels. We have demonstrated good values for the conductivity and cross-talk ratio using the track etched membranes.

Although the current work uses contact structures made by a conventional microelectronic process, the size of the polymer wires is constrained by the size of the pores in the membrane. Hence it should be possible to downscale the dimensions for use in 3D nanoelectronic computing structures, and indeed have 'true' molecular wires. The minimum pore size used so far of 30 nm, is already in the nanoscale region. Work is also continuing on the construction of a three chip stack.

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