16

MEMS Fabrication[1]

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[1]This chapter was originally published in Madou, M.J. (1997) "Wet Bulk Micromachining" and "Surface Micromachining" (chaps. 4 and 5), in *Fundamentals of Microfabrication*, CRC Press, Boca Raton, FL.

16.1 Wet Bulk Micromachining: Introduction

In wet bulk micromachining, features are sculpted in the bulk of materials such as silicon, quartz, SiC, GaAs, InP, Ge and glass by orientation-dependent (anisotropic) and/or by orientation-independent (isotropic) wet etchants. The technology employs pools as tools [Harris, 1976], instead of the plasmas studied in Madou (1997, chap. 2). A vast majority of wet bulk micromachining work is based on single crystal silicon. There has been some work on quartz, some on crystalline Ge and GaAs, and a minor amount on GaP, InP and SiC. Micromachining has grown into a large discipline, comprising several tool sets for fashioning microstructures from a variety of materials. These tools are used to fabricate microstructures either in parallel or serial processes. Madou (1997, Table 7.7) summarizes these tools. It is important to evaluate all the presented micromanufacturing methods before deciding on one specific machining method optimal for the application at hand—in other words, to zero-base the technological approach [Block, B., private communication]. The principle commercial Si micromachining tools used today are the well-established wet bulk micromachining and the more recently introduced surface micromachining (see Section 16.10). A typical structure fashioned in a bulk micromachining process is shown in Figure 16.1. This type of piezoresistive membrane structure, a likely base for a pressure sensor or an accelerometer, demonstrated that batch fabrication of miniature components does not need to be limited to integrated circuits (ICs). Despite all the emerging new micromachining options, Si wet bulk micromachining, being the best characterized micromachining tool, remains

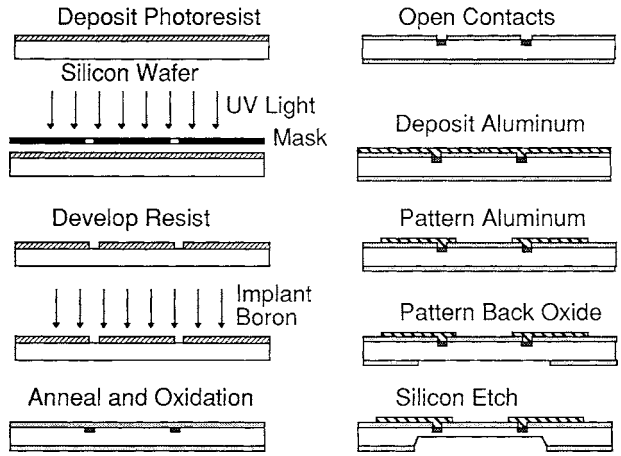


FIGURE 16.1 A wet bulk micromachining process is used to craft a membrane with piezoresistive elements. Silicon micromachining selectively thins the silicon wafer from a starting thickness of about 400 μm. A diaphragm having a typical thickness of 20 μm or less with precise lateral dimensions and vertical thickness control results.

most popular in industry. An emphasis in this chapter is on the wet etching process itself. Other machining steps typically used in conjunction with wet bulk micromachining, such as additive processes and bonding processes, are covered in Madou (1997, chaps. 3 and 8, respectively).

Wet bulk micromachining had its genesis in the Si IC industry, but further development will require the adaptation of many different processes and materials. To emphasize the need for micromachinists to look beyond Si as the ultimate substrate and/or building material, we have presented many examples of non-Si micromachinery throughout the book. The need to incorporate new materials and processes is especially urgent for progress in chemical sensors and micro-instrumentation which rely on non-IC materials and often are relatively large. The merging of bulk micromachining with other new fabrication tools such as surface micromachining and electroplating and the adaptation of new materials such as Ni and polyimides has fostered a powerful new, nontraditional precision engineering method. A truly multidisciplinary engineering education will be required to design miniature systems with the most appropriate building philosophy.

After a short historical note on wet bulk micromachining we begin this chapter with an introduction to the crystallography of single crystal Si and a listing of its properties, clarifying why Si is such an important sensor material. Some empirical data on wet etching are reviewed and different models for anisotropic and isotropic etching behavior follow. Then, etch stop techniques, which catapulted micromachining into an industrial manufacturing technique, are discussed. Subsequently, a discussion of problems associated with bulk micromachining such as IC incompatibility, extensive real-estate usage, and issues involving corner compensation is presented. Finally, examples of applications of wet bulk micromachining in mechanical and chemical sensors are given.

16.2 Historical Note

The earliest use of wet etching of a substrate, using a mask (wax) and etchants (acid-base), appears to be in the fifteenth century for ***decorating armor*** [Harris, 1976]. Engraving hand tools were not hard enough to work the armor and more powerful acid-base processes took over. By the early seventeenth century, etching to decorate arms and armor was a completely established process. Some pieces stemming from that period have been found where the chemical milling was accurate to within 0.5 mm. The masking in this traditional chemical milling was accomplished by cutting the maskant with a scribing tool and peeling the maskant off where etching was wanted. Harris (1976) describes in detail all of the improvements that, by the mid-1960s, made this type of chemical milling a valuable and reliable method of manufacturing. It is especially popular in the aerospace world. The method enables many parts to be produced more easily and cheaply than by other means and in many cases provides a means to design and produce parts and configurations not previously possible. Through the introduction of photosensitive masks by Niépce in 1822 [Madou, 1997, chap. 1], chemical milling in combination with lithography became a reality and a new level of tolerances came within reach. The more recent major applications of lithography-based chemical milling are the manufacture of printed circuit boards, started during the Second World War, and, by 1961, the fabrication of Si-integrated circuitry. Photochemical machining is also used for such precision parts as color television shadow masks, integrated circuit lead frames, light chopper and encoder discs, and decorative objects such as costume jewelry [Allen, 1986]. The geometry of a 'cut' produced when etching silicon integrated circuits is similar to the chemical-milling cut of the aerospace industry, but the many orders of magnitude difference in size and depth of the cut account for a major difference in achievable accuracy. Accordingly, the tolerances for fashioning integrated circuitry are many orders of magnitude smaller than in the chemical milling industry.

In this book we are concerned with lithography and chemical machining used in the IC industry and in microfabrication. A major difference between these two fields is in the aspect ratio (height-to-width ratio) of the features crafted. In the IC industry one deals with mostly very small, flat structures with aspect ratios of 1 to 2. In the microfabrication field, structures typically are somewhat larger and aspect ratios might be as high as 400.

Decorating armor. (From Harris, T. W., *Chemical Milling,* Clarendon Press, Oxford, 1976. With permission.)

Isotropic etching has been used in silicon semiconductor processing since its beginning in the early 1950s. Representative work from that period is the impressive series of papers by Robbins and Schwartz (1959, 1960) and Schwartz and Robbins (1961, 1976) on chemical isotropic etching, and Uhlir's paper on electrochemical isotropic etching [Uhlir, 1956]. The usual chemical isotropic etchant used for silicon was HF in combination with HNO_3 with or without acetic acid or water as diluent [Robbins and Schwartz, 1959; 1960; Schwartz and Robbins, 1961; 1976]. The early work on isotropic etching in an electrochemical cell (i.e., 'electropolishing') was carried out mostly in nonaqueous solutions, avoiding black or red deposits that formed on the silicon surface in aqueous solutions [Hallas, 1971]. Turner showed that if a critical current density is exceeded, silicon can be electropolished in aqueous HF solutions without the formation of any deposits [Turner, 1958].

In the mid-1960s, the Bell Telephone Laboratories started the work on anisotropic Si etching in mixtures of, at first, KOH, water and alcohol and later in KOH and water. This need for high aspect ratio cuts in silicon arose for making dielectrically isolated structures in integrated circuits such as for beam leads. Chemical and electrochemical anisotropic etching methods were pursued [Stoller and Wolff, 1966; Stoller, 1970; Forster and Singleton, 1966; Kenney, 1967; Lepselter, 1966; 1967; Waggener, 1970; Kragness and Waggener, 1973; Waggener et al., 1967a; 1967b; Bean and Runyan, 1977]. In the mid-1970s, a new surge of activity in anisotropic etching was associated with the work on V-groove and U-groove transistors [Rodgers et al., 1976; 1977; Ammar and Rodgers, 1980].

The first use of Si as a micromechanical element can be traced back to a discovery and an idea from the mid-1950s and early 1960s, respectively. The discovery was the large piezoresistance in Si and Ge by Smith in 1954 [Smith, 1954]. The idea stems from Pfann et al. in 1961 [Pfann, 1961], who proposed a diffusion technique for the fabrication of Si piezoresistive sensors for stress, strain and pressure. As early as 1962 Tufte et al. (1962), at Honeywell, followed up on this suggestion. By using a combination of a wet isotropic etch, dry etching and oxidation processes, Tufte et al. made the first thin Si piezoresistive diaphragms, of the type shown in Figure 16.1, for pressure sensors [Tufte et al., 1962]. Sensym/National Semiconductor (sold to Hawker Siddley in 1988) became the first to make stand-alone Si sensor products

Some Private California MEMS Companies

1972	Foxboro ICT (called SenSym ICT since 1999)
1972	SenSym (called SenSym ICT since 1999)
1975	Endevco
1975	IBM Micromachining
1976	Cognition (sold to Rosemount in 1978)
1980	Irvine Sensors Corp.
1981	ChemIcon Inc.
1981	Microsensor Technology (sold to Tylan in 1986)
1982	ICSensors (sold to EG&G in 1994)
1982	Transensory Devices (sold to ICSensors in 1987)
1985	NovaSensor (sold to Lucas in 1990)
1986	Captor (sold to Dresser in 1991)
1987	Aura
1988	Nanostructures
1988	Redwood Microsystems
1988	TiNi Alloys
1989	Abaxis
1989	Advanced Recording Technologies
1991	Incyte Genomics
1991	Sentir
1992	Silicon Microstructures
1993	Affymetrix
1993	Fluid IC (dissolved in 1995)
1993	Nanogen
1993	Silicon Micromachines
1994	Berkeley Microsystems Incorporated (BMI)
1995	Aclara Biosciences
1995	Integrated Micromachines
1995	MicroScape
1996	Caliper
1996	Cepheid
1997	Microsensors
1997	Mycometrix
1998	Quantum Dot
1998	Zyomyx
1999	Symyx

(1972). By 1974, National Semiconductor described a broad line of Si pressure transducers, in the first complete silicon pressure transducer catalog [Editorial, 1974]. Other early commercial suppliers of micromachined pressure sensor products were Foxboro/ICT, Endevco, Kulite and Honeywell's Microswitch. Other micromachined structures began to be explored by the mid- to late-1970s: Texas Instruments produced a thermal print head (1977) [Editorial, 1977]; Hewlett Packard made thermally isolated diode detectors (1980) [O'Neill, 1976]; fiberoptic alignment structures were made at Western Electric [Boivin, 1974]; and IBM produced ink jet nozzle arrays (1977) [Bassous et al., 1977]. Many ***Silicon Valley microsensor companies*** played and continue to play a pivotal role in the development of the market for Si sensor products.

European and Japanese companies followed the U.S. lead more than a decade later; for example, Druck Ltd. in the U.K. started exploiting Greenwood's micromachined pressure sensor in the mid-1980s [Greenwood, 1984].

Petersen's 1982 paper, extolling the excellent mechanical properties of single crystalline silicon, helped galvanize academia to get involved in Si micromachining in a major way [Petersen, 1982]. Before that time most efforts had played out in industry and practical needs were driving the technology (market pull). The new generation of micromachined devices often constitutes gadgetry only, and the field is perceived by many as a technology looking for applications (technology push). It has been estimated that

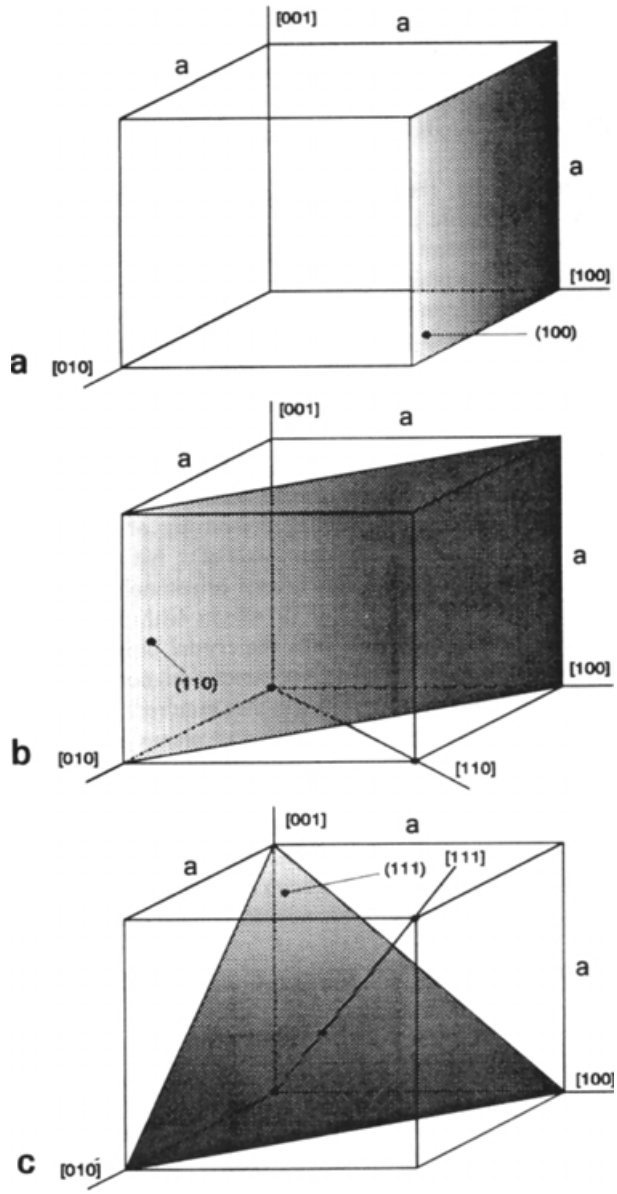


FIGURE 16.2 Miller indices in a cubic lattice: planes and axes. Shaded planes are: a (100), b (110), c (111).

today there are more than 10,000 scientists worldwide involved in Si sensor research and development [Middlehoek and Dauderstadt, 1994]. In order to justify the continued investment, it has become an absolute priority to understand the intended applications better and to be able to select a more specific micromachining tool set intelligently and to identify large market applications [Madou, 1997, chap. 10].

16.3 Silicon Crystallography

16.3.1 Miller Indices

The periodic arrangement of atoms in a crystal is called the lattice. The unit cell in a lattice is a segment representative of the entire lattice. For each unit cell, basis vectors (a_1, a_2 and a_3) can be defined such that

if that unit cell is translated by integral multiples of these vectors, one arrives at a new unit cell identical to the original. A simple cubic-crystal unit cell for which $a_1 = a_2 = a_3$ and the axes angles are $\alpha = \beta = \gamma = 90°$ is shown in Figure 16.2. In this figure, the dimension 'a' is known as the lattice constant. To identify a plane or a direction, a set of integers h, k and l called the Miller indices is used. To determine the Miller indices of a plane, one takes the intercept of that plane with the axes and expresses these intercepts as multiples of the basis vectors a_1, a_2, a_3. The reciprocal of these three integers is taken, and, to obtain whole numbers, the three reciprocals are multiplied by the smallest common denominator. The resulting set of numbers is written down as (hkl). By taking the reciprocal of the intercepts, infinities (∞) are avoided in the plane identification. A direction in a lattice is expressed as a vector with components as multiples of the basis vectors. The rules for determining the Miller indices of an orientation are: translate the orientation to the origin of the unit cube and take the normalized coordinates of its other vertex. For example, the body diagonal in a cubic lattice as shown in Figure 16.2 is 1a, 1a and 1a or a diagonal along the [111] direction. Directions [100], [010] and [001] are all crystallographically equivalent and are jointly referred to as the family, form or group of <100> directions. A form, group or family of faces which bear like relationships to the crystallographic axes—for example, the planes (001), (100), (010), $(00\bar{1})$, $(\bar{1}00)$ and $(0\bar{1}0)$—are all equivalent and they are marked as {100} planes. For illustration, in Figure 16.3, some of the planes of the {100} family of planes are shown.

16.3.2 Crystal Structure of Silicon

Crystalline silicon forms a covalently bonded structure, the diamond-cubic structure, which has the same atomic arrangement as carbon in diamond form and belongs to the more general zinc-blend classification [Kittel, 1976]. Silicon, with its four covalent bonds, coordinates itself tetrahedrally, and these tetrahedrons make up the diamond-cubic structure. This structure can also be represented as two interpenetrating face-centered cubic lattices, one displaced (1/4,1/4,1/4)a with respect to the other, as shown in Figure 16.4. The structure is face-centered cubic (fcc), but with two atoms in the unit cell. For such a cubic lattice, direction [hkl] is perpendicular to a plane with the three integers (hkl), simplifying further discussions about the crystal orientation, i.e., the Miller indices of a plane perpendicular to the [100] direction are (100). The lattice parameter 'a' for silicon is 5.4309 Å and silicon's diamond-cubic lattice is surprisingly wide open, with a packing density of 34%, compared to 74% for a regular face-centered cubic lattice. The {111} planes present the highest packing density and the atoms are oriented such that three bonds are below the plane. In addition to the diamond-cubic structure, silicon is known to have several stable high-pressure crystalline phases [Hu et al., 1986] and a stress-induced metastable phase with a wurtzite-like structure, referred to as diamond-hexagonal

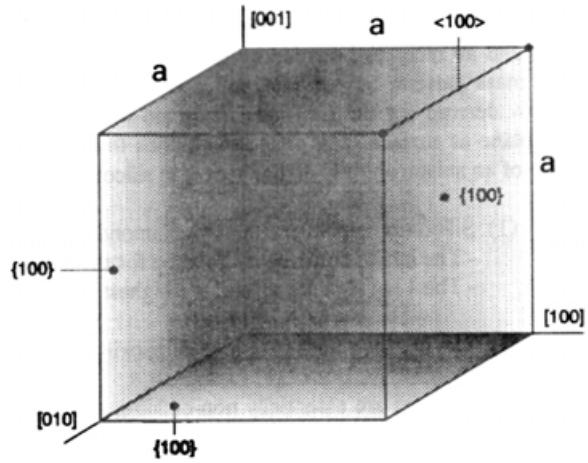


FIGURE 16.3 Miller indices for some of the planes of the {100} family of planes.

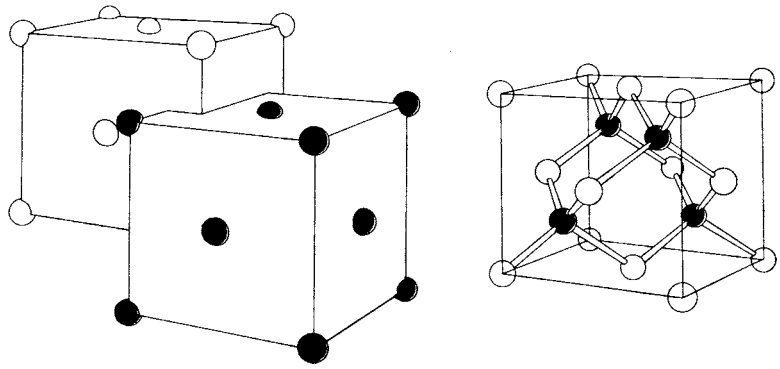


FIGURE 16.4 The diamond-type lattice can be constructed from two interpenetrating face-centered cubic unit cells. Si forms four covalent bonds, making tetrahedrons.

silicon. The latter has been observed after ion-implantation [Tan et al., 1981] and hot indentation [Eremenko and Nikitenko, 1972].

When ordering silicon wafers, the crystal orientation must be specified. The most common orientations used in the IC industry are the <100> and <111> orientation; in micromachining, <110> wafers are used quite often as well. The <110> wafers break or cleave much more cleanly than other orientations. In fact, it is the only major plane that can be cleaved with exactly perpendicular edges. The <111> wafers are used less, as they cannot be etched anisotropically except when using laser-assisted etching [Alavi et al., 1992]. On a <100> wafer, the <110> direction is often made evident by a flat segment, also called an orientation flat. The precision on the flat is about 3°. The position of the flat on (110)-oriented wafers varies from manufacturer to manufacturer, but often parallels a (111) direction. Flat areas help orientation determination, placement of slices in cassettes and fabrication equipment (large primary flat), and help identify orientation and conductivity type (smaller secondary flat; see Madou [1997, chap. 3, Si growth]). Primary and secondary flats on <111> and <100> silicon wafers are indicated in Figure 16.5.

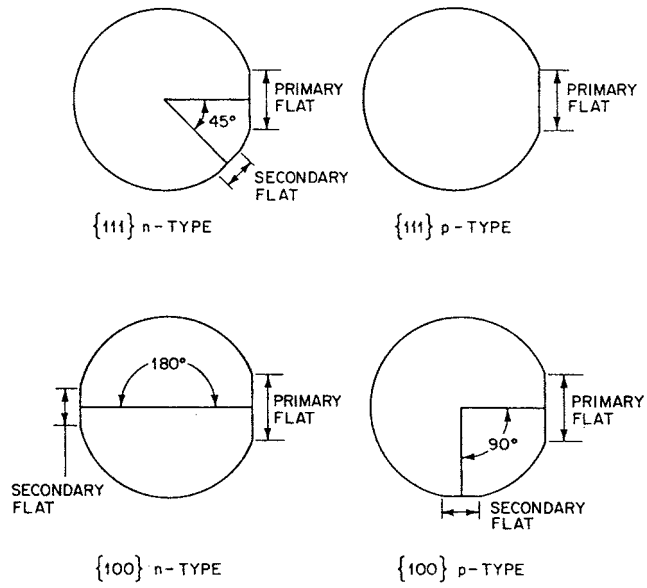


FIGURE 16.5 Primary and secondary flats on silicon wafers.

16.3.3 Geometric Relationships between Some Important Planes in the Silicon Lattice

To better appreciate the different three-dimensional shapes resulting from anisotropically etched single crystal Si (SCS) and to better understand the section further below on corner compensation, some of the more important geometric relationships between different planes within the Si lattice need further clarification. We will consider only silicon wafers with a (100) or a (110) as the surface planes. We will also accept, for now, that in anisotropic alkaline etchants the {111} planes, which have the highest atom-packing density, are nonetching compared to the other planes. As the {111} planes are essentially not attacked by the etchant, the sidewalls of an etched pit in SCS will ultimately be bounded by this type of plane, given that the etch time is long enough for features bounded by other planes to be etched away. The types of planes introduced initially depend on the geometry and the orientation of the mask features.

16.3.3.1 [100]-Oriented Silicon

In Figure 16.6, the unity cell of a silicon lattice is shown together with the correct orientation of a [100]-type wafer relative to this cell [Peeters, 1994]. It can be seen from this figure that intersections of the nonetching {111} planes with the {100} planes (e.g., the wafer surface) are mutually perpendicular and lying along the <110> orientations. Provided a mask opening (say, a rectangle or a square) is accurately aligned with the primary orientation flat, i.e., the [110] direction, only {111} planes will be introduced as sidewalls from the very beginning of the etch. Since the nonetching character of the {111} planes renders an exceptional degree of predictability to the recess features, this is the mask arrangement most often utilized in commercial applications. During etching, truncated pyramids (square mask) or truncated V-grooves (rectangular mask) deepen but do not widen (Figure 16.7). The edges in these structures are <110> directions, the ribs are <211> directions, the sidewalls are {111} planes and the bottom is a (100) plane parallel with the wafer surface. After prolonged etching, the {111} family of planes is exposed down to their common intersection and the (100) bottom plane disappears, creating a pyramidal pit (square mask) or a V-groove (rectangular mask) (Figure 16.7). As shown in Figure 16.7, no underetching of the

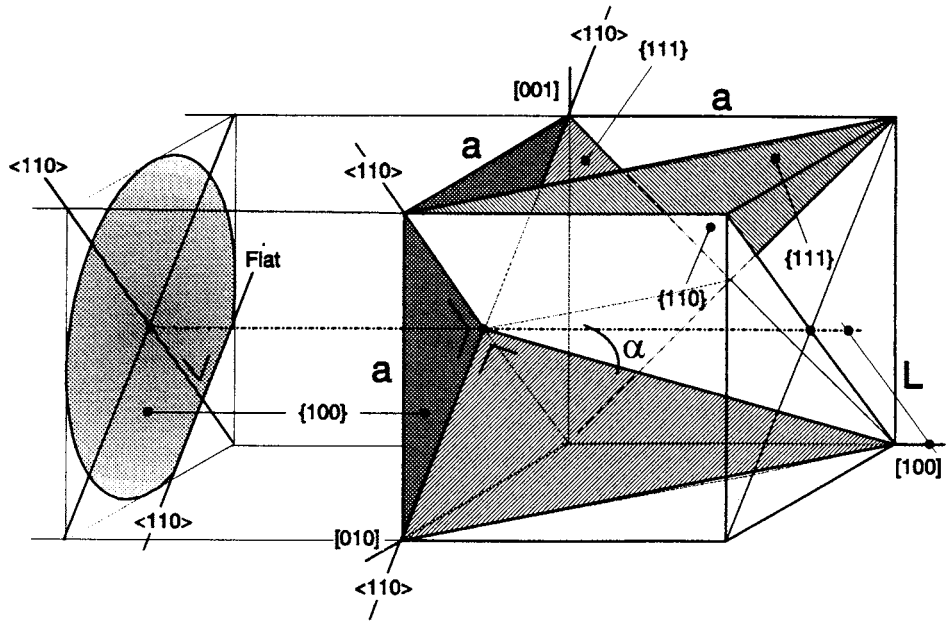


FIGURE 16.6 (100) silicon wafer with reference to the unity cube and its relevant planes. (From Peeters, E., *Process Development for 3D Silicon Microstructures with Application to Mechanical Sensor Design,* KUL, Belgium, 1994. With permission.)

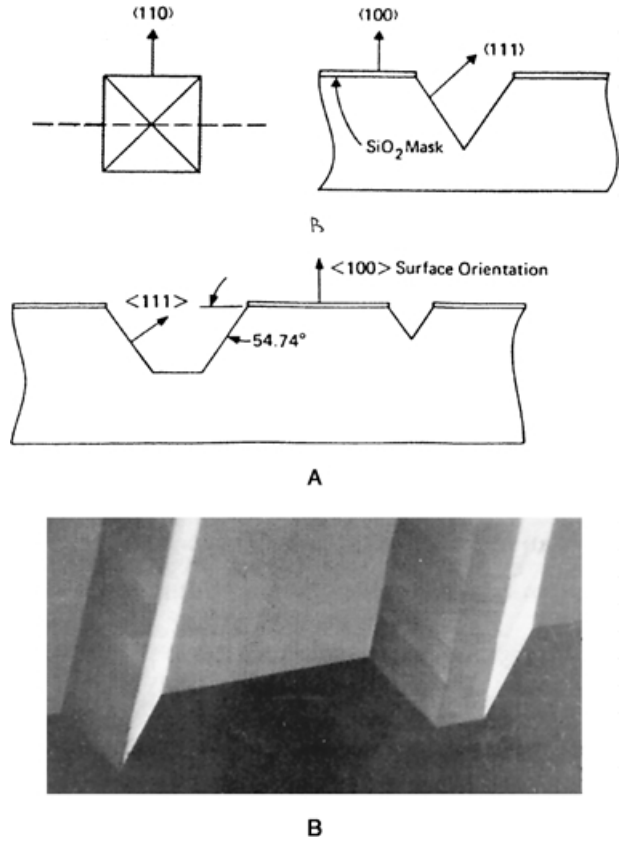


FIGURE 16.7 Anisotropically etched features in a (100) wafer with (A) Square mask (schematic) and (B) Rectangular mask (scanning electron microscope micrograph of resulting actual V- and U-grooves).

etch mask is observed, due to the perfect alignment of the concave oxide mask opening with the <110> direction. Misalignment still results in pyramidal pits, but the mask will be undercut. For a mask opening with arbitrary geometry and orientation (for example, a circle) and for sufficiently long etch times, the anisotropically etched recess in a {100} wafer is pyramidal with a base perfectly circumscribing the circular mask opening [Peeters, 1994]. Convex corners (>180°) in a mask opening will always be completely undercut by the etchant after sufficiently long etch times. This can be disadvantageous (for example, when attempting to create a mesa rather than a pit) or it can be advantageous for undercutting suspended cantilevers or bridges. In the section of this chapter on corner compensation, the issue of undercutting will be addressed in detail. The slope of the sidewalls in a cross section perpendicular to the wafer surface and to the wafer flat is determined by the angle α as in Figure 16.6 depicting the off-normal angle of the intersection of a (111) sidewall and a (110) cross-secting plane, and can be calculated from:

$$\tan\alpha = \frac{L}{a} \tag{16.1}$$

with $L = a \times \frac{\sqrt{2}}{2}$ or $\alpha = \arctan \frac{\sqrt{2}}{2} = 35.26°$, or 54.74° for the complementary angle. The tolerance on this slope is determined by the alignment accuracy of the wafer surface with respect to the (100) plane. Wafer manufacturers typically specify this misalignment to 1° (0.5° in the best cases).

The width of the rectangular or square cavity bottom plane, W_0, in Figure 16.8, aligned with the <110> directions, is completely defined by the etch depth, z, the mask opening, W_m, and the above-calculated sidewall slope:

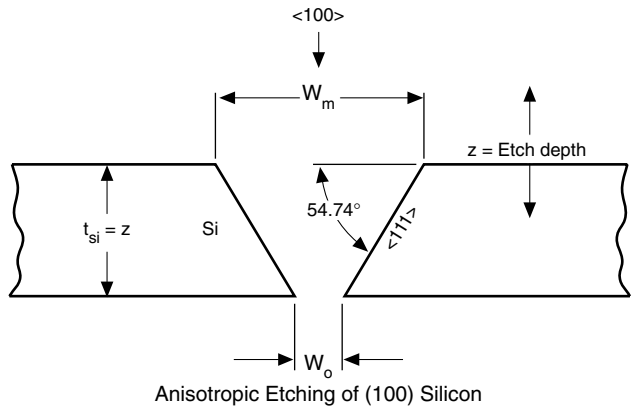


FIGURE 16.8 Relation of bottom cavity plane width with mask opening width.

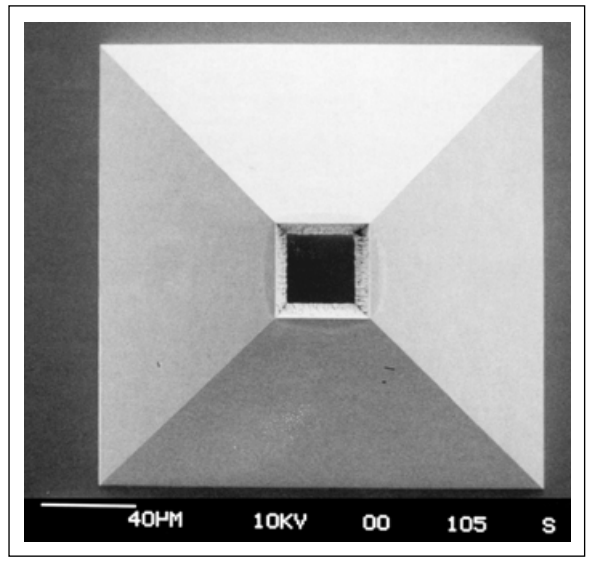
$$W_0 = W_m - 2\text{cotan}(54.74^\circ)z$$

or

$$W_0 = W_m - \sqrt{2}\, z \tag{16.2}$$

The larger the opening in the mask, the deeper the point at which the {111} sidewalls of the pit intersect. The etch stop at the {111} sidewalls' intersection occurs when the depth is about 0.7 times the mask opening. If the oxide opening is wide enough, $W_m > 849$ μm (for a typical 6-in. wafer with thickness $t_{si} = z = 600$ μm), the {111} planes do not intersect within the wafer. The etched pit in this particular case extends all the way through the wafer, creating a ***small orifice*** or ***via***. If a high density of such vias through the Si is required, the wafer must be made very thin.

Corners in an anisotropically etched recess are defined by the intersection of crystallographic planes, and the resulting corner radius is essentially zero. This implies that the size of a silicon diaphragm is very well defined, but it also introduces a considerable stress concentration factor. The influence of the zero corner radius on the yield load of diaphragms can be studied with finite element analysis (FEA).



Orifice (A via through Si wafer).

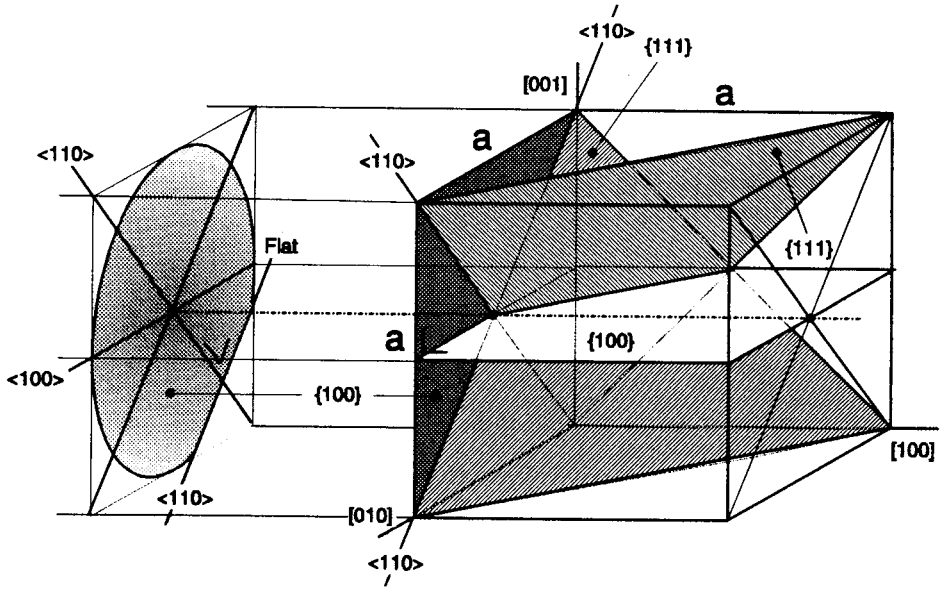


FIGURE 16.9 (100) silicon wafer with <100> mask-aligned features introduces vertical sidewalls. (From Peeters, E., *Process Development for 3D Silicon Microstructures with Application to Mechanical Sensor Design,* KUL, Belgium, 1994. With permission.)

One way to obtain vertical sidewalls instead of 54.7° sidewalls using a [100]-oriented Si wafer is illustrated in Figure 16.9. It can be seen in this figure that there are {100} planes perpendicular to the wafer surface and that their intersections with the wafer surface are <100> directions. These <100> directions enclose a 45° angle with the wafer flat (i.e., the <110> directions). By aligning the mask opening with these <100> orientations, {100} facets are initially introduced as sidewalls. The {110} planes etch faster than the {100} planes and are not introduced. As the bottom and sidewall planes are all from the same {100} group, lateral underetch equals the vertical etch rate and rectangular channels, bounded by slower etching {100} planes, result (Figure 16.10). Since the top of the etched channels is exposed to the etchant longer than the bottom, one might have expected the channels in Figure 16.10 to be wider at the top than at the bottom. With some minor corrections in Peeters' derivation [Peeters, 1994], we can use his explanation for why the sidewalls stay vertical. Assume the width of the mask opening to be W_m. At a given depth, z, into the wafer, the underlying Si is no longer masked by W_m, but rather by the intersection of the previously formed {100} facets with the bottom surface. The width of this new mask is larger than the lithography mask W_m by the amount the latter is being undercut. Let's call the new mask width W_2 the effective mask width at a depth z. The relation

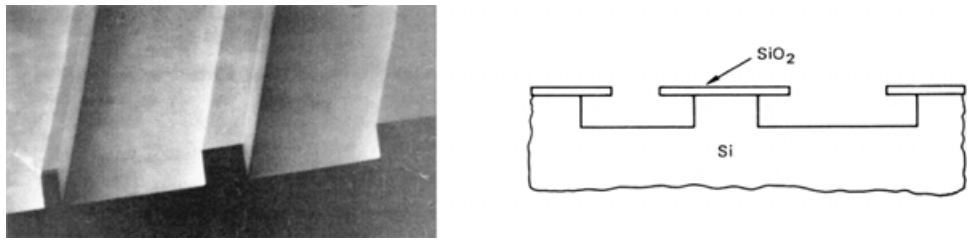


FIGURE 16.10 Vertical sidewalls in a (100) wafer.

between W_m and W_z is given by the lateral etch rate of a {100} facet and the time that facet was exposed to the etchant at depth z, i.e.:

$$W_z = W_m + 2R_{xy}\Delta t_z \tag{16.3}$$

where R_{xy} is the lateral underetch rate (i.e., etch rate in the x-y plane) and Δt_z the etch time at depth z. The underetching, U_z, of the effective mask opening W_z is given by:

$$U_z = TR_{xy} - R_{xy}\Delta t_z \tag{16.4}$$

where T is the total etch time so far. The width of the etched pit, W_{tot}, at depth z is further given by the sum of W_m and twice the underetching for that depth:

$$W_{\text{tot}} = W_z + 2U_z = W_m + 2TR_{xy} \tag{16.5}$$

Or, since T can also be written as the measured total etch depth z divided by the vertical etch rate R_z, Eq. (16.5) can be rewritten as

$$\begin{aligned} W_{\text{tot}} &= W_m + 2z(R_{xy}/R_z) \quad \text{or since } R_{xy} = R_z, \\ W_{\text{tot}} &= W_m + 2z \end{aligned} \tag{16.6}$$

The width of the etched recess is therefore equal to the photolithographic mask width plus twice the etch depth—independent of that etch depth, in other words; the walls remain vertical independent of the depth z.

For sufficiently long etch times, {111} facets take over eventually from the vertical {100} facets. These inward sloping {111} facets are first introduced at the corners of a rectangular mask and grow larger at the expense of the vertical sidewalls until the latter ultimately disappear altogether. Alignment of mask features with the <100> directions in order to obtain vertical sidewalls in {100} wafers, therefore, is not very useful for the fabrication of diaphragms. However, it can be very effective for anticipating the undercutting of convex corners on {100} wafers. This useful aspect will be revisited when discussing corner compensation.

16.3.3.2 [110]-Oriented Silicon

In Figure 16.11, we show a unit cell of Si properly aligned with the surface of a (110) Si wafer. This drawing will enable us to predict the shape of an anisotropically etched recess on the basis of elementary geometric crystallography. Whereas the intersections of the {111} planes with the (100) wafer surface are mutually perpendicular, here they enclose an angle γ in the (110) plane. Moreover, the intersections are not parallel (<110>) or perpendicular (<100>) to the main wafer flat (assumed to be <110> in this case), but rather enclose angles δ or $\delta + \gamma$. It follows that a mask opening that will not be undercut (i.e., oriented such that resulting feature sidewalls are exclusively made up by {111} planes) cannot be a rectangle aligned with the flat, but must be a parallelogram skewed by $\gamma - 90°$ and δ degrees off-axis. The angles γ and δ are calculated as follows [Peeters, 1994] (see Figures 16.11 and 16.12):

$$\tan\beta = \frac{\frac{1}{2}a\frac{\sqrt{2}}{2}}{\frac{a}{2}} = \frac{\sqrt{2}}{2} \tag{16.7}$$

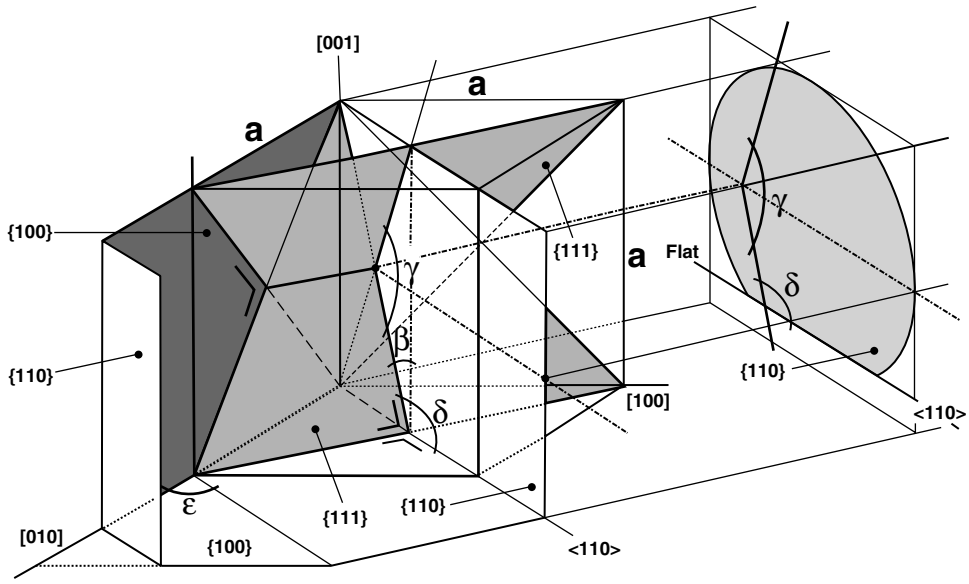


FIGURE 16.11 (110) silicon wafer with reference to the unity cube and its relevant planes. The wafer flat is in a <110> direction. (From Peeters, E., *Process Development for 3D Silicon Microstructures with Application to Mechanical Sensor Design,* KUL, Belgium, 1994. With permission.)

$$\begin{aligned}\gamma &= 180^\circ - 2\beta = 180^\circ - 2\arctan\left(\frac{\sqrt{2}}{2}\right) = 109.47^\circ \\ \delta &= 90^\circ + \beta = 90^\circ + \arctan\left(\frac{\sqrt{2}}{2}\right) = 125.26^\circ \\ \varphi &= 270^\circ - \delta = 144.74^\circ\end{aligned} \tag{16.8}$$

From Figure 16.11, it can also be seen that the {111} planes are oriented perpendicular to the (110) wafer surface. This makes it possible to etch pits with vertical sidewalls (Figure 16.12). The bottom of the pit shown here is bounded by {110} and/or {100} planes, depending on the etch time. At short etch times, one mainly sees a flat {110} bottom. As the {110} planes are etching slightly faster than the {100} planes, the flat {110} bottom is getting smaller and smaller and a V-shaped bottom bounded by {100} planes eventually results. The angle ε as shown in Figure 16.12 equals 45°, being the angle enclosed by the intersections of a {100} and a {110} bottom plane. The general rule does apply that an arbitrary window opening is circumscribed by a parallelogram with the given orientation and skewness for sufficiently long etch times. Another difference between (100)- and (110)-oriented Si wafers is that on the (110) wafers it is possible to etch under microbridges crossing at a 90° angle a shallow V-groove (formed by (111) planes). In order to undercut a bridge on a (100) plane, the bridge cannot be perpendicular to the V-groove; it must be oriented slightly off normal [Elwenspoek et al., 1994].

16.3.3.3 Selection of [100]- or [110]-Oriented Silicon

In Table 16.1, we compare the main characteristics of etched features in [100]- and [110]-oriented wafers. This guide can help decide which orientation to use for a specific microfabrication application at hand.

From this table it is obvious that for membrane-based sensors, [100] wafers are preferred. The understanding of the geometric considerations with [110] wafers is important, though, if one wants to fully appreciate all the possible single crystal silicon (SCS) micromachined shapes, and it is especially helpful

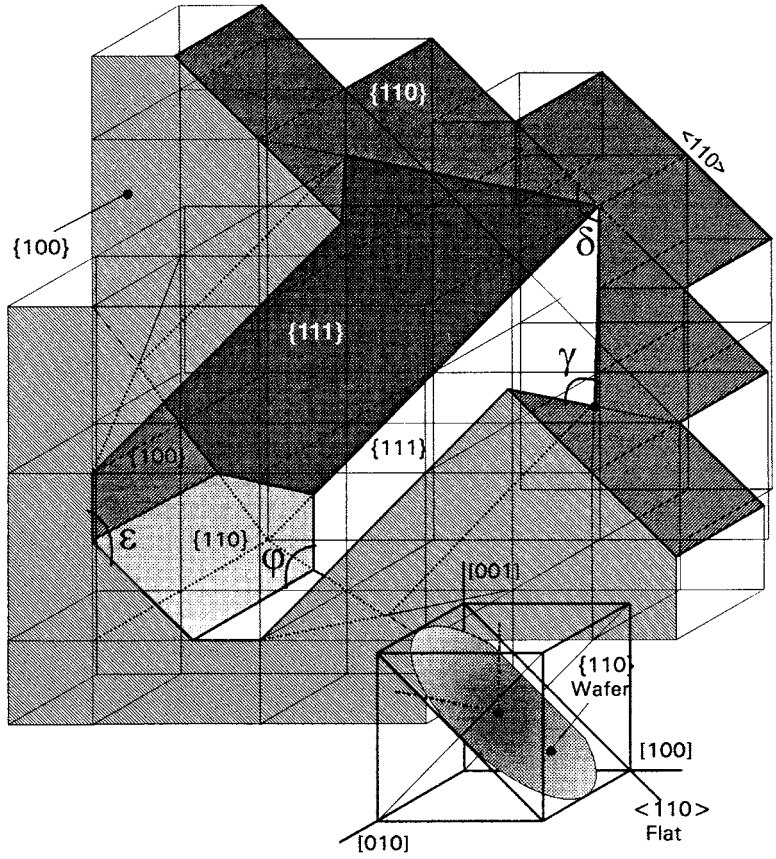


FIGURE 16.12 (110) silicon wafer with anisotropically etched recess inscribed in the Si lattice. $\gamma = 109.47°$; $\delta = 125.26°$; $\varphi = 144.74°$; and $\varepsilon = 45°$. (From Peeters, E., *Process Development for 3D Silicon Microstructures with Application to Mechanical Sensor Design,* KUL, Belgium, 1994. With permission.)

to understand corner compensation schemes (see below). Moreover, all processes for providing dielectric isolation require that the silicon be separated into discrete regions. To achieve a high component density with anisotropic etches on (100) wafers, the silicon must be made very thin because of the aspect ratio limitations due to the sloping walls (see above). With vertical sidewall etching in a (100) wafer, the etch mask is undercut in all directions to a distance approximately equal to the depth of the etching. Vertical etching in (110) surfaces relaxes the etching requirement dramatically and enables more densely packed

TABLE 16.1 Selection of Wafer Type

[100] Orientation	[110] Orientation
Inward sloping walls (54.74°)	Vertical {111} walls
The sloping walls cause a lot of lost real estate	Narrow trenches with high aspect ratio are possible
Flat bottom parallel to surface is ideal for membrane fabrication	Multifaceted cavity bottom ({110} and {100} planes) makes for a poor diaphragm
Bridges perpendicular to a V-groove bound by (111) planes cannot be underetched	Bridges perpendicular to a V-groove bound by (111) planes can be undercut
Shape and orientation of diaphragms convenient and simple to design	Shape and orientation of diaphragms awkward and more difficult to design
Diaphragm size, bounded by nonetching {111} planes, is relatively easy to control	Diaphragm size is difficult to control; the <100> edges are not defined by nonetching planes

structures such as beam leads or image sensors. Kendall describes and predicts a wide variety of applications for (110) wafers such as fabrication of trench capacitors, vertical multi-junction solar cells, diffraction gratings, infrared interference filters, large area cathodes and filters for bacteria [Kendall, 1975; 1979].

16.4 Silicon as a Substrate and Structural Material

16.4.1 Silicon as Substrate

For many mechanical sensor applications, single crystal Si, based on its intrinsic mechanical stability and the feasibility of integrating sensing and electronics on the same substrate, often presents an excellent substrate choice. For chemical sensors, on the other hand, Si, with few exceptions,[2] is merely the substrate and the choice is not always that straightforward.

In Table 16.2, we show a performance comparison of substrate materials in terms of cost, metallization ease and machinability. Both ceramic and glass substrates are difficult to machine, and plastic substrates are not readily amenable to metallization. Silicon has the highest material cost per unit area, but this cost often can be offset by the small feature sizes possible in a silicon implementation. Si with or without passivating layers, due to its extreme flatness, relative low cost and well-established coating procedures, often is the preferred substrate especially for thin films. A lot of thin-film deposition equipment is built to accommodate Si wafers and, as other substrates are harder to accommodate, this lends Si a convenience advantage. There is also a greater flexibility in design and manufacturing with silicon technology compared to other substrates. In addition, although much more expensive, the initial capital equipment investment is not product specific. Once a first product is on line, a next generation or new products will require changes in masks and process steps but not in the equipment itself.

Disadvantages of using Si usually are most pronounced with increasing device size and low production volumes and when electronics do not need or cannot be incorporated on the same Si substrate. The latter could be either for cost reasons (e.g., in the case of disposables such as glucose sensors) or for technological reasons (e.g., the devices will be immersed in conductive liquids or they must operate at temperatures above 150°C).

An overwhelming determining factor for substrate choice is the final package of the device. A chemical sensor on an insulating substrate almost always is easier to package than a piece of Si with conductive edges in need of insulation.

Sensor packaging is so important in sensors that as a rule sensor design should start from the package rather than from the sensor. In this context, an easier to package substrate has a huge advantage. The latter is the most important reason why recent chemical sensor development in industry has retrenched from a move toward integration on silicon in the 1970s and early 1980s to a hybrid thick film on ceramic approach in the late 1980s and early 1990s. In academic circles in the U.S. chemical sensor integration with electronics continued until the late 1980s; in Europe and Japan, such efforts are still going on [Madou, 1994].

TABLE 16.2 Performance Comparison of Substrate Materials

Substrate	Cost	Metallization	Machinability
Ceramic	Medium	Fair	Poor
Plastic	Low	Poor	Fair
Silicon	High	Good	Very good
Glass	Low	Good	Poor

[2] A notable exception is the ion-sensitive field effect transistor (ISFET) where the Si space charge is modulated by the presence of chemicals for which the ISFET chemical coating is sensitive [Madou, 1997, chap. 10].

16.4.2 Silicon as a Structural Element in Mechanical Sensors

16.4.2.1 Introduction

In mechanical sensors the active structural elements convert a mechanical external input signal (force, pressure, acceleration etc.) into an electrical signal output (voltage, current or frequency). The transfer functions in mechanical devices describing this conversion are mechanical, electro-mechanical and electrical.

In the mechanical conversion, a given external load is concentrated and maximized in the active member of the sensor. Structurally active members are typically high-aspect-ratio elements such as suspended beams or membranes. The electromechanical conversion is the transformation of the mechanical quantity into an electrical quantity such as capacitance, resistance, charge etc. Often the electrical signal needs further electrical conversion into an output voltage, frequency or current. For electrical conversion into an output voltage, a Wheatstone bridge may be used as in the case of a piezoresistive sensor, and a charge amplifier may be used in the case of a piezoelectric sensor. To optimize all three transfer functions, detailed electrical and mechanical modeling is required. One of the most important inputs required for the mechanical models are the experimentally determined independent elasticity constants or moduli. In what follows, we describe what makes Si such an important structural element in mechanical sensors and present its elasticity constants.

16.4.2.2 Important Characteristics of Mechanical Structural Elements: Stress-Strain Curve and Elasticity Constants

Yield, tensile strength, hardness and creep of a material all relate to the elasticity curve, i.e., the stress–strain diagram of the material as shown in Figure 16.13. For small strain values, Hooke's law applies, i.e., stress (force per unit area, N/m^2) and strain (displacement per unit length, dimensionless) are proportional and the stress–strain curve is linear, with a slope corresponding to the elastic modulus E (Young's modulus-N/m^2). This regime as in Figure 16.13 is marked as the elastic deformation regime. For isotropic media such as amorphous and polycrystalline materials, the applied axial force per unit area or tensile stress, σ_a, and the axial or tensile strain, ε_a, are thus related as:

$$\sigma_a = E\varepsilon_a \tag{16.9}$$

with ε_a given by the dimensionless ratio of $L_2 - L_1/L_1$, i.e., the ratio of the wire's elongation to its original length. The elastic modulus may be thought of as stiffness or a material's resistance to elastic deformation.

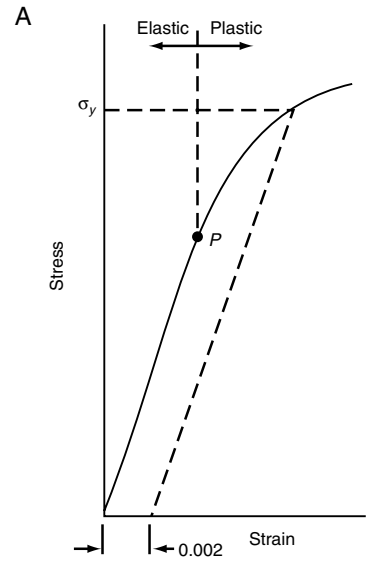


FIGURE 16.13 Typical stress-strain behavior for a material showing elastic and plastic deformations, the proportional limit P and the yield strength σ_y, as determined using the 0.002 strain offset method (see text).

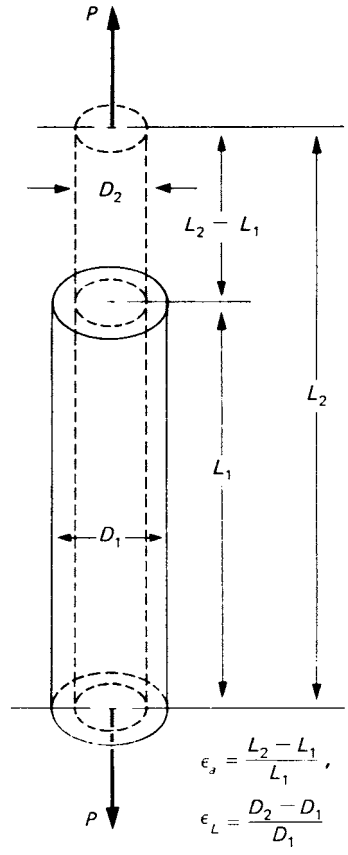


FIGURE 16.14 Metal wire under axial or normal stress; normal stress creates both elongation and lateral contraction.

The greater the modulus, the stiffer the material. A tensile stress usually also leads to a lateral strain or contraction (Poisson effect), ε_1, given by the dimensionless ratio of $D_2 - D_1/D_1$ ($\Delta D/D_1$), where D_1 is the original wire diameter and ΔD is the change in diameter under axial stress (see Figure 16.14). The Poisson ratio is the ratio of lateral over axial strain:

$$\nu = -\frac{\varepsilon_1}{\varepsilon_a} \tag{16.10}$$

The minus sign indicates a contraction of the material. For most materials, ν is a constant within the elastic range. Normally, some slight volume change does accompany the deformation, and, consequently, ν is smaller than 0.5. The magnitude of the Young's modulus ranges from 4.1×10^4 MPa (the N/m^2 unit is called the Pascal, Pa) for magnesium, to 40.7×10^4 MPa for tungsten and 144 GPa for Invar. With increasing temperature, the elastic modulus diminishes. The Poisson ratios for aluminum and cast steel are 0.34 and 0.28, respectively. The value of ν fluctuates for different materials over a relatively narrow range. Generally, it is on the order of 0.25 to 0.35. In extreme cases, values as low as 0.1 (certain types of concrete) and as high as 0.5 (rubber) occur. A value of 0.5 is the largest value possible. It is attained by materials during plastic flow and indicates a constant volume. For an elastic isotropic medium subjected to a triaxial state of stress, the resulting strain component in the x direction, ε_x, is given by the summation of elongation and contraction:

$$\varepsilon_x = \frac{1}{E}[\sigma_x - \nu(\sigma_y + \sigma_z)] \tag{16.11}$$

and so on for the y and z directions (three equations in total).

For an analysis of mechanical structures we must consider not only compressional and tensile strains but also shear strains. Whereas normal stresses create elongation plus lateral contraction with accompanying volume changes, shear stresses (e.g., by twisting a body) create shape changes without volume changes, i.e., shear strains. The one-dimensional shear strain, γ, is produced by the shear stress, τ (N/m^2). For small strains, Hooke's law may be applied again:

$$\gamma = \frac{\tau}{G} \tag{16.12}$$

where G is called the elastic shear modulus or the modulus of rigidity. For any three-dimensional state of shear stress, three equations of this type will hold. Isotropic bodies are characterized by two independent elastic constants only, since the shear modulus G, as can be shown [Chou and Pagano, 1967], relates the Young's modulus and the Poisson ratio as:

$$G = \frac{E}{2(1+\nu)} \tag{16.13}$$

Crystal materials, whose elastic properties are anisotropic, require more than two elastic constants, the number increasing with decreasing symmetry. Cubic crystals (bcc, fcc), for example, require 3 elastic constants, hexagonal crystals require 5, and materials without symmetry require 21 [Kittel, 1976; Chou and Pagano, 1967]. The relation between stresses and strains is more complex in this case and depends greatly on the spatial orientation of these quantities with respect to the crystallographic axes. Hooke's law in the most generic form is expressed in two formulas:

$$\sigma_{ij} = E_{ijkl} \cdot \varepsilon_{kl} \quad \text{and} \quad \varepsilon_{ij} = S_{ijkl} \cdot \sigma_{kl} \tag{16.14}$$

where σ_{ij} and σ_{kl} are stress tensors of rank 2 expressed in N/m^2; ε_{ij} and ε_{kl} are strain tensors of rank 2 and are dimensionless; E_{ijkl} is a stiffness coefficient tensor of rank 4 expressed in N/m^2; and S_{ijkl} is a compliance coefficient tensor of rank 4 expressed in m^2/N. The first expression is analogous to Eq. (16.9) and the second expression is the inverse, giving the strains in terms of stresses. The tensor representations in Eq. (16.14) can also be represented as two matrices:

$$\sigma_m = \sum_{n=1}^{6} E_{mn}\varepsilon_n \quad \text{and} \quad \varepsilon_m = \sum_{n=1}^{6} S_{mn}\sigma_n \tag{16.15}$$

Components of tensors E_{ijkl} and S_{ijkl} are substituted by elements of the matrices E_{mn} and S_{mn}, respectively. To convert the ij indices to m and the kl indices to n, the following scheme applies:

$11 \rightarrow 1$, $22 \rightarrow 2$, $33 \rightarrow 3$, 23 and $32 \rightarrow 4$, 13 and $31 \rightarrow 5$, 12 and $21 \rightarrow 6$, $E_{ijkl} \rightarrow E_{mn}$ and $S_{ijkl} \rightarrow S_{mn}$ when m and n = 1,2,3; 2 $S_{ijkl} \rightarrow S_{mn}$ when m or n = 4,5,6; $4S_{ijkl} \rightarrow S_{mn}$ when m and n = 4,5,6; $\sigma_{ij} \rightarrow \sigma_m$ when m = 1,2,3; and $\varepsilon_{ij} \rightarrow \varepsilon_m$ when m = 4,5,6

With these reduced indices there are thus six equations of the type:

$$\sigma_x = E_{11}\varepsilon_x + E_{12}\varepsilon_y + E_{13}\varepsilon_z + E_{14}\gamma_{yz} + E_{15}\gamma_{zx} + E_{16}\gamma_{xy} \tag{16.16}$$

and hence 36 moduli of elasticity or E_{mn} stiffness constants. There are also six equations of the type:

$$\varepsilon_x = S_{11}\sigma_x + S_{12}\sigma_y + S_{13}\sigma_z + S_{14}\tau_{yz} + S_{15}\tau_{zx} + S_{16}\tau_{xy} \tag{16.17}$$

defining 36 S_{mn} constants which are called the compliance constants; see also Madou (1997, Eq. (9.29)). It can be shown that the matrices E_{mn} and S_{mn}, each composed of 36 coefficients, are symmetrical; hence, a material without symmetry elements has 21 independent constants or moduli. Due to symmetry of crystals, several more of these may vanish until, for our isotropic medium, they number two only (E and ν). The stiffness coefficient and compliance coefficient matrices for cubic-lattice crystals with the vector of stress oriented along the [100] axis are given as:

$$E_{mn} = \begin{bmatrix} E_{11} & E_{12} & E_{12} & 0 & 0 & 0 \\ E_{12} & E_{11} & E_{12} & 0 & 0 & 0 \\ E_{12} & E_{12} & E_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & E_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & E_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & E_{44} \end{bmatrix} \quad S_{mn} = \begin{bmatrix} S_{11} & S_{12} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{11} & S_{12} & 0 & 0 & 0 \\ S_{12} & S_{12} & S_{11} & 0 & 0 & 0 \\ 0 & 0 & 0 & S_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & S_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & S_{44} \end{bmatrix} \tag{16.18}$$

In cubic crystals, the three remaining independent elastic moduli are usually chosen as E_{11}, E_{12} and E_{44}. The S_{mn} values can be calculated simply from these E_{mn} values. Expressed in terms of the compliance constants, one can show that $1/S_{11} = E$ = Young's modulus, $-S_{12}/S_{11} = \nu$ = Poisson's ratio, and $1/S_{44} = G$ = shear modulus. In the case of an isotropic material, such as a metal wire, there is an additional relationship:

$$E_{44} = \frac{E_{11} - E_{12}}{2} \tag{16.19}$$

reducing the number of independent stiffnesses constants to two. The anisotropy coefficient α is defined as:

$$\alpha = \frac{2E_{44}}{E_{11} - E_{12}} \tag{16.20}$$

making $\alpha = 1$ for an isotropic crystal. For an anisotropic crystal, the degree of anisotropy is given by the deviation of α from 1. Single crystal silicon has moderately anisotropic elastic properties [Brantley, 1973; Nikanorov et al., 1972], with $\alpha = 1.57$. Brantley (1973) gives the non-zero stiffness components, referred to the [100] crystal orientation as: $E_{11} = E_{22} = E_{33} = 166 \times 10^9$ N/m^2, $E_{12} = E_{13} = E_{23} = 64 \times 10^9$ N/m^2 and $E_{44} = E_{55} = E_{66} = 80 \times 10^9$ N/m^2:

$$\begin{vmatrix} \sigma_x \\ \sigma_y \\ \sigma_z \\ \tau_{xy} \\ \tau_{xz} \\ \tau_{yz} \end{vmatrix} = \begin{vmatrix} 166(E_{11}) & 64(E_{12}) & 64(E_{12}) & 0 & 0 & 0 \\ 64(E_{12}) & 166(E_{11}) & 64(E_{12}) & 0 & 0 & 0 \\ 64(E_{12}) & 64(E_{12}) & 166(E_{11}) & 0 & 0 & 0 \\ 0 & 0 & 0 & 80(E_{44}) & 0 & 0 \\ 0 & 0 & 0 & 0 & 80(E_{44}) & 0 \\ 0 & 0 & 0 & 0 & 0 & 80(E_{44}) \end{vmatrix} \times \begin{vmatrix} \varepsilon_x \\ \varepsilon_y \\ \varepsilon_z \\ \gamma_{xy} \\ \gamma_{xz} \\ \gamma_{yz} \end{vmatrix} \tag{16.21}$$

with σ normal stress, τ shear stress, ε normal strain and γ shear strain. The values for E_{mn}, in Eq. (16.21), compare with a Young's modulus of 207 GPa for a low carbon steel. Variations on the values of the elastic constants on the order of 30%, depending on crystal orientation, must be considered; doping level (see below) and dislocation density have minor effects as well. From the stiffness coefficients the compliance coefficients of Si can be calculated as $S_{11} = 7.68 \times 10^{-12}$ m^2/N, $S_{12} = -2.14 \times 10^{-12}$ m^2/N, and $S_{44} = 12.6 \times 10^{-12}$ m^2/N [Khazan, 1994]. A graphical representation of elastic constants

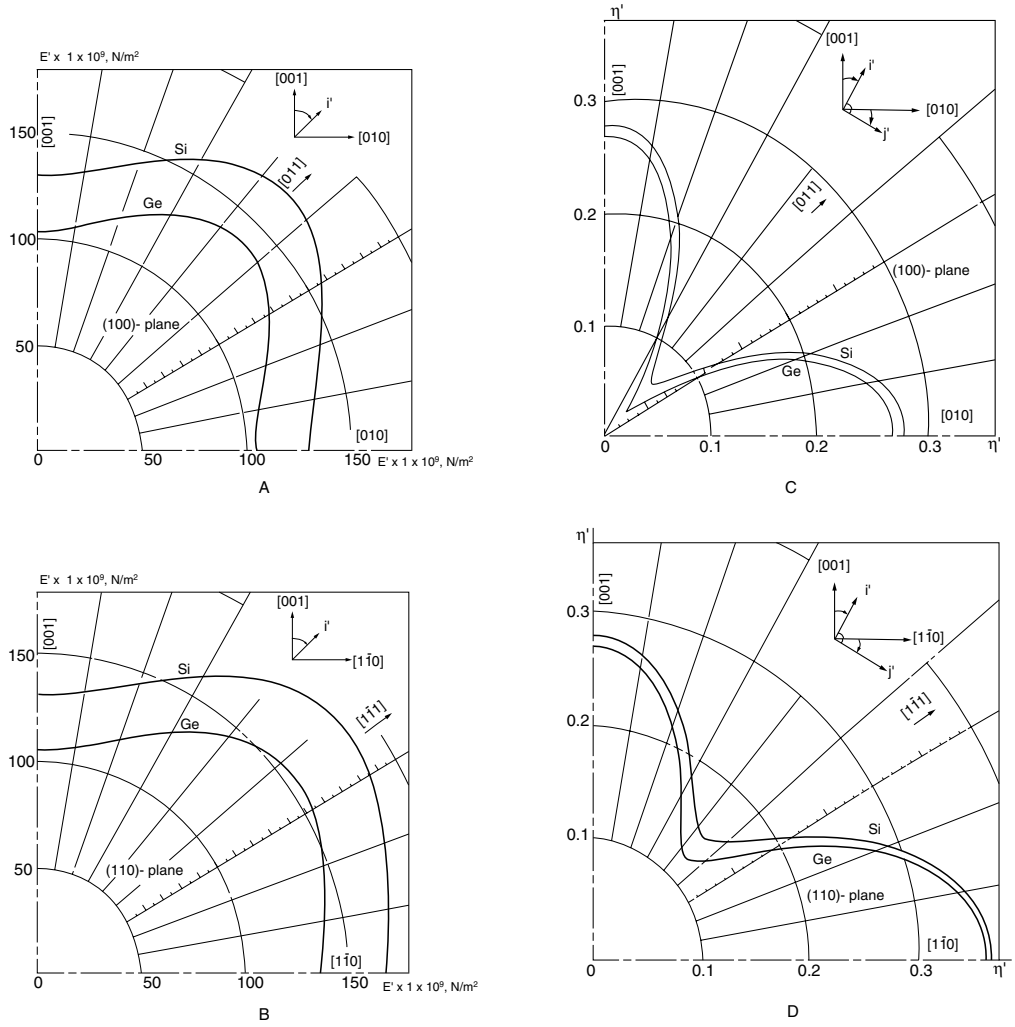


FIGURE 16.15 Elasticity constants for Si and Ge. (A) Young's modulus as a function of direction in the (100) plane. (B) Young's modulus as a function of direction in the (110) plane. (C) Poisson ratio as a function of direction in the (100) plane. (D) Poisson's ratio as a function of direction in the (110) plane. (From Worthman, J. J. and R. A. Evans, *J. Appl. Phys.*, 36, 153–156, 1965. With permission.)

for different crystallographic directions in Si and Ge is given in Worthman and Evans (1965) and is reproduced in Figure 16.15. Figure 16.15A to D displays E and ν for Ge and Si in planes (100) and (110) as functions of direction. Calculations show that E, G and ν are constant for any direction in the (111) plane. In other words, a plate lying in this plane can be considered as having isotropic elastic properties. A review of independent determinations of the Si stiffness coefficients, with their respective temperature coefficients, is given in Metzger and Kessler (1970). Some of the values from that review are reproduced in Table 16.3. Values for Young's modulus and the shear modulus of Si can also be found in Greenwood (1988) and are reproduced in Table 16.4 for the three technically important crystal orientations.

16.4.2.3 Residual Stress

Most properties, such as the Young's modulus, for lightly and highly doped silicon are identical. From Section 16.10 on, we will see that the Young's modulus for polycrystalline silicon is about 161 GPa.

TABLE 16.3 Stiffness Coefficients and Temperature Coefficient of Stiffness for Si [Metzger and Kessler, 1970]

Stiffness Coefficients (GPa = 10^9 N/m^2)	Temperature Coefficient of Stiffness (δE/δT/E)
E_{11} = 164.8 ± 0.16	-122×10^{-6}
E_{12} = 63.5 ± 0.3	-162×10^{-6}
E_{44} = 79.0 ± 0.06	-97×10^{-6}

TABLE 16.4 Derived Values for Young's Modulus and Shear Modulus for Si [Greenwood, 1988]

Miller Index for Orientation	Young's Modulus (E) (GPa)	Shear Modulus (G) (GPa)
[100]	129.5	79.0
[110]	168.0	61.7
[111]	186.5	57.5

Residual stress and associated stress gradients in highly boron doped single crystal silicon present some controversy. Highly boron-doped membranes, which are usually reported to be tensile, also have been reported compressive [Huff and Schmidt, 1992; Maseeh and Senturia, 1990]. From a simple atom-radius argument, one expects that a large number of substitutional boron atoms would create a net shrinkage of the lattice compared to pure silicon and that the residual stress would be tensile with a stress gradient corresponding to the doping gradient. That is, an etched cantilever would be expected to bend up out of the plane of the silicon wafer. Maseeh and Santuria (1990) believe that the appearance of compressive behavior in heavily boron-doped single crystal layers results from the use of an oxide etch mask. They suggest that plastic deformation of the p^+ silicon beneath the compressively stressed oxide can explain the observed behavior. Ding and Ko (1991), who also found compressive behavior for nitride-covered p^+ Si thin membranes, believe that the average stress in p^+ silicon is indeed tensile, but great care is required to establish this fact because the combination of heavy boron doping and a high-temperature drive-in under oxidizing conditions can create an apparent reversal of both the net stress (to compressive) and of the stress gradient (opposite to the doping gradient). A proposed explanation is that at the oxide-silicon interface, a thin compressively stressed layer is formed during the drive-in which is not removed in buffered HF. It can be removed by reoxidation and etching in HF, or by etching in KOH.

16.4.2.4 Yield, Tensile Strength, Hardness and Creep

As a material is deformed beyond its elasticity limit, yielding or plastic deformation—permanent, non-recoverable deformation—occurs. The point of yielding in Figure 16.13 is the point of initial departure from linearity of the stress–strain curve and is sometimes called the proportional limit indicated by a letter "P." The Young's modulus of mild steel is ±30,000,000 psi,[3] and its proportional limit (highest stress in the elastic range) is approximately 30,000 psi. Thus, the maximum elastic strain in mild steel is about 0.001 under a condition of uniaxial stress. This gives an idea as to the magnitude of the strains we are dealing with. A convention has been established wherein a straight line is constructed parallel to the elastic portion of the stress–strain curve at some specified strain offset, usually 0.002. The stress corresponding to the intersection of this line and the stress–strain curve as it bends over in the plastic region is defined as the yield strength, σ_y (see Figure 16.13). The magnitude of the yield strength of a material

[3] In the sensor area it is still mandatory to be versatile in the different unit systems especially with regards to expressing units for quantities such as pressure and stress. In this book we are using mostly Pascal, Pa (=N/m^2), but in industry it is still customary to use psi when dealing with metal properties, torr when dealing with vacuum systems, and dyne/cm^2 when dealing with surface tension.

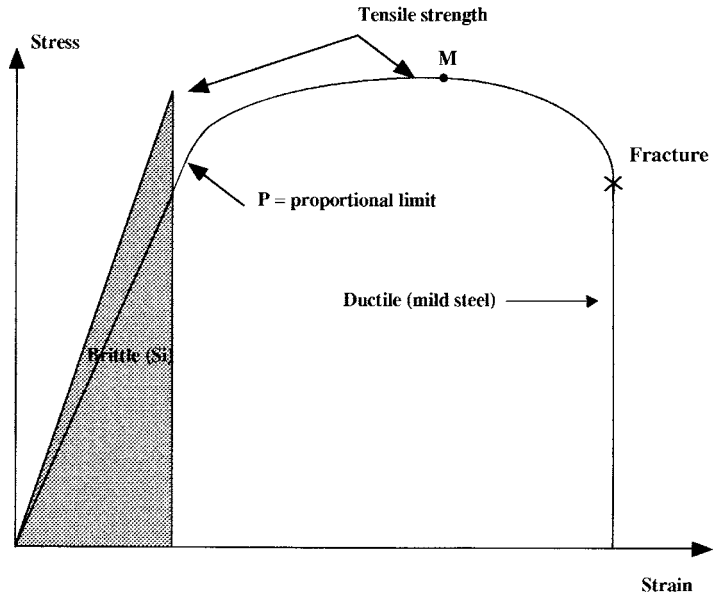


FIGURE 16.16 Stress–strain curve. Tensile strength of a metal is the stress at the maximum of this curve. Abrupt brittle fracture of a high modulus material with no plastic deformation region like Si is indicated as well.

is a measure of its resistance to plastic deformation. Yield strengths may range from 35 MPa (5000 psi) for a soft and weak aluminum to over 1400 MPa (200,000 psi) for high strength steels. The tensile strength is the stress at the maximum of the stress–strain curve (Figure 16.16). This corresponds to the maximum stress that can be sustained by a structure in tension; if the stress is applied and maintained, fracture will result. Both tensile strength and hardness are indicators of a metal's resistance to plastic deformation. Consequently, they are roughly proportional [Callister, 1985]. Material deformation occurring at elevated temperatures and static material stresses is termed creep. It is defined as a time-dependent and permanent deformation of materials when subjected to a constant load or stress.

Silicon exhibits no plastic deformation or creep below 800°C; therefore, Si sensors are inherently very insensitive to fatigue failure when subjected to high cyclic loads. Silicon sensors have actually been cycled in excess of 100 million cycles with no observed failures. This ability to survive a very large number of duty cycles is due to the fact that there is no energy absorbing or heat generating mechanism due to intergranular slip or movement of dislocations in silicon at room temperature. However, single crystal Si, as a brittle material, will yield catastrophically, when stress beyond the yield limit is applied, rather than deform plastically as metals do (see Figure 16.16). At room temperature, high modulus materials such as Si, SiO_2 and Si_3N_4 often exhibit linear-elastic behavior at lower strain and transition abruptly to brittle-fracture behavior at higher strain. Plastic deformation in metals is based on stress-induced dislocation generation in the grain boundaries and a subsequent dislocation migration that results in a macroscopic deformation from inter-grain shifts in the material. No grain boundaries exist in single crystal silicon (SCS), and plastic deformation can only occur through migration of the defects originally present in the lattice or of those that are generated at the surface. As the number of these defects is very low in SCS, the material can be considered a perfect elastic material at normal temperatures. Perfect elasticity implies proportionality between stress and strain (i.e., load and flexure) and the absence of irreversibilities or mechanical hysteresis. The absence of plastic behavior also accounts for the extremely low mechanical losses in SCS, which enable the fabrication of resonating structures that exhibit exceptionally high Q-factors. Values of up to 10^8 in vacuum have been reported. At elevated temperatures, and with metals and polymers at ordinary temperatures, complex behavior in the stress–strain curve can occur. Considerable plasticity can be induced in SCS at elevated temperatures (>800°C), when the mobility of defects in the

lattice is substantially increased. Huff and Schmidt (1992) actually report a pressure switch exhibiting hysteresis based on buckling of plastically deformed silicon membranes. To eliminate plastic deformation of Si wafers, it is important that during high temperature steps the presence of films that could stress or even warp the wafer in an asymmetric way, typically oxides or nitrides, be avoided.

16.4.2.5 Piezoresistivity in Silicon

Piezoresistance is the fractional change in bulk resistivity induced by small mechanical stresses applied to a material. Most materials exhibit piezoresistivity, but the effect is particularly important in some semiconductors (more than an order of magnitude higher than that of metals). Monocrystalline silicon has a high piezoresistivity and, combined with its excellent mechanical and electronic properties, makes a superb material for the conversion of mechanical deformation into an electrical signal. Actually, the history of silicon-based sensors started with the discovery of the piezoresistance effect in Si and Ge more than four decades ago [Smith, 1954]. The two main classes of piezoresistive sensors are membrane-type structures (typically pressure and flow sensors) and cantilever beams (typically acceleration sensors) with in-diffused resistors (boron, arsenic or phosphorus) strategically placed in zones of maximum stress.

For a three-dimensional anisotropic crystal, the electrical field vector (E) is related to the current vector (i) by a 3-by-3 resistivity tensor [Khazan, 1994]. Experimentally the nine coefficients are always found to reduce to six, and the symmetric tensor is given by:

$$\begin{bmatrix} E_1 \\ E_2 \\ E_3 \end{bmatrix} = \begin{bmatrix} \rho_1 & \rho_6 & \rho_5 \\ \rho_6 & \rho_2 & \rho_4 \\ \rho_5 & \rho_4 & \rho_3 \end{bmatrix} \cdot \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} \tag{16.22}$$

For the cubic Si lattice, with the axes aligned with the <100> axes, ρ_1, ρ_2 and ρ_3 define the dependence of the electric field on the current along the same direction (one of the <100> directions); ρ_4, ρ_5 and ρ_6 are cross-resistivities, relating the electric field to the current along a perpendicular direction.

The six resistivity components in Eq. (16.22) depend on the normal (σ) and shear (τ) stresses in the material as defined in the preceding section. Smith (1954) was the first to measure the resistivity coefficients π_{11}, π_{12} and π_{44} for Si at room temperature. Table 16.5 lists Smith's results [Smith, 1954]. The piezoresistance coefficients are largest for π_{11} in n-type silicon and π_{44} in p-type silicon, about -102.10^{-11} and 138.10^{-11} Pa^{-1}, respectively.

Resistance change can now be calculated as a function of the membrane or cantilever beam stress. The contribution to resistance changes from stresses that are longitudinal (σ_l) and transverse (σ_t) with respect to the current flow is given by:

$$\frac{\Delta R}{R} = \sigma_l \pi_l + \sigma_t \pi_t \tag{16.23}$$

where

σ_l = Longitudinal stress component, i.e., stress component parallel to the direction of the current.

σ_t = Transversal stress component, i.e., the stress component perpendicular to the direction of the current.

π_l = Longitudinal piezoresistance coefficient.

π_t = Transversal piezoresistance coefficient.

The piezoresistance coefficients π_l and π_t for (100) silicon as a function of crystal orientation are reproduced from Kanda in Figure 16.17A (for p-type) and B (for n-type) [Kanda, 1982]. By maximizing the expression for the stress-induced resistance change in Eq. (16.23), one optimizes the achievable sensitivity in a piezoresistive silicon sensor.

TABLE 16.5 Resistivity and Piezoresistance at Room Temperature [Smith, 1954; Khazan, 1994]

	ρ (Ω cm)	π_{11}[a]	π_{12}[a]	π_{44}[a]
p-Si	7.8	+6.6	–1.1	+138.1
n-Si	11.7	–102.2	+53.4	–13.6

[a] Expressed in 10^{-12} cm^2 $dyne^{-1}$ or 10^{-11} Pa^1.

The orientation of a membrane or beam is determined by its anisotropic fabrication. The surface of the silicon wafer is usually a (100) plane; the edges of the etched structures are intersections of (100) and (111) planes and are thus <110> directions. p-Type piezoresistors are most commonly used because the orientation of maximum piezoresistivity (<110>) happens to coincide with the edge orientation of a conventionally etched diaphragm and because the longitudinal coefficient is roughly equal in magnitude but opposite in sign as compared to the transverse coefficient (Figure 16.17A)[Peeters, 1994]. With the values in Table 16.5, π_l and π_t now can be calculated numerically for any orientation. The longitudinal piezoresistive coefficient in the <110> direction is $\pi_l = 1/2(\pi_{11} + \pi_{12} + \pi_{44})$. The corresponding transverse coefficient is $\pi_t = 1/2(\pi_{11} + \pi_{12} - \pi_{44})$. From Table 16.5 we know that, for p-type resistors, π_{44} is more important than the other two coefficients and Eq. (16.23) is approximated by:

$$\frac{\Delta R}{R} = \frac{\pi_{44}}{2}(\sigma_l - \sigma_t) \tag{16.24}$$

For n-type resistors, π_{44} can be neglected, and we obtain:

$$\frac{\Delta R}{R} = \frac{\pi_{11} + \pi_{12}}{2}(\sigma_1 + \sigma_t) \tag{16.25}$$

Equations (16.24) and (16.25) are valid only for uniform stress fields or if the resistor dimensions are small compared with the membrane or beam size. When stresses vary over the resistors they have to be integrated, which is most conveniently done by computer simulation programs.

To convert the piezoresistive effect into a measurable electrical signal, a Wheatstone bridge is often used. A balanced Wheatstone bridge configuration is constructed as in Figure 16.18A by locating four p-piezoresistors midway along the edges of a square diaphragm as in Figure 16.18B (location of maximum stress). Two resistors are oriented so that they sense stress in the direction of their current axes and two are placed to sense stress perpendicular to their current flow. Two longitudinally stressed resistors (A) are balanced against two transversally stressed resistors (B); two of them increase in value and the other two decrease in value upon application of a stress. In this case, from Eq. (16.24),

$$\frac{\Delta R}{R} \approx 70 \cdot 10^{-11}(\sigma_l - \sigma_t) \tag{16.26}$$

with σ in Pa. For a realistic stress pattern where σ_l = 10 MPa and σ_t = 50 MPa, Eq. (16.26) gives us a $\Delta R/R \approx 2.8\%$ [Peeters, 1994].

By varying the diameter and thickness of the silicon diaphragms, piezoresistive sensors in the range of 0 to 200 MPa have been made. The bridge voltages are usually between 5 and 10 volts, and the sensitivity may vary from 10 mV/kPa for low pressure to 0.001 mV/kPa for high pressure sensors.

Peeters (1994) shows how a more sensitive device could be based on n-type resistors when all the n-resistors oriented along the <100> direction are subjected to an uniaxial stress pattern in the longitudinal axis, as shown in Figure 16.19. The overall maximum piezoresistivity coefficient (π_l in the <100> direction) is substantially higher for n-silicon than it is for p-type silicon in any direction (maximum π_t and π_l in the

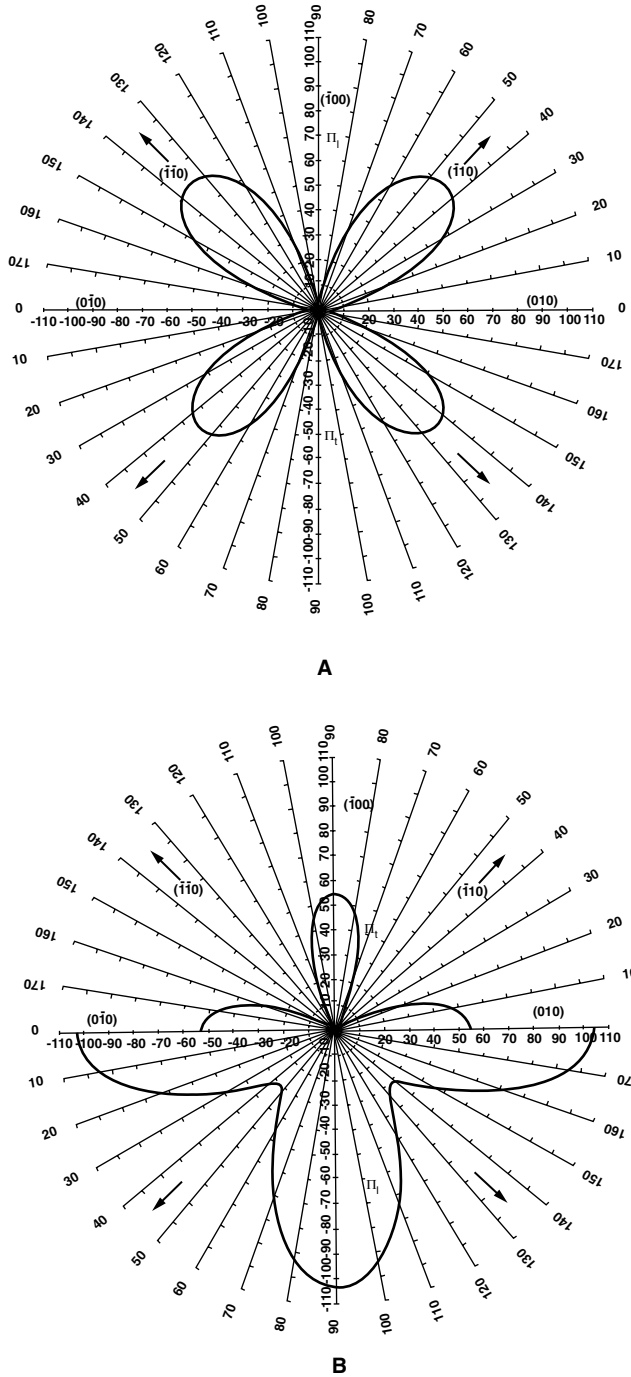


FIGURE 16.17 Piezoresistance coefficients π_1 and π_t for (100) silicon. (A) For p-type in the (001) plane (10^{-12} cm^2/dyne). (B) For n-type in the (001) plane (10^{-12} cm^{-2}/dyne). (From Kanda, Y., *IEEE Trans. Electr. Dev.*, ED-29, 64–70, 1982. With permission.)

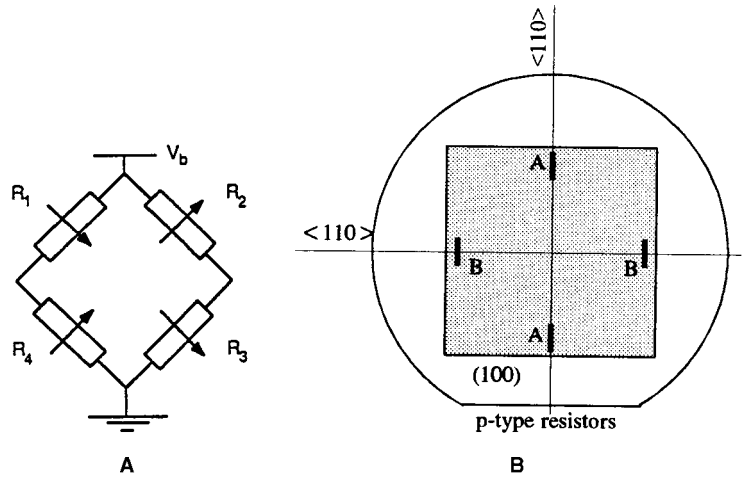


FIGURE 16.18 Measuring on a membrane with piezoresistors. (A) Wheatstone-bridge configuration of four in-diffused piezoresistors. The arrows indicate resistance changes when the membrane is bent downward. (B) Maximizing the piezoresistive effect with p-type resistors. The A resistors are stressed longitudinally and the B resistors are stressed transversally. (From Peeters, E., Ph.D. thesis, KUL, Belgium, 1994. With permission.)

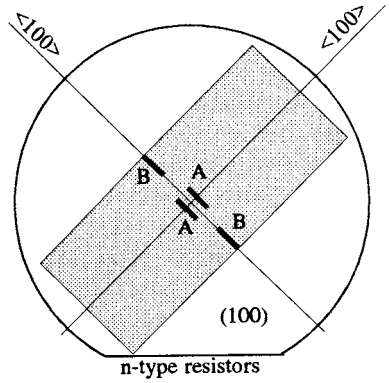


FIGURE 16.19 Higher pressure sensitivity by strategic placement of in-diffused piezoresistors proposed by Peeters (1994). The n-resistors are stressed longitudinally with the A resistors under tensile stress, and the B resistors under compressive stress. (From Peeters, E., Ph.D. thesis, KUL, Belgium, 1994. With permission.)

<100> direction, Figure 16.17B). Exploitation of these high piezoresistivity coefficients is less obvious, though, since the resistor orientation for maximum sensitivity (<100>) is rotated over 45° with respect to the <110> edges of an anisotropically etched diaphragm. Also evident from Figure 16.17B is that a transversally stressed resistor cannot be balanced against a longitudinally stressed resistor. Peeters has circumvented these two objections by a uniaxial, longitudinal stress pattern in the rectangular diaphragm represented in Figure 16.19. With a (100) substrate and a <100> orientation (45° to wafer flat) we obtain:

$$\frac{\Delta R}{R} \approx 53 \cdot 10^{-11} \cdot \sigma_t - 102 \cdot 10^{-11} \cdot \sigma_l \qquad (16.27)$$

with σ in Pa. Based on Eq. (16.27), with σ_t = 10 MPa and σ_l = 50 MPa, $\Delta R/R \approx -4.6\%$. In the proposed stress pattern it is important to minimize the transverse stress by making the device truly uniaxal as the

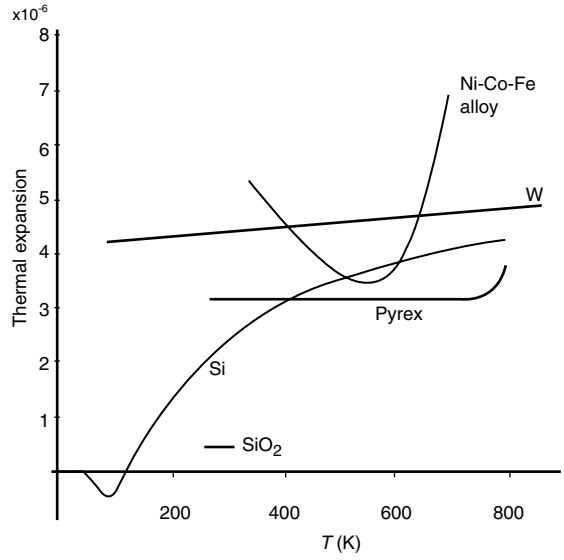


FIGURE 16.20 Thermal expansion coefficient vs. absolute temperature. (From Greenwood, J.C., *J. Phys. E: Sci. Instrum.*, 21 1114–1128, 1988. With permission.)

longitudinal and transverse stress components have opposite effects and can even cancel out. In practice, a pressure sensor with an estimated 65% gain in pressure sensitivity over the more traditional configurations could be made in the case of an 80% uniaxiality [Peeters, 1994].

The piezoresistive effect is often described in terms of the gauge factor, *G*, defined as:

$$G = \frac{1}{\varepsilon}\frac{\Delta R}{R} \tag{16.28}$$

which is the relative resistance change divided by the applied strain. The gauge factor of a metal strain gauge is typically around 2, for single crystal Si it is 90, and for poly-crystalline Si it is about 30 (see also Section 16.10).

16.4.2.6 Thermal Properties of Silicon

In Figure 16.20, the expansion coefficient of Si, W, SiO_2, Ni-Co-Fe alloy and Pyrex® is plotted vs. absolute temperature. Single crystal silicon has a high thermal conductivity (comparable with metals such as steel and aluminum) and a low thermal expansion coefficient. Its thermal expansion coefficient is closely matched to Pyrex glass but exhibits considerable temperature dependence. A good match in thermal expansion coefficient between the device wafer (e.g., Si) and the support substrate (e.g., Pyrex) is required. A poor match introduces stress, which degrades the device performance. This makes it difficult to fabricate composite structures of Pyrex and Si that are stress-free over a wide range of temperatures. Drift in silicon sensors often stems from packaging. In this respect, several types of stress-relief, subassemblies for stress-free mounting of the active silicon parts play a major role; using silicon as the support for silicon sensors is highly desirable. The latter aspect is addressed in Madou (1997, chap. 8).

Although the Si band-gap is relatively narrow, by employing silicon on insulator (SOI) wafers, high temperature sensors can be fashioned. For the latter application, relatively highly doped Si, which is relatively linear in its temperature coefficient of resistance and sensitivity over a wide range, typically is employed.

When fabricating thermally isolated structures on Si, the large thermal conductivity of Si poses a considerable problem as the major heat leak occurs through the Si material. For thermally isolated structures, machining in glass or quartz with their lower thermal conductivity represents an important alternative.

16.5 Wet Isotropic and Anisotropic Etching

16.5.1 Wet Isotropic and Anisotropic: Empirical Observations

16.5.1.1 Introduction

Wet etching of Si is used mainly for cleaning, shaping, polishing and characterizing structural and compositional features [Uhlir, 1956]. Wet chemical etching provides a higher degree of selectivity than dry etching techniques. Wet etching often is also faster; compare a few microns to several tens of microns per minute for isotropic etchants and about 1 μm/min for anisotropic etchants vs. 0.1 μm/min in typical dry etching. More recently though, with ECR dry etching, rates of up to 6 μm/min were achieved (see Madou [1997, chap. 2]). Modification of wet etchant and/or temperature can alter the selectivity to silicon dopant concentration and type and, especially when using alkaline etchants, to crystallographic orientation. Etching proceeds by reactant transport to the surface (1), surface reaction (2), and reaction product transport away from the surface (3). If (1) or (3) is rate determining, etching is diffusion limited and may be increased by stirring. If (2) is the rate-determining step, etching is reaction rate limited and depends strongly on temperature, etching material and solution composition. Diffusion-limited processes have lower activation energies (of the order of a few Kcal/mol) than reaction-rate controlled processes and therefore are relatively insensitive to temperature variations. In general, one prefers reaction rate limitation as it is easier to reproduce a temperature setting than a stirring rate. The etching apparatus needs to have both a good temperature controller and a reliable stirring facility [Kaminsky, 1985; Stoller et al., 1970].

Isotropic etchants, also polishing etchants, etch in all crystallographic directions at the same rate; they usually are acidic, such as $HF/HNO_3/CH_3COOH$ (HNA), and lead to rounded isotropic features in single crystalline Si. They are used at room temperature or slightly above (<50°C). Historically they were the first Si etchants introduced [Robbins and Schwartz, 1959; 1960; 1961; 1976; Uhlir, 1956; Hallas, 1971; Turner, 1958; Kern, 1978; Klein and D'Stefan, 1962]. Later it was discovered that some alkaline chemicals will etch anisotropically, i.e., they etch away crystalline silicon at different rates depending on the orientation of the exposed crystal plane. Typically the pH stays above 12, while more elevated temperatures are used for these slower type etchants (>50°C). The latter type of etchants surged in importance in the late 1960s for the fabrication of dielectrically isolated structures in silicon [Stoller and Wolff, 1966; Stoller, 1970; Forster and Singleton, 1966; Kenney, 1967; Lepselter, 1966; 1967; Waggener, 1970; Kragness, 1973; Waggener et al., 1967a; 1967b; Bean and Runyan, 1977; Rodgers et al., 1977; Rodgers et al., 1976; Ammar and Rodgers, 1980; Schnable and Schmidt, 1976]. Isotropic etchants typically show diffusion limitation, while anisotropic etchants are reaction rate limited.

Preferential or selective etching (also structural etchants) usually are isotropic etchants that show some anisotropy [Kern and Deckert, 1978]. These etchants are used to produce a difference in etch rate between different materials or between compositional or structural variations of the same material on the same crystal plane. These type of etches often are the fastest and simplest techniques to delineate electrical junctions and to evaluate the structural perfection of a single crystal in terms of slip, lineage and stacking faults. The artifacts introduced by the defects etch into small pits of characteristic shape. Most of the etchants used for this purpose are acids with some oxidizing additives [Yang, 1984; Chu and Gavaler, 1965; Archer, 1982; Schimmel and Elkind, 1973; Secco d'Aragona, 1972].

16.5.1.2 Isotropic Etching

Usage of Isotropic Etchants

When etching silicon with aggressive acidic etchants, rounded isotropic patterns form. The method is widely used for:

1. Removal of work-damaged surfaces
2. Rounding of sharp anisotropically etched corners (to avoid stress concentration)
3. Removing of roughness after dry or anisotropic etching

4. Creating structures or planar surfaces in single-crystal slices (thinning)
5. Patterning single-crystal, polycrystalline, or amorphous films
6. Delineation of electrical junctions and defect evaluation (with preferential isotropic etchants)

For isotropic etching of silicon, the most commonly used etchants are mixtures of nitric acid (HNO_3) and hydrofluoric acids (HF). Water can be used as a diluent, but acetic acid (CH_3COOH) is preferred because it prevents the dissociation of the nitric acid better and so preserves the oxidizing power of HNO_3 which depends on the undissociated nitric acid species for a wide range of dilution [Robbins and Schwartz, 1960]. The etchant is called the HNA system; we will return to this etch system below.

Simplified Reaction Scheme

In acidic media, the Si etching process involves hole injection into the Si valence band by an oxidant, an electrical field, or photons. Nitric acid in the HNA system acts as an oxidant; other oxidants such as H_2O_2 and Br_2 also work [Tuck, 1975]. The holes attack the covalently bonded Si, oxidizing the material. Then follows a reaction of the oxidized Si fragments with OH^- and subsequent dissolution of the silicon oxidation products in HF. Consider the following reactions that describe these processes.

The holes are, in the absence of photons and an applied field, produced by HNO_3, together with water and trace impurities of HNO_2:

$$HNO_3 + H_2O + HNO_2 \rightarrow 2HNO_2 + 2OH^- + 2h^+ \qquad \text{(Reaction 16.1)}$$

The holes in Reaction 16.1 are generated in an autocatalytic process; HNO_2 generated in the above reaction re-enters into the further reaction with HNO_3 to produce more holes. With a reaction of this type, one expects an induction period before the oxidation reaction takes off, until a steady-state concentration of HNO_2 has been reached. This has been observed at low HNO_3 concentrations [Tuck, 1975]. After hole injection, OH^- groups attach to the oxidized Si species to form SiO_2, liberating hydrogen in the process:

$$Si^{4+} + 4OH^- \rightarrow SiO_2 + H_2 \qquad \text{(Reaction 16.2)}$$

Hydrofluoric acid (HF) dissolves the SiO_2 by forming the water-soluble H_2SiF_6. The overall reaction of HNA with Si looks like:

$$Si + HNO_3 + 6HF \rightarrow H_2SiF_6 + HNO_2 + H_2O + H_2 \text{ (bubbles)} \qquad \text{(Reaction 16.3)}$$

The simplification in the above reaction scheme is that only holes are assumed. In the actual Si acidic corrosion reaction, both holes and electrons are involved. The question of hole and/or electron participation in Si corrosion will be considered after the introduction of the model for the Si/electrolyte interfacial energetics. We will learn from that model that the rate-determining step in acidic etching involves hole injection in the valence band, whereas in alkaline anisotropic etching it involves electron injection in the conduction band by surface states. The reactivity of a hole injected in the valence band is significantly greater than that of an electron injected in the conduction band. The observation of isotropy in acidic etchants and anisotropy in alkaline etchants centers on this difference in reactivity.

Iso-Etch Curves

By the early 1960s, the isotropic HNA silicon etch was well characterized. Schwartz and Robbins published a series of four very detailed papers on the topic between 1959 and 1976 [Robbins and Schwartz, 1959; 1960; 1961; 1976]. Most of the material presented below is based on their work.

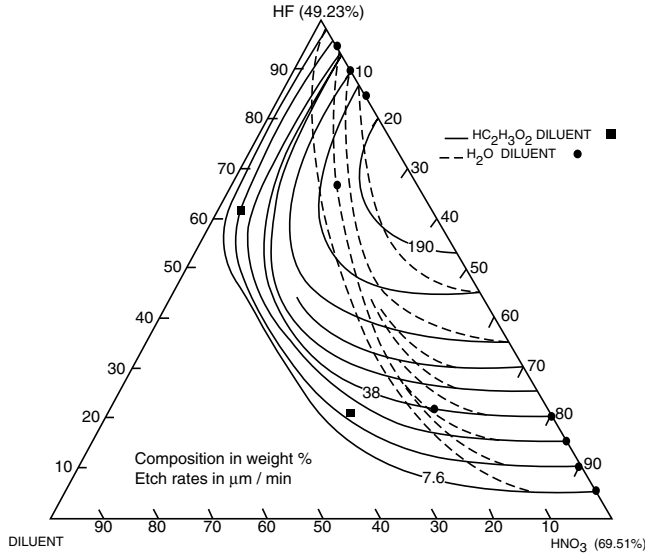


FIGURE 16.21 Iso-etch curves. From Robbins and Schwartz (1960), recalculated for one-sided Si etching and expressed in µm/min.

HNA etching results, represented in the form of iso-etch curves, for various weight percentages of the constituents are shown in Figure 16.21. For this work, normally available concentrated acids of 49.2 wt% HF and 69.5 wt% HNO_3 are used. Water as diluent is indicated by dash-line curves and acetic acid by solid-line curves. Also, as in Wong's representation [Wong, 1990], we have recalculated the curves from Schwartz et al to express the etch rate in µm/min and divided the authors' numbers by 2 as we are considering one-sided etching only. The highest etch rate is observed around a weight ratio HF-HNO_3 of 2:1 and is nearly 100 times faster than anisotropic etch rates. Adding a diluent slows down the etching. From these curves, the following characteristics of the HNA system can be summarized:

1. At high HF and low HNO_3 concentrations, the iso-etch curves describe lines of constant HNO_3 concentrations (parallel to the HF-diluent axis); consequently, the HNO_3 concentration controls the etch rate. Etching at those concentrations tends to be difficult to initiate and exhibits an uncertain induction period (see above). In addition, it results in relatively unstable silicon surfaces proceeding to slowly grow a layer of SiO_2 over a period of time. The etch is limited by the rate of oxidation, so that it tends to be orientation dependent and affected by dopant concentration, defects and catalysts (sodium nitrate often is used). In this regime the temperature influence is more pronounced, and activation energies for the etching reaction of 10 to 20 Kcal/mol have been measured.
2. At low HF and high HNO_3 concentrations, iso-etch curves are lines parallel to the nitric-diluent axis, i.e., they are at constant HF composition. In this case, the etch rate is controlled by the ability of HF to remove the SiO_2 as it is formed. Etches in this regime are isotropic and truly polishing, producing a bright surface with anisotropies of 1% or less (favoring the <110> direction) when used on <100> wafers [Wise et al., 1981]. An activation energy of 4 Kcal/mol is indicative of the diffusion limited character of the process; consequently, in this regime, temperature changes are less important.
3. In the region of maximal etch rate both reagents play an important role. The addition of acetic acid, as opposed to the addition of water, does not reduce the oxidizing power of the nitric acid until a fairly large amount of diluent has been added. Therefore, the rate contours remain parallel with lines of constant nitric acid over a considerable range of added diluent.

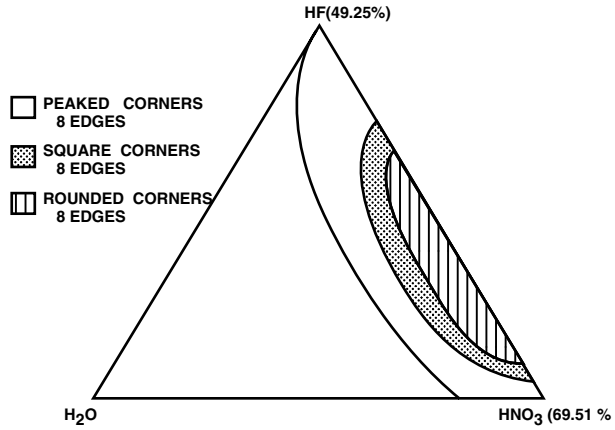


FIGURE 16.22 Topology of etched Si surfaces. (From Schwartz, B. and H. Robbins, *J. Electrochem. Soc.,* 123, 1903–1909, 1976. With permission.)

4. In the region around the HF vertex the surface reaction rate-controlled etch leads to rough, pitted Si surfaces and sharply peaked corners and edges. In moving towards the HNO_3 vertex, the diffusion-controlled reaction results in the development of rounded corners and edges and the rate of attack on (111) planes and (110) planes becomes identical in the polishing regime (anisotropy less than 1%; see point 2).

In Figure 16.22 we summarize how the topology of the Si surfaces depends strongly on the composition of the etch solution. Around the maximum etch rates the surfaces appear quite flat with rounded edges, and very slow etching solutions lead to rough surfaces [Schwartz and Robbins, 1976].

Arrhenius Plot for Isotropic Etching

The effect of temperature on the reaction rate in the HNA system was studied in detail by Schwartz and Robbins (1961). An Arrhenius plot for etching Si in 45% HNO_3, 20% HF and 35% $HC_2H_3O_2$, culled from their work, is shown in Figure 16.23. Increasing the temperature increases the reaction rate. The graph shows two straight-line segments, indicating a higher activation energy below 30°C and a lower one above this temperature. In the low temperature range, etching is preferential and the activation energy is associated with the oxidation reaction. At higher temperatures the etching leads to smooth surfaces and the activation energy is lower and associated with diffusion limited dissolution of the oxide [Schwartz and Robbins, 1961].

With isotropic etchants the etchant moves downward and outwards from an opening in the mask, undercuts the mask, and enlarges the etched pit while deepening it (Figure 16.24). The resulting isotropically etched features show more symmetry and rounding when agitation accompanies the etching (the process is diffusion limited). This agitation effect is illustrated in Figure 16.24. With agitation the etched feature approaches an ideal round cup; without agitation the etched feature resembles a rounded box [Petersen, 1982]. The flatness of the bottom of the rounded box generally is poor, since the flatness is defined by agitation.

Masking for Isotropic Silicon Etchants

Acidic etchants are very fast; for example, an etch rate for Si of up to 50 μ min^{-1} can be obtained with 66% HNO_3 and 34% HF (volumes of reagents in the normal concentrated form) [Kern, 1978; Kern and Deckert, 1978]. Isotropic etchants are so aggressive that the activation barriers associated with etching the different Si planes are not differentiated; all planes etch equally fast, making masking a real challenge.

Although SiO_2 has an appreciable etch rate of 300 to 800 Å/min in the HF:HNO_3 system, one likes to use thick layers of SiO_2 as a mask anyway, especially for shallow etching, as the oxide is so easy to form

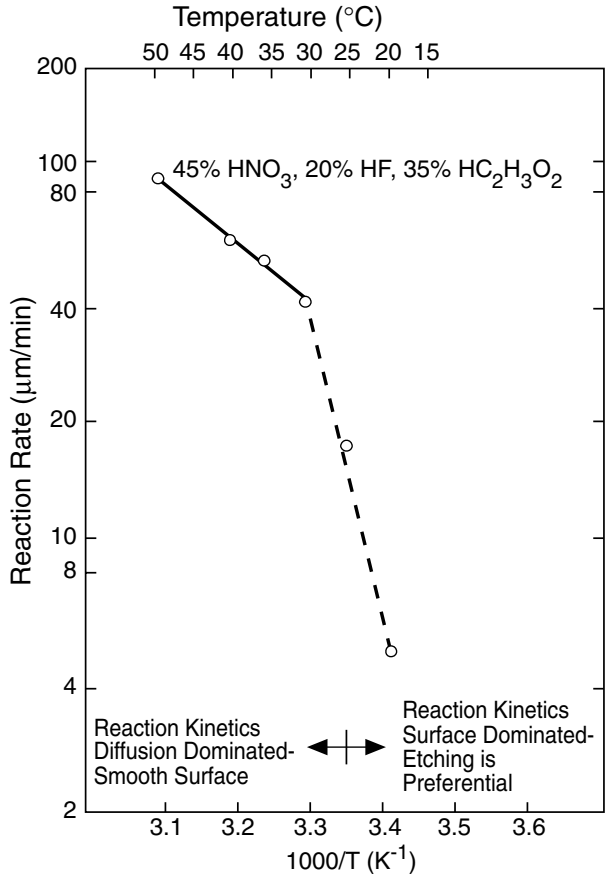


FIGURE 16.23 Etching Arrhenius plot. Temperature dependence of the etch rate of Si in HF:HNO_3:CH_3:COOH (1:4:3). (From Schwartz, B. and H. Robbins, *J. Electrochem. Soc.,* 108, 365–372, 1961. With permission.)

and pattern. A mask of nonetching Au or Si_3N_4 is needed for deeper etching. Photoresists do not stand up to strong oxidizing agents such as HNO_3, and neither does Al.

Silicon itself is soluble to a small extent in pure HF solutions; for a 48% HF, at 25°C, a rate of 0.3 Å/min was observed for n-type, 2-ohm cm (111)-Si. It was established that Si dissolution in HF is not due to oxidation by dissolved oxygen. Diluted HF etches Si at a higher rate because the reaction in aqueous solutions proceeds by oxidation of Si by OH^- groups [Hu and Kerr, 1967]. A typically buffered HF (BHF) solution has been reported to etch Si at radiochemically measured rates of 0.23 to 0.45 Å/min, depending on doping type and dopant concentration [Hoffmeister, 1969].

By reducing the dopant concentration (n or p) to below 10^{17} atoms/cm^3 the etch rate of Si in HNA is reduced by ~150 [Muraoka et al., 1973]. The doping dependence of the etch rate provides yet another means of patterning a Si surface (see next section). A summary of masks that can be used in acidic etching is presented in Table 16.6.

Dopant Dependence of Silicon Isotropic Etchants

The isotropic etching process is fundamentally a charge-transfer mechanism. This explains the etch rate dependence on dopant type and concentration. Typical etch rates with an HNA system (1:3:8) for n- or p-type dopant concentrations above 10^{18} cm^3 are 1 to 3 μm/min. As presented in the preceding section, a reduction of the etch rate by 150 times is obtained in n- or p-type regions with a dopant concentration of 10^{17} cm^{-3} or smaller [Muraoka et al., 1973]. This presumably is due to the lower mobile carrier

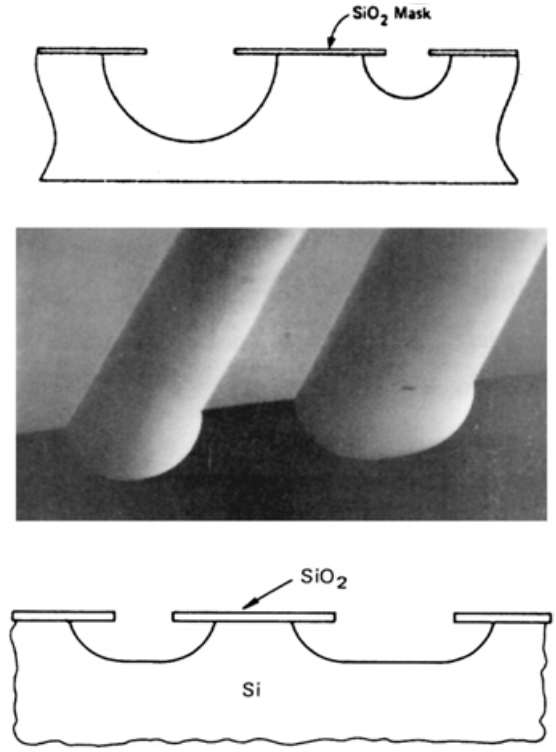


FIGURE 16.24 Isotropic etching of Si with (A) and without (B) etchant solution agitation.

TABLE 16.6 Masking Materials for Acidic Etchants[a]

	Etchants		
Masking	Piranha (4:1, H_2O_2:H_2SO_4)	Buffered HF (5:1 NH_4F:conc. HF)	HNA
Thermal SiO_2		0.1 μm/min	300–800 Å/min; limited etch time, thick layers often are used due to ease of patterning
CVD (450°C) SiO_2		0.48 μm/min	0.44 μm/min
Corning 7740 glass		0.063 μ/min	1.9 μ/min
Photoresist	Attacks most organic films	Good for short while	Resists do not stand up to strong oxidizing agents like HNO_3 and are not used
Undoped Si, polysilicon	Forms 30 Å of SiO_2	0.23 to 0.45 Å/min	Si 0.7 to 40 μm/min at room temperature; at a dopant concentration $<10^{17}$ cm^{-3} (n or p)
Black wax			Usable at room temperature
Au/Cr	Good	Good	Good
LPCVD Si_3N_4		1 Å/min	Etch rate is 10–100 Å/min; preferred masking material

[a] The many variables involved necessarily means that the given numbers are approximate only.

concentration available to contribute to the charge transfer mechanisms. In any event, heavily doped silicon substrates with high conductivity can be etched more readily than lightly doped materials. Dopant-dependent isotropic etching can also be exploited in an electrochemical set-up as described in the next section. Although doping does change the chemical etch rate, attempts to exploit these differences for industrial production have failed so far [Seidel, 1989]. This situation is different in electrochemical isotropic etching (see next section).

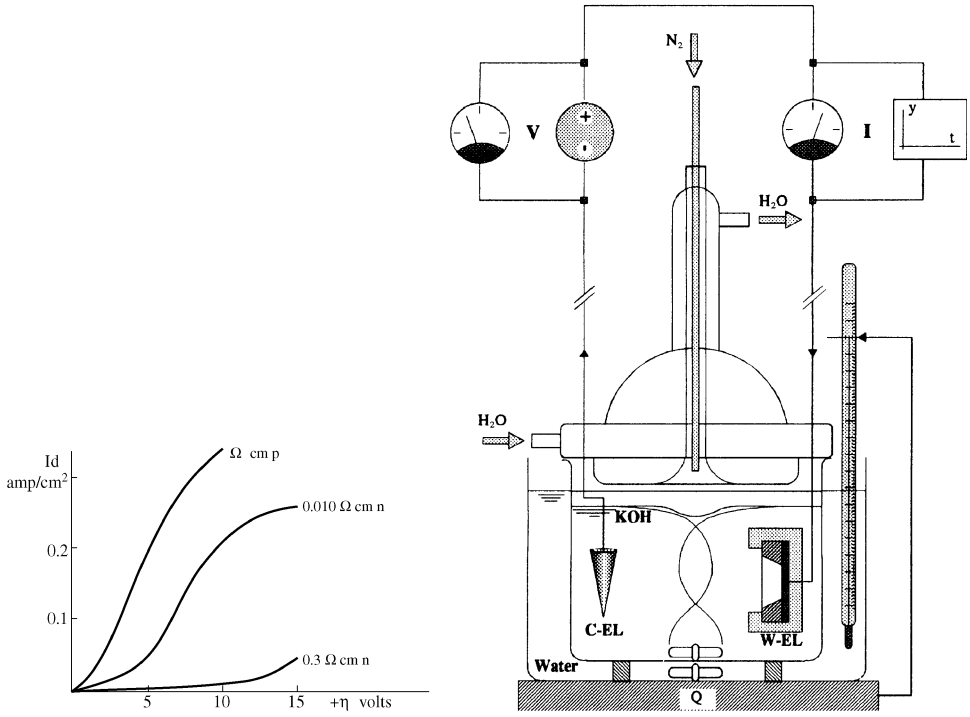


FIGURE 16.25 Electrochemical etching apparatus. W-EL: working electrode (Si), C-EL: counter electrode (e.g., Pt), Q = heat supplied. Inset: Current-voltage (I_d/η) curves in electrochemical etching of Si of various doping. Etch rate dependence on dopant concentration and dopant type for HF-anodic etching of silicon. (From van Dijk, H.J.A. and J. de Jonge, *J. Electrochem. Soc.,* 117, 553–554, 1970. With permission.)

Electrochemical Isotropic Silicon Etch-Etch Stop

Sometimes, a high temperature or extremely aggressive chemical etching process can be replaced by an electrochemical procedure utilizing a much milder solution, thus allowing a simple photoresist mask to be employed [Kern and Deckert, 1978]. In electrochemical acidic etching, with or without illumination of the corroding Si electrode, an electrical power supply is employed to drive the chemical reaction by supplying holes to the silicon surface (W-EL see Figure 16.25). A voltage is applied across the silicon wafer and a counter electrode (C-EL usually platinum) arranged in the same etching solution. Oxidation is promoted by a positive bias applied to the silicon causing an accumulation of holes in the silicon at the silicon/electrolyte interface. Under this condition, oxidation at the surface proceeds rapidly while the oxide is readily dissolved by the HF solution. No oxidant such as HNO_3 is needed to supply the holes; excess electron-hole pairs are created by the electrical field at the surface and/or by optical excitation, thereby increasing the etch rate. This technique proved successful in removing heavily doped layers, leaving behind the more lightly doped membranes in all possible dopant configurations: p on p^+, p on n^+, n on p^+, and n on n^+ [Theunissen et al., 1970; Meek, 1971]. This electrochemical etch-stop technique is demonstrated in the inset of Figure 16.25 [van Dijk et al., 1970]. A 5% HF solution is used, the electrolyte cell is kept in the dark at room temperature, and the distance between the Si anode and the Pt cathode in the electrochemical cell is 1 to 5 cm. Instead of using HF, one can substitute NH_4F (5 wt%) for the electrochemical etching as described by Shengliang et al. (1987). Shengliang reports a selectivity of n-silicon to n^+-silicon (0.001 Ωcm) of 300 with the latter etchant. In the inset in Figure 16.25 the current density vs. applied voltage across the anode and cathode during dissolution is plotted. The current density is related to the dissolution rate of silicon. It can be seen that p-type and heavily doped n-type materials can be dissolved at relatively low voltages, whereas n-type silicon with a lower doping level does not

dissolve at the same low voltages. Experiments in this same set-up with homogeneously doped silicon wafers show that n-type silicon of about 3.10^{18} cm^{-3} (<0.01 Ωcm) completely dissolves in these etching conditions, whereas n-type silicon of donor concentrations lower than 2.10^{16} cm^{-3} (>0.3 Ωcm) barely dissolves. For p-type silicon, dissolution is initiated when the acceptor concentration is higher than 5.10^{15} cm^{-3} (<3 Ωcm) and the dissolution rate further increases with increasing acceptor concentration. Under specific circumstances, namely high HF concentrations and low etching currents, porous Si may form [Bomchil et al., 1986].

The acidic electrochemical technique has not been used much in micromachining and is primarily used to polish surfaces. Since the etching rate increases with current density, high spots on the surface are more rapidly etched and very smooth surfaces result. The method of isotropic electrochemical etching has some major advantages which could make it a more important micromachining tool in the future. The etched surfaces are very smooth (say with an average roughness, R_a, of 7 nm), the process is room temperature and IC compatible, simpler resists schemes can be used as the process is much milder than etching in HNA, and etching can be controlled simply by switching a voltage on or off. We will pick up the discussion of anodic polishing, photo etching, and formation of porous silicon in HF solutions after gathering more insight in various etching models.

Preferential Etching

A variety of additives to the HNA system, mainly oxidants, can be included to modify the etch rate, surface finish or isotropy, rendering the etching baths preferential. It is clear that the effect of these additives will only show up in the reaction-controlled regime. Only additives that change the viscosity of the solution could modify the etch rate in the diffusion-limited regime, thereby changing the diffusion coefficient of the reactants [Tuck, 1975; Bogenschutz et al., 1967]. We will not review the effect of these additives any further; refer to Table 16.7 and the cited literature for further study [Yang, 1984; Chu and Gavaler, 1965; Archer, 1982; Schimmel and Elkind, 1973; Secco d'Aragona, 1972].

Problems with Isotropic Etchants

There are several problems associated with isotropic etching of Si. First, it is difficult to mask with high precision using a desirable and simple mask such as SiO_2 (etch rate is 2 to 3% of the silicon etch rate). Second, the etch rate is very agitation sensitive in addition to being temperature sensitive. This makes it difficult to control lateral as well as vertical geometries. Electrochemical isotropic etching (see above) and the development of anisotropic etchants in the late 1960s (see below) overcame many of these problems.

A comprehensive review of isotropic etchants solutions can be found in Kern and Deckert (1978). These authors also give a review of different techniques practiced in chemical etching such as immersion etching, spray etching, electrolytic etching, gas-phase etching, and molten salt etching (fusion techniques). In Table 16.7 some isotropic and preferential etchants and their specific applications are listed.

16.5.1.3 Anisotropic Etching

Introduction

Anisotropic etchants shape, also 'machine,' desired structures in crystalline materials. When carried out properly, anisotropic etching results in geometric shapes bounded by perfectly defined crystallographic planes. Anisotropic wet etching techniques, dating back to the 1960s at the Bell Laboratories, were developed mainly by trial and error. Going over some experimental data, before embarking upon the models, seems fitting. Moreover, we must keep in mind that for higher index planes most models fail.

Figure 16.1 shows a cross-section of a typical shape formed using anisotropic etching. The thinned membranes with diffused resistors could be used for a piezoresistive pressure sensor or an accelerometer. In the usual application, the wafer is selectively thinned from a starting thickness of 300 to 500 μm to form a diaphragm having a final thickness of 10 to 20 μm with precisely controlled lateral dimensions and a thickness control of the order of 1 μm or better. A typical procedure involves the steps summarized in Table 16.8 [Elwenspoek et al., 1994].

TABLE 16.7 Isotropic and Preferential Defect Etchants and Their Specific Applications

Etchant	Application	Remark
HF: 8 vol%, HNO_3: 75 vol%, and CH_3COOH: 17 vol%	n- and p-type Si, all planes, general etching	Planar etch; e.g., 5 μm/min at 25°C
1 part 49% HF, 1 part of (1.5 *M* CrO_3) (by volume)	Delineation of defects on (111), (100), and (110) Si without agitation	Yang etch[a]
5 vol parts nitric acid (65%), 3 vol parts HF (48%), 3 vol parts acetic acid (96%), 0.06 parts bromine	Polishing etchant used to remove damage introduced during lapping	So-called CP4 etchant; Heidenreich, U.S. Patent 2619414
HF	SiO_2	Si etch rate for 48% HF at 25°C is 0.3 Å/min with n-type 2 Ω cm (111) Si
1HF, $3HNO_3$, $10CH_3COOH$ (by volume)	Delineates defects in (111) Si; etches p^+ or n^+ and stops at p^- or n^-	Dash etch; p- and n-Si at 1300 Å/min in the [100] direction and 46 Å/min in the [111] direction at 25°C[b]
1HF, 1(5 *M* CrO_3) (by volume)	Delineates defects in (111); needs agitation; does not reveal etch pits well on (100) well	Sirtl etch[c]
2HF, 1(0.15 *M* $K_2Cr_2O_7$) (by volume)	Yields circular (100) Si dislocation etch pits; agitation reduces etch time	Secco etch[d]
60 ml HF, 30 ml HNO_3, 30 ml (5 *M* CrO_3), 2 g $Cu(NO_3)_2$, 60 ml CH_3COOH, 60 ml H_2O	Delineates defects in (100) and (111) Si; requires agitation	Jenkins etch[e]
2HF, 1 (1 *M* CrO_3) (by volume)	Delineates defects in (100) Si without agitation; works well on resistivities 0.6–15.0 Ωcm n- and p-types)	Schimmel etch[f]
2HF, 1 (1 *M* CrO_3), 1.5 (H_2O) (by volume)	Works well on heavily doped (100) silicon	Modified Schimmel[f]
$HF/KMnO_4/CH_3COOH$	Epitaxial Si	
H_3PO_4	Si_3N_4	160–180°C
KOH + alcohols	Polysilicon	85°C
$H_3PO_4/HNO_3/HC_2H_3O_2$	Al	40–50°C
HNO_3/BHF/water	Si and polysilicon	0.1 μm min^{-1} for single crystal Si

[a] Yang, K.H., *J. Electrochem. Soc.,* 131, 1140 (1984).
[b] Dash, W.C., *J. Appl. Phys.,* 27, 1193 (1956).
[c] Sirtl, E. and Adler, A., *Z. Metallkd.,* 52, 529 (1961).
[d] Secco d'Aragona, F., *J. Electrochem. Soc.,* 119, 948 (1972).
[e] Jenkins, M.W., *J. Electrochem. Soc.,* 124, 757 (1977).
[f] Schimmel, D.G., *J. Electrochem. Soc.,* 126, 479 (1979).

TABLE 16.8 Summary of the Process Steps Required for Anisotropic Etching of a Membrane [Elwenspoek et al., 1994]

Process	Duration	Process Temperature (°C)
Oxidation	Variable (hours)	900–1200
Spinning at 5000 rpm	20–30 sec	Room temperature
Prebake	10 min	90
Exposure	20 sec	Room temperature
Develop	1 min	Room temperature
Post-bake	20 min	120
Stripping of oxide (BHF:1:7)	±10 min	Room temperature
Stripping resist (acetone)	10–30 sec	Room temperature
RCA1 (NH_3(25%) + H_2O + H_2O_2:1:5:1)	10 min	Boiling
RCA2 (HCl + H_2O + H_2O_2:1:6:1)	10 min	Boiling
HF-dip (2% HF)	10 sec	Room temperature
Anisotropic etch	From minutes up to one day	70–100

The development of anisotropic etchants solved the lateral dimension control lacking in isotropic etchants. Lateral mask geometries on planar photoengraved substrates can be controlled with an accuracy and reproducibility of 0.5 μm or better, and the anisotropic nature of the etchant allows this accuracy to be translated into control of the vertical etch profile. Different etch stop techniques, needed to control the membrane thickness, are available. The invention of these etch stop techniques truly made items as shown in Figure 16.1 manufacturable.

While anisotropic etchants solve the lateral control problem associated with deep etching, they are not without problems. They are slower, even in the fast etching <100> direction, with etch rates of 1 μm/min or less. That means that etching through a wafer is a time-consuming process: to etch through a 300-μm-thick wafer one needs 5 hours. They also must be run hot to achieve these etch rates (85 to 115°C), precluding many simple masking options. Like the isotropic etchants, their etch rates are temperature sensitive; however, they are not particularly agitation sensitive, considered to be a major advantage.

Anisotropic Etchants

A wide variety of etchants have been used for anisotropic etching of silicon, including alkaline aqueous solutions of KOH, NaOH, LiOH, CsOH, NH_4OH, and quaternary ammonium hydroxides, with the possible addition of alcohol. Alkaline organics such as ethylenediamine, choline (trimethyl-2-hydroxy-ethyl ammonium hydroxide) or hydrazine with additives such as pyrocathechol and pyrazine are employed as well. Etching of silicon occurs without the application of an external voltage and is dopant insensitive over several orders of magnitude, but in a curious contradiction to its suggested chemical nature, it has been shown to be bias dependent [Allongue et al., 1993; Palik et al., 1987]. This contradiction will be explained with the help of the chemical models presented below.

Alcohols such as propanol and isopropanol butanol typically slow the attack on Si [Linde and Austin, 1992; Price, 1973]. The role of pyrocathechol [Finne and Klein, 1967] is to speed up the etch rate through complexation of the reaction products. Additives such as pyrazine and quinone have been described as catalysts by some [Reisman et al., 1979]; but this is contested by other authors [Seidel et al., 1990]. The etch rate in anisotropic etching is reaction rate controlled and thus temperature dependent. The etch rate for all planes increases with temperature and the surface roughness decreases with increasing temperature, so etching at the higher temperatures gives the best results. In practice, etch temperatures of 80 to 85°C are used to avoid solvent evaporation and temperature gradients in the solution.

Arrhenius Plots for Anisotropic Etching

A typical set of Arrhenius plots for <100>, <110> and <111> silicon etching in an anisotropic etchant (EDP, or ethylene-diamine/pyrocathechol) is shown in Figure 16.26 [Seidel et al., 1990]. It is seen that the temperature dependence of the etch rate is quite large and is less dependent on orientation. The slope differs for the different planes, i.e., (111) > (100) > (110). Lower activation energies in Arrhenius plots correspond to higher etch rates. The anisotropy ratio (AR) derived from this figure is

$$\mathrm{AR} = (hkl)_1 \text{ etch rate}/(hkl)_2 \text{ etch rate} \tag{16.29}$$

The AR is approximately 1 for isotropic etchants and can be as high as 400/200/1 for (110)/(100)/(111) in 50 wt% KOH/H_2O at 85°C. Generally, the activation energies of the etch rates of EDP are smaller than those of KOH. The (111) planes always etch slowest but the sequence for (100) and (110) can be reversed (e.g., 50/200/8 in 55 vol% ethylenediamine ED/H_2O; also at 85°C). The (110) Si plane etches 8 times slower and the (111) 8 times faster in KOH/H_2O than in ED/H_2O, while the (100) etches at the same rate [Kendall and Guel, 1985]. Working with alcohols and other organic additives often changes the relative etching rate of the different Si planes. Along this line, Seidel et al. (1990a; 1990b) found that the decrease in etch rate by adding isopropyl alcohol to a KOH solution was 20% for <100>, but almost 90% for <110>. As a result of the much stronger decrease of the etch rate on a (110) surface, the etch ratio of (100):(110) is reversed.

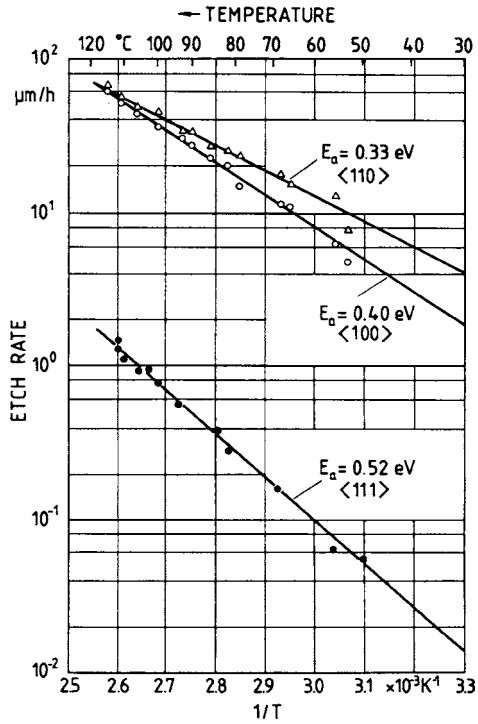


FIGURE 16.26 Vertical etch rates as a function of temperature for different crystal orientations: (100), (110) and (111). Etch solution is EDP (133 ml H_2O, 160 g pyrocatechol, 6 g pyrazine and 1 l ED). (From Seidel, H. et al., *J. Electrochem. Soc.*, 137, 3612–3626, 1990. With permission.)

Important Anisotropic Etchant Systems

In choosing an etchant, a variety of issues must be considered:

- Ease of handling
- Toxicity
- Etch rate
- Desired topology of the etched bottom surface
- IC-compatibility
- Etch stop
- Etch selectivity over other materials
- Mask material and thickness of the mask

The principal characteristics of four different anisotropic etchants are listed in Table 16.9. The most commonly used are KOH [Stoller and Wolff, 1966; Stoller, 1970; Forster and Singleton, 1966; Kenney, 1967; Lepselter, 1966; 1967; Waggener, 1970; Kragness and Waggener, 1973; Waggener et al., 1967a; 1967b; Bean and Ruyan, 1977; Rodgers et al., 1976; 1977; Ammar and Rodgers, 1980; Seidel et al., 1969; 1990; Kendall and de Guel, 1985; Lee, 1990; Noworolski et al., 1995; Waggener and Dalton, 1972; Weirauch, 1975; Clemens, 1973; Bean et al., 1974; Declercq et al., 1975] and ethylene-diamine/ pyrocatechol + water (EDP) [Finne and Klein, 1967; Reisman et al., 1979; Wu et al., 1986]; hydrazine-water rarely is used [Declercq et al., 1975; Mehregany and Senturia, 1988]. More recently, quaternary ammonium hydroxide solutions such as tetraethyl ammonium hydroxide (TEAH) have become more popular [Asano et al., 1976; Tabata et al., 1990]. Each has its advantages and problems. NaOH is not used much anymore [Pugacz-Muraszkiewicz and Hammond, 1977].

TABLE 16.9 Principal Characteristics of Four Different Anisotropic Etchants[a]

Etchant/Diluent/Additives/ Temperature	Etch Stop	Etch Rate (100) (μm/min)	Etch Rate Ratio (100)/(111)	Remarks	Mask (Etch Rate)
KOH/water, isopropyl alcohol additive, 85°C	$B > 10^{20}$ cm^{-3} reduces etch rate by 20	1.4	400 and 600 for (110)/(111)	IC incompatible, avoid eye contact, etches oxide fast, lots of H_2 bubbles	Photoresist (shallow etch at room temperature); Si_3N_4 (not attacked); SiO_2 (28 Å/min)
Ethylene diamine pyrocatechol (water), pyrazine additive, 115°C	$\geq 5 \times 10^{19}$ cm^{-3} reduces the etch rate by 50	1.25	35	Toxic, ages fast, O_2 must be excluded, few H_2 bubbles, silicates may precipitate	SiO_2 (2–5 Å/min); Si_3N_4 (1 Å/min); Ta, Au, Cr, Ag, Cu
Tetramethyl ammonium hydroxide (TMAH) (water), 90°C	$>4 \times 10^{20}$ cm^{-3} reduces etch rate by 40	1	From 12.5 to 50	IC compatible, easy to handle, smooth surface finish, few studies	SiO_2 etch rate is 4 orders of magnitude lower than (100) Si LPCVD Si_3N_4
N_2H_4/(water), isopropyl alcohol, 115°C	$>1.5 \times 10^{20}$ cm^{-3} practically stops the etch	3.0	10	Toxic and explosive, okay at 50% water	SiO_2 (<2 Å/min) and most metallic films; does not attack Al according to some authors [Wise, 1985]

[a] Given the many possible variables, the data in the table are only typical examples.

Hydrazine-water is explosive at high hydrazine concentrations (rocket fuel) and is a suspected carcinogen. Its use should be avoided for safety reasons. A 50% hydrazine/water solution is stable, though, and, according to Mehregany and Senturia (1988), excellent surface quality and sharply defined corners are obtained in Si. Also on the positive side, the etchant has a very low SiO_2 etch rate and will not attack most metal masks except for Al, Cu and Zn. According to Wise, on the other hand, Al does not etch in hydrazine either, but the etch produces rough Si surfaces [Wise, 1985].

Ethylenediamine in EDP reportedly causes allergic respiratory sensitization, and pyrocathechol is described as a toxic corrosive. The material is also optically dense, making end-point detection harder, and it ages quickly; if the etchant reacts with oxygen, the liquid turns to a red-brown color and it loses its good properties. If cooled down after etching, one gets precipitation of silicates in the solution. Sometimes one even gets precipitation during etching, spoiling the results. When preparing the solution, the last ingredient added should be the water, since water addition causes the oxygen sensitivity. All of the above make the etchant quite difficult to handle. But, a variety of masking materials can be used in conjunction with this etchant and it is less toxic than hydrazine. No sodium or potassium contamination occurs with this compound and the etch rate of SiO_2 is slow. The ratio of etch rates of Si and SiO_2 using EDP can be as large as 5000:1 (about 2 Å/min of SiO_2 compared to 1 μm/min of Si) which is much larger than the ratio in KOH a ratio of as high as 400:1 has been reported [Bean, 1978]. Importantly, the etch rate slows down at a lower boron concentration than with KOH. A typical fastest-to-slowest hierarchy of Si etch rates with EDP at 85°C according to Barth (1984) is (110) > (411) > (311) > (511) > (211) > (100) > (331) > (221) > (111).

The simple KOH water system is the most popular etchant. A KOH etch, in near saturated solutions (1:1 in water by weight) at 80°C, produces a uniform and bright surface. Nonuniformity of etch rate gets considerably worse above 80°C. Plenty of bubbles are seen emerging from the Si wafer while etching in KOH. The etching selectivity between Si and SiO_2 is not very good in KOH, as it etches SiO_2 too fast. KOH is also incompatible with the IC fabrication process and can cause blindness when it gets in contact with the eyes. The etch rate for low index planes is maximal at around 4 *M* (see Figure 16.27A [Peeters, 1994] and Lambrechts and Sansen [1992]). The surface roughness continuously decreases with increasing concentration as can be gleaned from Figure 16.27B. Since the difference in etch rates for different KOH concentrations is small, a highly concentrated KOH (e.g., 7 *M*) is preferred to obtain a smooth surface on low index planes.

Except at very high concentrations of KOH, the etched (100) plane becomes rougher the longer one etches. This is thought to be due to the development of hydrogen bubbles, which hinder the transport of fresh solution to the silicon surface [Ternz, 1988]. Average roughness, R_a, is influenced strongly by fluid agitation. Stirring can reduce the R_a values over an order of magnitude, probably caused by the more efficient removal of hydrogen bubbles from the etching surface when stirring [Gravesen, 1986]. The silicon etch rate as a function of KOH concentration is shown in Figure 16.27C [Seidel et al., 1990].

Herr and Baltes (1991) found that the high-index crystal planes exhibit the highest etch rates for 6 *M* KOH and that for lower concentrations the etch bottoms disintegrate into microfacets. In 6 *M* KOH, the etch-rate order is (311) > (144) > (411) > (133) > (211) > (122). These authors could not correlate the particular etch rate sequence with the measured activation energies. This is in contrast to lower activation energies corresponding to higher etching rates for low index planes as shown in Figure 16.26. Their results obtained on large open area structures differ significantly from previous ones obtained by underetching special mask patterns. The vertical etching rates obtained here are substantially higher than the underetching rates described elsewhere, and the etch rate sequence for different planes is also significantly different. These results suggest that crevice effects may plan an important role in anisotropic etching.

Besides KOH [Clark and Edell, 1987], other hydroxides have been used, including NaOH [Allongue et al., 1993; Pugacz-Muraszkiewicz and Hammond, 1977], CsOH [Clark et al., 1988] and NH_4OH [Schnakenberg et al., 1990]. A major disadvantage of KOH is the presence of alkali ions, which are detrimental to the fabrication of sensitive electronic parts. Work is under way to find anisotropic etchants

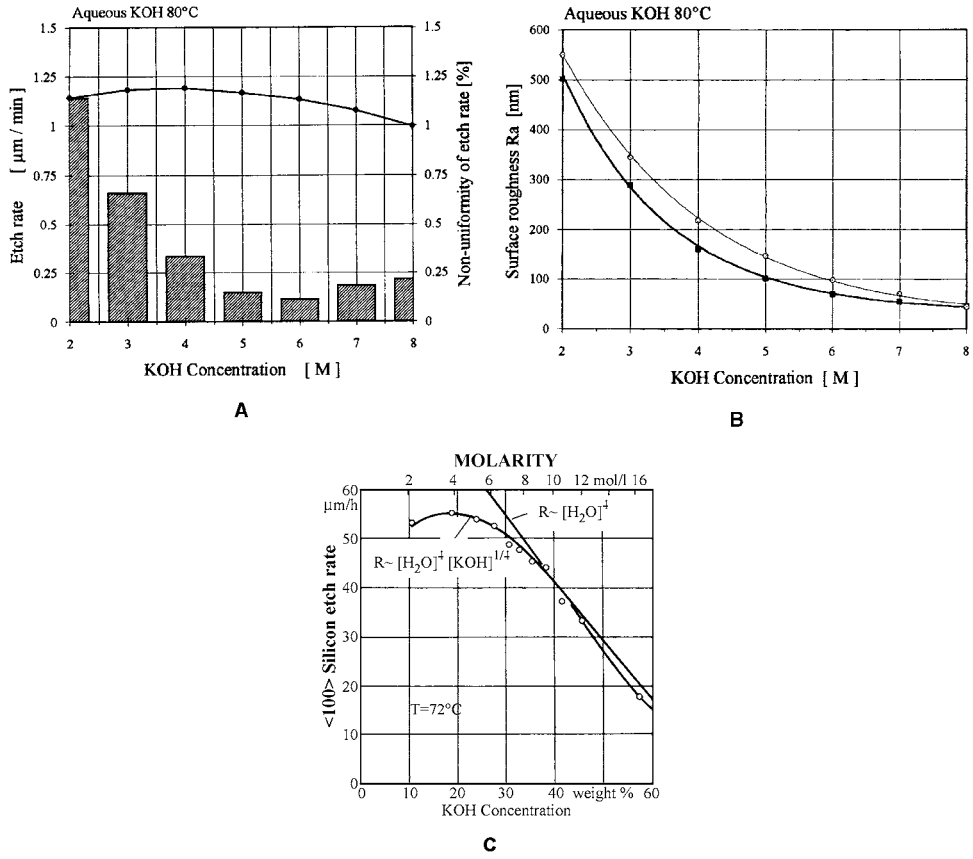
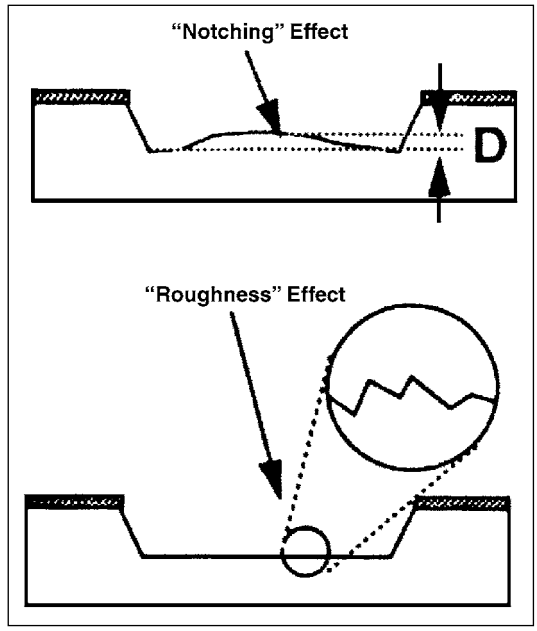


FIGURE 16.27 Anisotropic etching of silicon. (A) Silicon (100) etch rate (line) and nonuniformity of etch rate (column) in KOH at 80°C as a function of KOH concentration. The etch rate for all low index planes is maximal at around 4 *M*. (B) Silicon (100) surface roughness (Ra) in aqueous KOH at 80°C as a function of concentration for a 1-hour etch time (thin line) and for an etch depth of 60 µm (thick line). (C) Silicon (100) etch rate as a function of KOH concentration at a temperature of 72°C. (A and B from Peeters, E., Ph.D. thesis, 1996, KUL, Belgium. With permission. C from Seidel et al., *J. Electrochem. Soc.*, 137, 3612–3626, 1990. With permission.)

that are more compatible with CMOS processing and that are neither toxic nor harmful. Two examples are ammonium hydroxide-water (AHW) mixtures [Schnakenberg et al., 1990] and tetramethyl ammonium hydroxide-water (TMAHW) mixtures [Tabata et al., 1990; Schnakenberg et al., 1990]. TMAHW solutions do not decompose at temperatures below 130°C, a very important feature from the viewpoint of production. They are nontoxic and can be handled easily. TMAHW solutions also exhibit excellent selectivity to silicon oxide and silicon nitride. At a solution temperature of 90°C and 22 wt% TMAH, a maximum (100) silicon etch rate of 1.0 µm/min is observed, 1.4 µm/min for (110) planes (this is higher than those observed with EDP, AHW, hydrazine water and tetraethyl ammonium hydroxide [TEA], but slower than those observed for KOH and an anisotropy ratio, AR(100)/(111), of between 12.5 and 50 [Tabata et al., 1992]). From the viewpoint of fabricating various silicon sensors and actuators, a concentration above 22 wt% is preferable, since lower concentrations result in larger roughness on the etched surface. However, higher concentrations give a lower etch rate and lower etch ratio (100)/(111). Tabata (1995) also studied the etching characteristics of pH-controlled TMAHW. To obtain a low aluminum etching rate of 0.01 µm/min, pH values below 12 for 22 wt% TMAHW were required. At those pH values the Si(100) etching rate is 0.7 µm/min.



Macroscopic roughness (notching effect) and microscopic roughness.

Surface Roughness and Notching

Anisotropic etchants frequently leave too rough a surface behind, and a slight isotropic etch is used to 'touch-up'. A distinction must be made between ***macroscopic*** and ***microscopic roughness***. Macroscopic roughness, also referred to as notching or pillowing, results when centers of exposed areas etch with a seemingly lower average speed compared with the borders of the areas, so that the corners between sidewalls and (100) ground planes are accentuated. Membranes or double-sided clamped beams (microbridges) therefore tend to be thinner close to the clamped edges than in the center of the structure. This difference can be as large as 1 to 2 μm, which is quite considerable if one is etching 10 to 20 μm thick structures. Notching increases linearly with etch depth but decreases with higher concentrations of KOH. The microscopic smoothness of originally mirror-like polished wafers can also be degraded into microscopic roughness. It is this type of short-range roughness we referred to in discussing Figure 16.27B above.

Masking for Anisotropic Etchants

Etching through a whole wafer (400 to 600 μm) takes several hours (a typical wet anisotropic etch rate being 1.1 μm/min), definitely not a fast process. When using KOH, SiO_2 cannot be used as a masking material for features requiring that long an exposure to the etchants. The SiO_2 etch rate as a function of KOH concentration at 60°C is shown in Figure 16.28. There is a distinct maximum at 35 wt% KOH of nearly 80 nm/hr. The shape of this curve will be explained further below on the basis of Seidel et al.'s model. Experiments have shown that even a 1.5-μm-thick oxide is not sufficient for the complete etching of a 380-μm-thick wafer (6 hours) because of pinholes in the oxide [Lambrechts and Sansen, 1992]. The etch rate of thermally grown SiO_2 in KOH-H_2O somewhat varies and apparently depends not only on the quality of the oxide, but also on the etching container and the age of the etching solution, as well as other factors [Kendall, 1979]. The Si/SiO_2 selectivity ratio at 80°C in 7 *M* KOH is 30 ± 5. This ratio increases with decreasing temperature; reducing the temperature from 80 to 60°C increases the selectivity ratio from 30 to 95 in 7 *M* KOH [Kendall, 1975]. Thermal oxides are under strong compressive stress due to the fact that in the oxide layer one silicon atom takes nearly twice as much space as in single crystalline Si (see also Madou [1997, chap. 3]). This might have severe consequences; for example, if the oxide mask is stripped on one side of the wafer, the wafer will bend. Atmospheric pressure chemical vapor deposited (APCVD) SiO_2 tends to exhibit pinholes and etches much faster than thermal oxide.

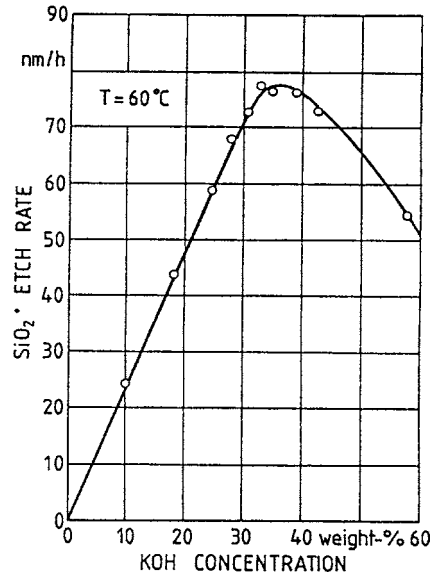


FIGURE 16.28 The SiO_2 etch rate in nm/hr as a function of KOH concentration at 60°C. (From Seidel, H. et al., *J. Electrochem. Soc.,* 137, 3612–3626, 1990. With permission.)

Annealing of APCVD oxide removes the pinholes but the etch rate in KOH remains greater by a factor of 2 to 3 than that of thermal oxide. Low pressure chemical vapor deposited (LPCVD) oxide is a mask material of comparable quality as thermal oxide. The etch rate of SiO_2 in EDP is smaller by two orders of magnitude than in KOH.

For prolonged KOH etching, a high density silicon nitride mask has to be deposited. A low pressure chemical vapor deposited (LPCVD) nitride generally serves better for this purpose than a less dense plasma deposited nitride [Puers, 1991]. With an etch rate of less than 0.1 nm/min, a 400-Å layer of LPCVD nitride suffices to mask against KOH etchant. The etch selectivity Si/Si_3N_4 was found to be better than 10^4 in 7 *M* KOH at 80°C. The nitride also acts as a good ion-diffusion barrier, protecting sensitive electronic parts. Nitride can easily be patterned with photoresist and etched in a CF_4/O_2-based plasma or, in a more severe process, in H_3PO_4 at 180°C (10 nm/min) [Buttgenbach, 1991]. Nitride films are typically under a tensile stress of about 1×10^9 Pa. If in the overall processing of the devices, nitride deposition does not pose a problem, KOH emerges as the preferential anisotropic wet etchant. For dopant dependent etching, EDP is the better etchant and generally better suited for deep etching since its oxide etch rate is negligible (<5 Å/min).

Oxide and nitride are masking for anisotropic etchants to varying degrees with both mask types being used. When these layers are used to terminate an etch in the [100] direction, a low etch rate of the mask layer allows overetching of silicon, to compensate for wafer thickness variations. A KOH solution etches SiO_2 at a relatively fast rate of 1.4 to 3 nm/min so that Si_3N_4 or Au/Cr must be used as a mask against KOH for deep and long etching.

Backside Protection

In many cases it is necessary to protect the backside of a wafer from an isotropic or anisotropic etchant. The backside is either mechanically or chemically protected. In the mechanical method the wafer is held in a holder, often made from Teflon. The wafer is fixed between Teflon-coated O-rings which are carefully aligned in order to avoid mechanical stress in the wafer. In the chemical method, waxes or other organic coatings are spun onto the back side of the wafer. Two wafers may be glued back-to-back for faster processing.

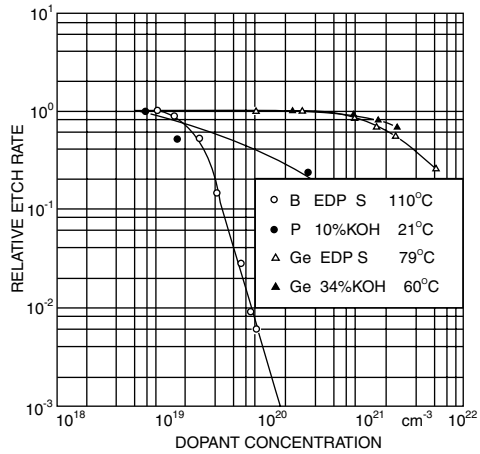


FIGURE 16.29 Relative etch rate for (100) Si in EDP and KOH solutions as a function of concentration of boron, phosphorus and germanium. (From Seidel, H. et al., *J. Electrochem. Soc.,* 137, 3626–3632, 1990. With permission.)

Etch Rate and Etch Stops

The Si etch rate, R, as a function of KOH concentration at 72°C, was shown in Figure 16.27C. The etch rate has a maximum at about 20% KOH. The best fit for this experimentally determined etch rate, for most KOH concentrations, is [Seidel et al., 1990a; 1990b]

$$R = k[H_2O]^4[KOH]^{\frac{1}{4}} \tag{16.30}$$

Any model of anisotropic etching will have to explain this peculiar dependency on the water and KOH concentration, as well as the fact that all anisotropic etchant systems of Table 16.9 exhibit drastically reduced etch rates for high boron concentrations in silicon ($\geq 5 \times 10^{19}$ cm^{-3} solid solubility limit). Other impurities (P, Ge) also reduce the etch rate, but at much higher concentrations (see Figure 16.29 [Seidel et al., 1990]). Boron typically is incorporated using ion implantation (thin layers) or liquid/solid source deposition (thick layers >1 μm). These doped layers are used as very effective etch stop layers (see below). Hydrazine or EDP, which displays a smaller (100)-to-(111) etch rate ratio (~35) than KOH, exhibits a stronger boron concentration dependency. The etch rate in KOH is reduced by a factor of 5 to 100 for a boron concentration larger than 10^{20} cm^{-3}. When etching in EDP, the factor climbs to 250 [Bogh, 1971]. With TMAHW solutions, the Si etch rate decreases to 0.01 μm/min for boron concentrations of about 4×10^{20} cm^{-3} [Steinsland et al., 1995]. The mechanism eludes us, but Seidel et al.'s model (see below) gives the most plausible explanation for now. Some of the different mechanisms to explain etch stop effects that have been suggested follow:

1. Several observations suggest that doping leads to a more readily oxidized Si surface. Highly boron- or phosphorus-doped silicon in aqueous KOH spontaneously can form a thin passivating oxide layer [Palik et al., 1982; 1985]. The boron-oxides and -hydroxides initially generated on the silicon surface are not soluble in KOH or EDP etchants [Petersen, 1982]. The substitutional boron creates local tensile stress in the silicon, increasing the bond strength so that a passivating oxide might be more readily formed at higher boron concentrations. Boron-doped silicon has a high defect density (slip planes), encouraging oxide growth.
2. Electrons produced during oxidation of silicon are needed in a subsequent reduction step (hydrogen evolution in Reaction 16.2). When the hole density passes 10^{19} cm^{-3} these electrons combine with holes instead, thus stopping the reduction process [Palik et al., 1982]. Seidel et al.'s model follows this explanation (see below).

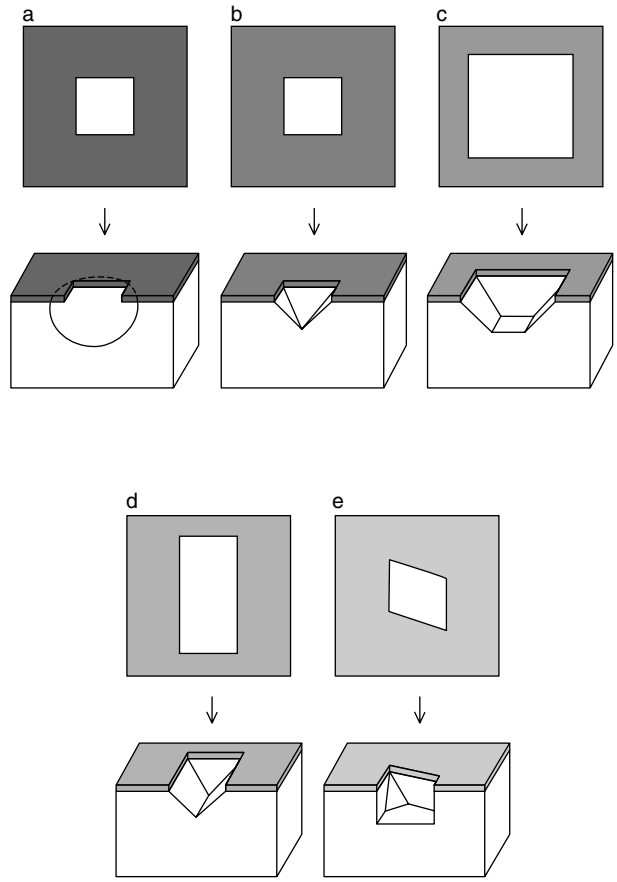


FIGURE 16.30 Isotropic and anisotropic etched features in <100> and <110> wafers. (a) isotropic etch; (b) to (e) anisotropic etch. (a) to (d): <100> oriented wafers and (e): <110> oriented wafer.

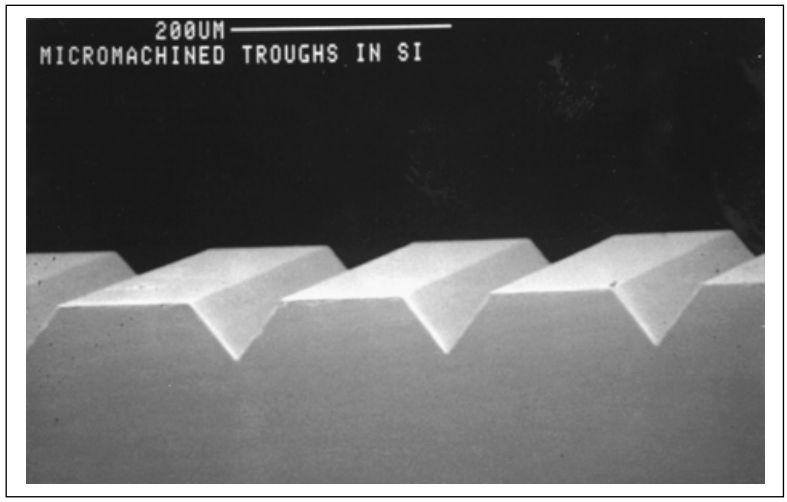
3. Silicon doped with boron is under tension as the smaller boron atoms enter the lattice substitutionally. The large local tensile stress at high boron concentration makes it energetically more favorable for the excess boron (above 5×10^{19} cm^{-3}) to enter interstitial sites. The strong B-Si bonds bind the lattice rigidly. With high enough doping the high binding energy can stop etching [Petersen, 1982]. This hypothesis is similar to item 1, except that no oxide formation is invoked.

In what follows we review the results of some typical anisotropic etching experiments.

16.5.1.4 Anisotropically Etched Structures

Examples

In Figure 16.30 we compare a wet isotropic etch (a) with examples of anisotropic etches (b to e). In the anisotropic etching examples, a square (b and c) and a rectangular pattern (d) are defined in an oxide mask with sides aligned along the <110> directions on a <100>-oriented silicon surface. The square openings are precisely aligned (within one or two degrees) with the <110> directions on the (100) wafer surface to obtain pits that conform exactly to the oxide mask rather than undercutting it. Most (100) silicon wafers have a main flat parallel to a <110> direction in the crystal, allowing for an easy alignment of the mask (see Figure 16.5). Etching with the square pattern results in a pit with well-defined {111} sidewalls (at angles of 54.74° to the surface) and a (100) bottom.



Long V-shaped grooves in a (100) Si wafer.

The dimensions of the hole at the bottom of the pit, as we saw above, are given by Eq. (16.2). The larger the square opening in the mask, the deeper the point where the {111} sidewalls of the pit intersect. If the oxide opening is wide enough, i.e., $W_m > \sqrt{2}\ z$ (with $z = 600$ µm for a typical 6-in. wafer, this means $W_m > 849$ µm), the {111} planes do not intersect within the wafer (see also earlier in this chapter). The etched pit in this particular case extends all the way through the wafer, creating a small square opening on the bottom surface. As shown in Figure 16.30 (b to d), no under-etching of the etch mask is observed due to the perfect alignment of the concave oxide mask opening with the <110> direction. In Figure 16.30a, an undercutting isotropic etch (acidic) is shown. Misalignment in the case of an anisotropic etch still results in pyramidical pits, but the mask will also be severely undercut. A rectangular pattern aligned along the <110> directions on a <100> wafer leads to ***long V-shaped grooves*** (see Figure 16.30d) or an open slit, depending on the width of the opening in the oxide mask.

Using a properly aligned mask on a <110> wafer, holes with four vertical walls ({111} planes) result (see Figure 16.30e and Figure 16.31A and C). Figure 16.31B shows that a slight mask misorientation

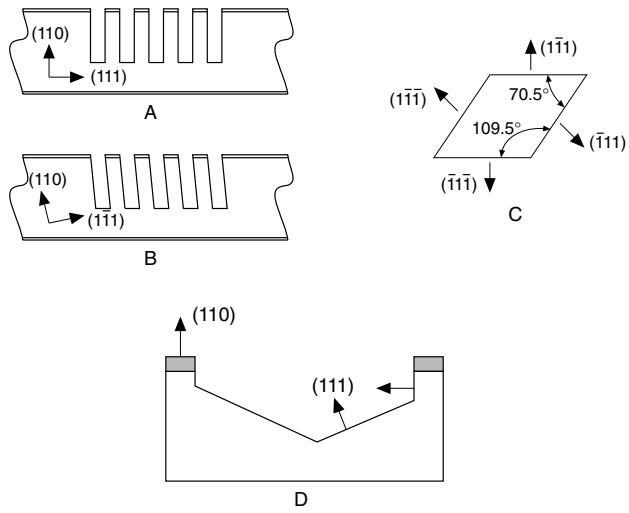


FIGURE 16.31 Anisotropic etching of <110> wafers. (A) Closely spaced grooves on correctly oriented (110) surface. (B) Closely spaced grooves on misoriented <110> wafer. (C) Orientations of the {111} planes looking down on a (110) wafer. (D) Shallow slanted (111) planes eventually form the bottom of the etched cavity.

leads to all skewed sidewalls. A U-groove based on a rectangular mask with the long sides along the <111> directions and anisotropically etched in (110) silicon has a complex shape delineated by six {111} planes, four vertical and two slanted (see Figure 16.31D). Before emergence of {111} planes, the U-groove is defined by four vertical (111) planes and a horizontal (110) bottom. Self-stopping occurs when the tilted end planes intersect at the bottom of the groove. It is easy to etch long, narrow U-grooves very deeply into a <110> silicon wafer. However, it is impossible to etch a short, narrow U-groove deeply into a slice of silicon [Kendall, 1979], because the narrow dimension of the groove is quickly limited by slow-etching {111} planes that subtend an angle of 35° to the surface and cause etch termination. At a groove of length $L = 1$ mm on the top surface, etching will stop when it reaches a depth of 0.289 mm, i.e., $D_{max} = L/2\sqrt{3}$. For very long grooves, the tilted end planes are too far apart to intersect in practical cases, making the end effects negligible compared to the remaining U-shaped part of the groove.

A laser can be used to melt or 'spoil' the shallow (111) surfaces, making it possible to etch deep vertical-walled holes through a (110) wafer as shown in Figure 16.32A [Schumacher et al., 1994; Barth et al., 1985; Seidel and Csepregi, 1988]. The technique is illustrated in Figure 16.32B. The absorbed energy of a Nd:YAG laser beam causes a local melting or evaporation zone enabling etchants to etch the shallow (111) planes in the line-of-sight of the laser. Etching proceeds until 'unspoiled' (111) planes are encountered. Some interesting resulting possibilities, including partially closed microchannels, are shown in Figure 16.32C [Schumacher et al., 1994; Alavi et al., 1991]. Note that with this method it is possible to use <111> wafers for micromachining. The light of the Nd:YAG laser is very well suited for this micromachining technique due to the 1.17-eV photon energy, just exceeding the band gap energy of Si. Details on this laser machining process can be found, for example, in Alavi et al. (1991; 1992).

Especially when machining surface structures by undercutting, the orientation of the wafer is of extreme importance. Consider, for example, the formation of a bridge in Figure 16.33A [Barth et al., 1985]. When using a (100) surface, a suspension bridge cannot form across the etched V-groove; two independent truncated V-grooves flanking a mesa structure result instead. To form a suspended bridge it must be oriented away from the <110> direction. This in contrast with a (110) wafer where a microbridge crossing a V-groove with a 90° angle will be undercut. Convex corners will be undercut by etchant, allowing formation of cantilevers as shown in Figure 16.33B. The diving board shown forms by undercutting starting at the convex corners.

To create vertical (100) faces, as shown in Figure 16.10, in general only KOH works (not EDP or TMAHW) and it has to happen in high-selectivity conditions (low temperature, low concentration: 25 wt% KOH, 60°C). Interestingly, high concentration KOH (45 wt%) at higher temperatures (80°C) produces a smooth sidewall, controllable and repeatable at an angle of 80°. EDP produces 45° angled planes and TMAHW usually makes a 30° angle [Palik et al., 1985].

Alignment Patterns

When alignment of a pattern is critical, pre-etch alignment targets become useful to delineate the planes of interest since the wafer flats often are aligned to ±1° only. In order to find the proper alignment for the mask, a test pattern of closely spaced lines can be etched (see Figure 16.34). The groove with the best vertical walls determines the proper final mask orientation. Along this line, Ciarlo (1987) made a set of lines 3 mm long and 8 μm wide, fanning out like spokes in a wagon wheel at angles 0.1° apart. This target was printed near the perimeter of the wafer and then etched 100 μm into the surface. Again, by evaluating the undercut in this target the correct crystal direction could be determined. Alignment with better than 0.05° accuracy was accomplished this way. Similarly, to obtain detailed experimental data on crystal orientation dependence of etch rates, Seidel et al. (1990) used a wagon-wheel or star-shaped mask (e.g., made from CVD-Si_3N_4; SiH_4 and NH_3 at 900°C), consisting of radially divergent segments with an angular separation of one degree. Yet finer 0.1° patterns were made around the principal crystal directions. The etch pattern emerging on a <100> oriented wafer covered with such a mask is shown in Figure 16.35A. The blossom-like figure is due to the total underetching of the passivation layer in the vicinity of the center of the wagon wheel,

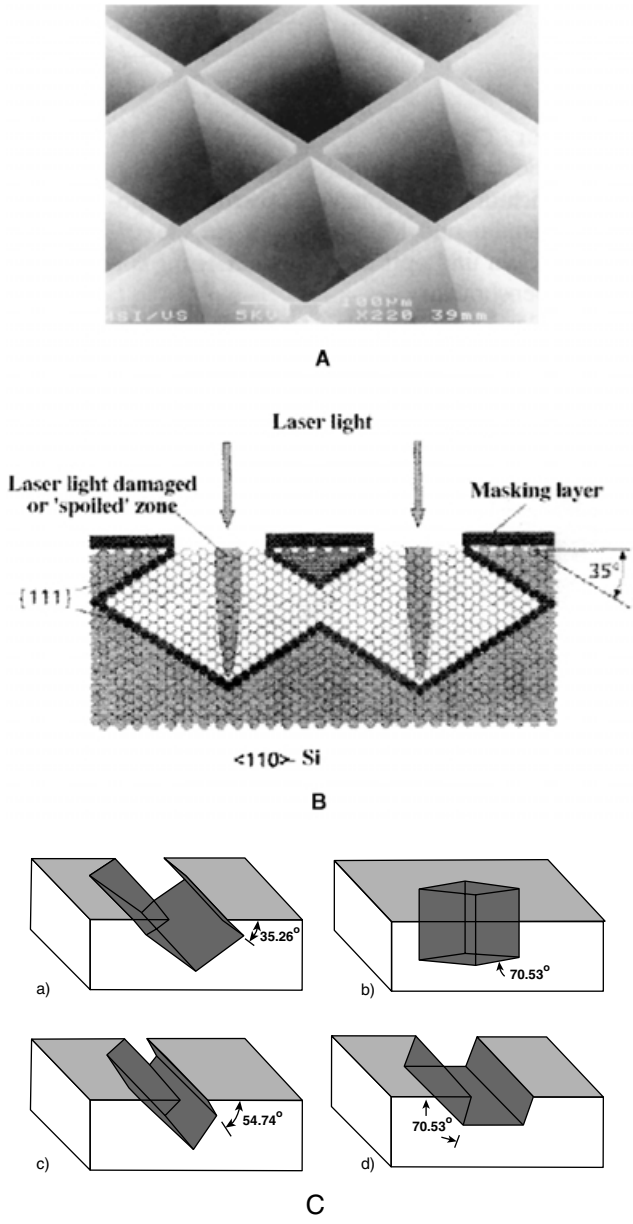


FIGURE 16.32 Laser/KOH machining. (A) Holes through a (110) Si wafer created by laser spoiling and subsequent KOH etching. The two sets of (111) planes making an angle of 70° are the vertical walls of the hole. The (111) planes making a 35° angle with the surface tend to limit the depth of the hole but laser spoiling enables one to etch all the way through the wafer (see also B [c]). (B) After laser spoiling, the line-of-sight (111) planes are spoiled and etching proceeds until unspoiled (111) planes are reached. (C) Some of the possible features rendered by laser spoiling. (From Schumacher, A. et al., *Technische Rundschau,* 86, 20–23, 1994. With permission.)

leaving an area of bare exposed Si. The radial extension of the bare Si area depends on the crystal orientation of the individual segments, leading to a different amount of total underetching. The observation of these blossom-like patterns was used for qualitative guidance of etching rates only. In order to establish quantitative numbers for the lateral etch rates, the width, *w*, of the overhanging passivation layer was measured with an optical line-width measurement system (see Figure 16.35B).

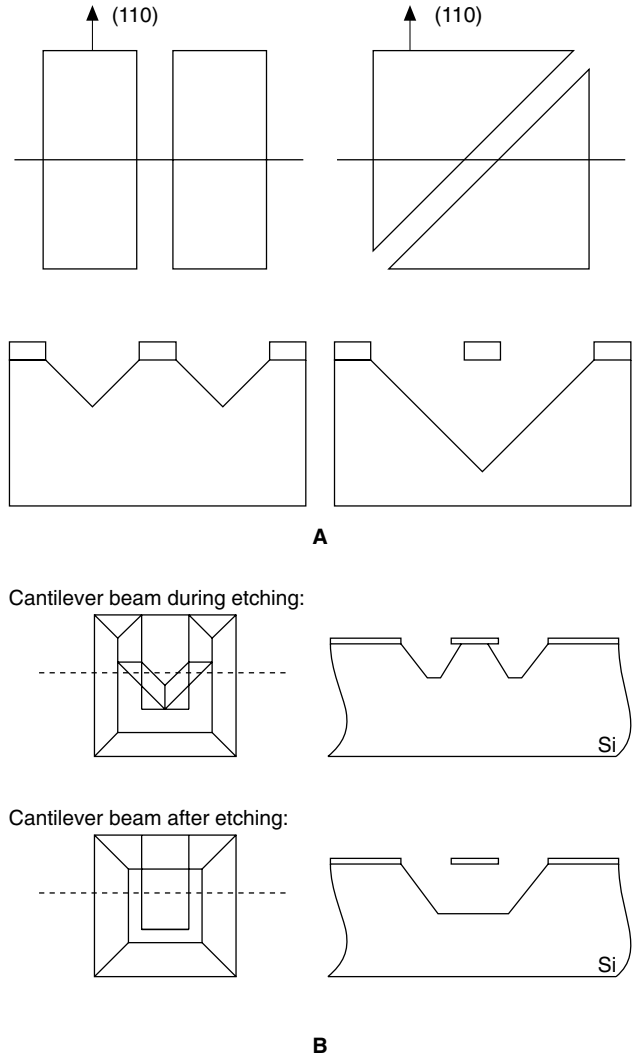


FIGURE 16.33 How to make (A) a suspension bridge from a (100) Si wafer and (B) a diving board from a (110) Si wafer [Barth et al., 1985].

Laser beam reflection was used to identify the crystal planes and ellipsometry was used to monitor the etching rate of the mask itself. Lateral etch rates determined in this way on <100>- and <110>-oriented wafers at 95°C in EDP (470 ml water, 11 ED, 176 g pyrocatechol) and at 78°C in a 50% KOH solution are shown in Figure 16.36. Etch rates shown are normal to the actual crystal surface and are conveniently described in a polar plot in which the distance from the origin to the polar plot surface (or curve in two dimensions) indicates the etch rate for that particular direction. Note the deep minima at the {111} planes. It can also be seen that in KOH the peak etch rates are more pronounced. A further difference is that with EDP the minimum at {111} planes is steeper than with KOH. For both EDP and KOH, the etch rate depends linearly on misalignment. All the above observations have important consequences for the interpretation of anisotropy of an etch (see below). The difference between KOH and EDP etching behavior around the {111} minima has the direct practical consequence that it is more important for etching in EDP to align the crystallographic direction more precisely than in KOH [Elwenspoek et al., 1994].

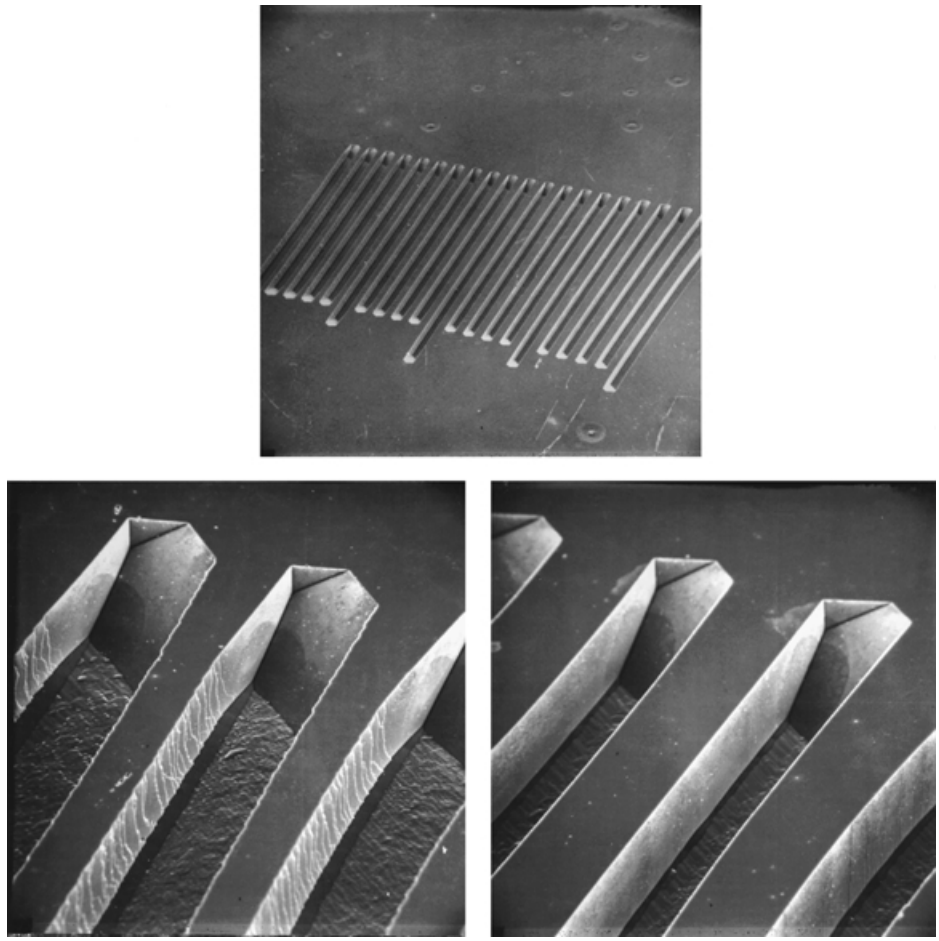


FIGURE 16.34 Test pattern of U-grooves in a <110> wafer to help in the alignment of the mask; final alignment is done with the groove that exhibits the most perfect long perpendicular walls.

When determining etch rates without using underetching masks but by using vertical etching of beveled silicon samples, results are quite different than when working with masked silicon [Herr and Baltes, 1991]. The etch rates on open areas of beveled structures are much larger than in underetching experiments with masked silicon, and different crystal planes develop. Herr et al. conclude that crevice effects may play an important role in anisotropic etching. Elwenspoek et al.'s model [Elwenspoek, 1993; Elwenspoek et al. 1994], analyzed below, is the only model which predicts such a crevice effect. He explains why, when etchants are in a small restricted crevice area and are not refreshed fast enough, etching rates slow down and increase anisotropy.

16.5.2 Chemical Etching Models

16.5.2.1 Introduction

Lots of conflicting data exist in the literature on the anisotropic etch rates of the different Si planes, especially for the higher index planes. This is not too surprising, given the multiple parameters influencing individual results: temperature, stirring, size of etching feature (i.e., crevice effect), KOH concentration, addition of alcohols and other organics, surface defects, complexing agents, surfactants, pH, cation influence etc. More rigorous experimentation and standardization will be needed, as well as better etching models, to better understand the influence of all these parameters on etch rates.

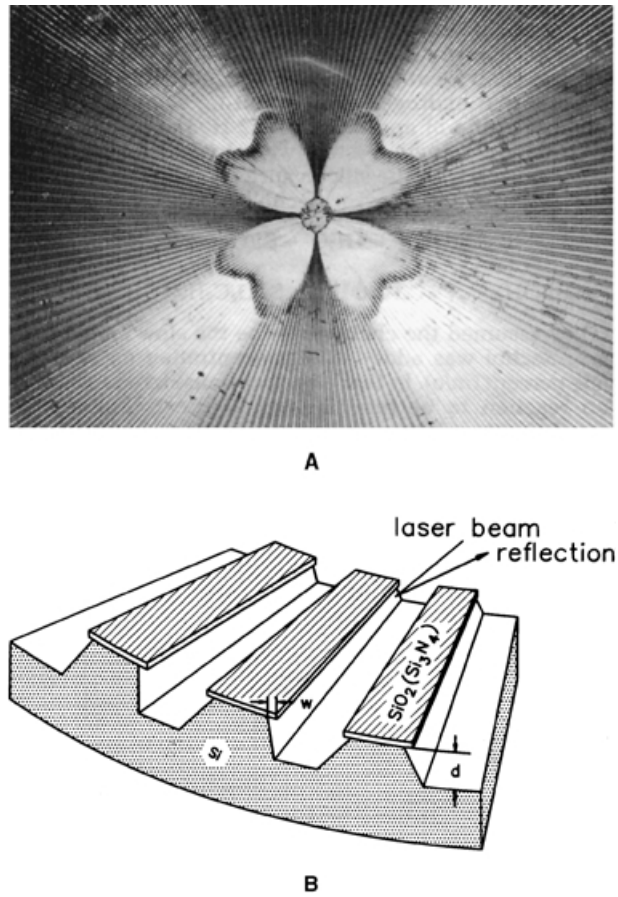


FIGURE 16.35 (A) Etch pattern emerging on a wagon wheel-masked, <100>-oriented Si wafer after etching in an EDP solution. (B) Schematic cross section of a silicon test chip covered with a wagon wheel-shaped masking pattern after etching. The measurement of 'w' is used to construct polar diagrams of lateral underetch rates as shown in Figure 16.36. (From Seidel et al., *J. Electrochem. Soc.*, 177, 3612–3626, 1990. With permission.)

Several chemical models explaining the anisotropy in etching rates for the different Si orientations have been proposed. Presently we will list all of the proposed models and compare the two most recent and most detailed models (the one by Seidel et al. [1990a; 1990b] and the one by Elwenspoek [1993] and Elwenspoek et al. [1994]). Different Si crystal properties have been correlated with the anisotropy in silicon etching.

1. It has been observed that the {111} Si planes present the highest density of atoms per cm^2 to the etchant and that the atoms are oriented such that ***three bonds are below the plane***. It is possible that these bonds become chemically shielded by surface bonded (OH) or oxygen, thereby slowing the etch rate.
2. It also has been suggested that etch rate correlates with available bond density, the surfaces with the highest bond density etching faster [Price, 1973]. The available bond densities in Si and other diamond structures follow the sequence 1:0.71:0.58 for the {100}:{110}:{111} surfaces. However, Kendall (1979) commented that bond density alone is an unlikely explanation because of the magnitude of etching anisotropy (e.g., a factor of 400), compared to the bond density variations of at most a factor of 2.

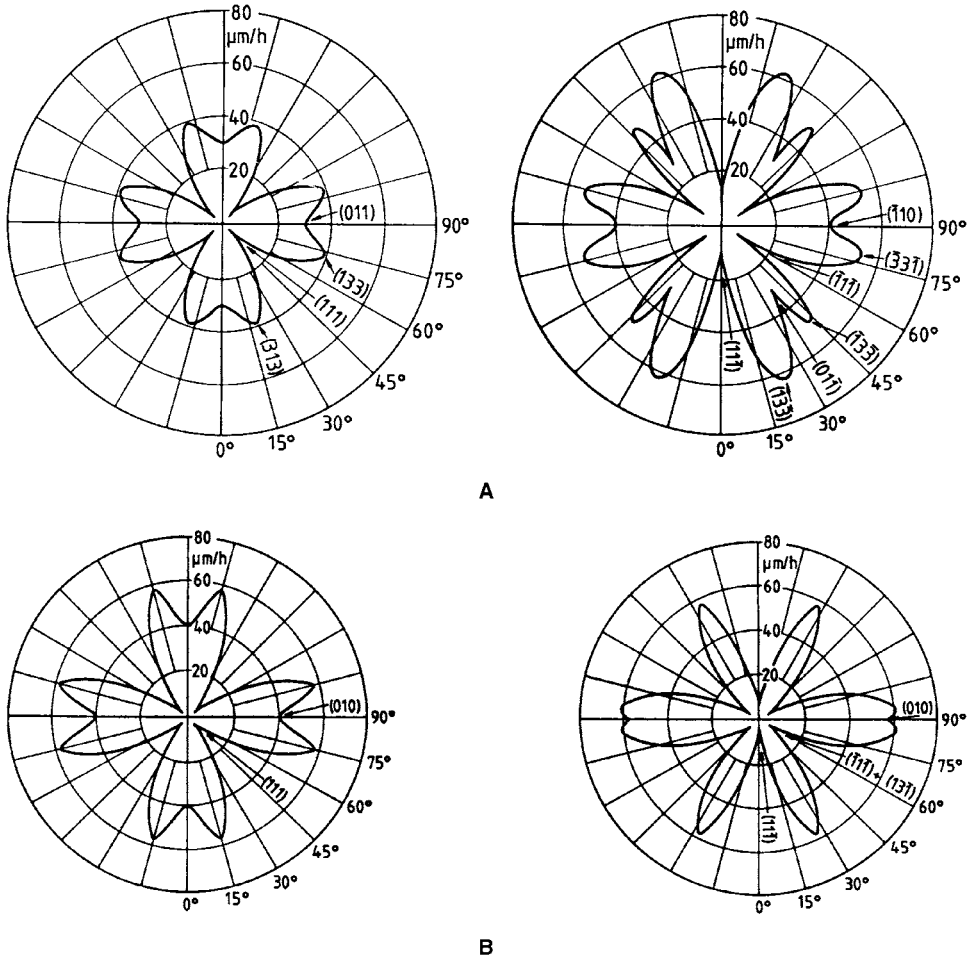
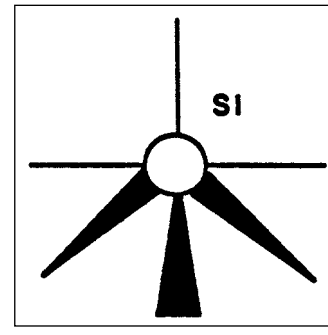


FIGURE 16.36 Lateral underetch rates as a function of orientation for (A) EDP (470 ml water, 1 l ED, 176 g pyrocatechol) at 95°C. (B) KOH (50% solution) at 78°C. Left, <100> - and right, <110>-oriented Si wafers. (From Seidel, H. et al., *J. Electrochem. Soc.,* 137, 3612–3626, 1990. With permission.)



On {111} planes three backbonds are below the plane.

3. Kendall (1979) explains the slow etching of {111} planes on the basis of their faster oxidation during etching; this does not happen on the other faces, due to greater distance of the atoms on planes other than (111). Since they oxidize faster, these planes may be better protected against etching. The oxidation rate in particular follows the sequence {111} > {110} > {100}, and the etch rate often follows the

reverse sequence (see also Madou [1997, chap. 3 on Si oxidation]). In the most used KOH-H_2O, however, the sequence is {110} > {100} > {111}.

4. In yet another model, it is assumed that the anisotropy is due to differences in activation energies and backbond geometries on different Si surfaces [Glembocki et al., 1985].
5. Seidel et al.'s model [Seidel et al., 1990a; 1990b] supports the previous explanation. They detail a process to explain anisotropy based on the difference in energy levels of backbond-associated surface states for different crystal orientations.
6. Finally, Elwenspoek (1993) and Elwenspoek et al. (1994) propose that it is the degree of atomic smoothness of the various surfaces that is responsible for the anisotropy of the etch rates. Basically, this group argues that the kinetics of smooth faces (the (111) plane is atomically flat) is controlled by a nucleation barrier that is absent on rough surfaces. The latter, therefore, would etch faster by orders of magnitude.

The reason why acidic media lead to isotropic etching and alkaline media to anisotropic etching was, until recently, not addressed in any of the models surveyed. In the following we will give our own model as well as Elwenspoek et al.'s to explain isotropic vs. anisotropic etching behavior.

It is our hope that the reading of this section will inspire more detailed electrochemistry work on Si electrodes. The refining of an etching model will be of invaluable help in writing more predictive Si etching software code.

16.5.2.2 Seidel et al.'s Model

Seidel et al.'s model is based on the fluctuating energy level model of the silicon/electrolyte interface and assumes the injection of electrons in the conduction band of Si during the etching process. Consider the situation of a piece of Si immersed in a solution without applied bias at open circuit. After immersion of the silicon crystal into the alkaline electrolyte a negative excess charge builds up on the surface due to the higher original Fermi level of the H_2O/OH^- redox couple as compared to the Fermi level of the solid, i.e., the work function difference is equalized. This leads to a downward bending of the energy bands on the solid surface for both p- and n-type silicon (Figure 16.37A and B). The downward bending is more pronounced for p-type than for n-type due to the initially larger difference of the Fermi levels between the solid and the electrolyte.

Next, hydroxyl ions cause the Si surface to oxidize, consuming water and liberating hydrogen in the process. The detailed steps, based on suggestions by Palik et al. (1985), are:

$$\begin{aligned} &Si + 2OH^- \rightarrow Si(OH)_2^{2+} + 2e^- \\ &Si(OH)_2^{2+} + 2OH^- \rightarrow Si(OH)_4 + 2e^- \\ &Si(OH)_4 + 4e^- + 4H_2O \rightarrow Si(OH)_6^{2-} + 2H_2 \end{aligned} \qquad \text{(Reaction 16.4)}$$

Silicate species were observed by Raman spectroscopy [Palik et al., 1983].

The overall silicon oxidation reaction consumes four electrons first injected into the conduction band, where they stay near the surface due to the downward bending of the energy bands (see Figure 16.37). Evidence for injection of four electrons rather than a mixed hole and electron mechanism was first presented by Raley et al. (1984). The authors could explain the measured etch-rate dependence on hole concentration only by assuming that the proton or water reduction reaction is rate determining and that a four-electron injection mechanism with the conduction band is involved. These injected electrons are highly 'reducing' and react with water to form hydroxide ions and hydrogen:

$$4H_2O + 4e^- \rightarrow 4H_2O^- \qquad \text{(Reaction 16.5)}$$

$$4H_2O^- \rightarrow 4OH^- + 4H^+ + 4e^- \rightarrow 4OH^- + 2H_2 \qquad \text{(Reaction 16.6)}$$

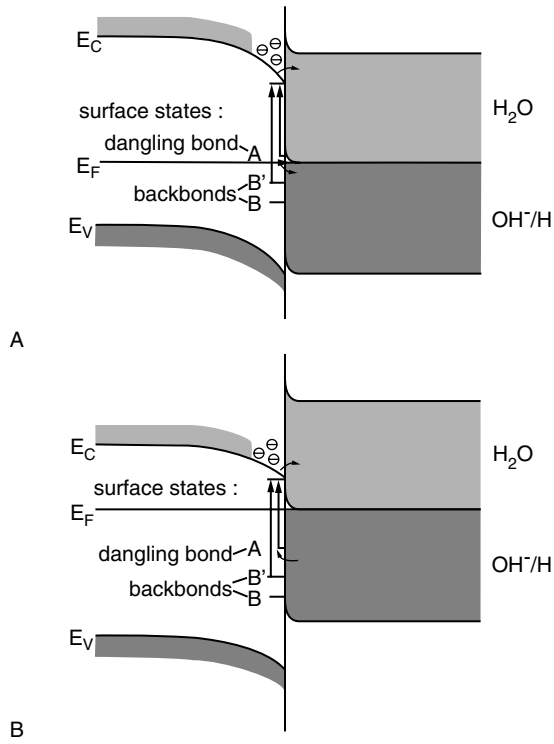
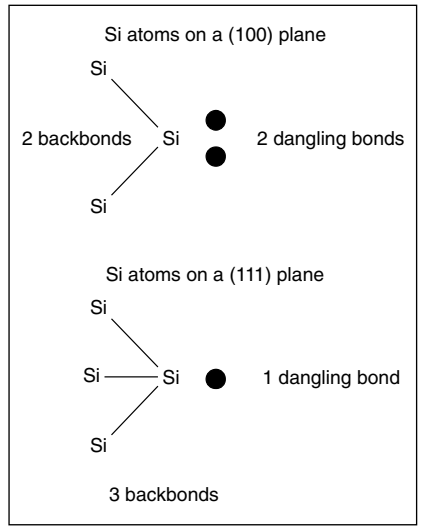


FIGURE 16.37 Band model of the silicon/electrolyte interface for moderately doped Si (electrolyte at pH > 12): (A) p-type Si and (B) n-type Si. We assume no applied bias and no illumination. The energy scale functions in respect to the saturated calomel electrode (SCE), an often-used reference in electrochemistry. Notice that p-type Si exhibits more band bending as its Fermi level is lower in the band gap. For simplicity, we show only one energetic position for surface states associated with dangling bonds and backbonds; in reality, there will be new surface states arising during reactions as the individual dangling bonds and backbonds are taking on different energies as new Si-OH bonds are introduced.

It is thought that the hydroxide ions in Reaction 16.6, generated directly at the silicon surface, react in the oxidation step. The hydroxide ions from the bulk of the solution may not play a major role, as they will be repelled by the negatively charged Si surface, whereas the hydroxide ions formed *in situ* do not need to overcome this repelling force. This would explain why the etch rates for an EDP solution with an OH^- concentration of 0.034 mol/l are nearly as large as those for KOH solutions with a hundred-fold higher OH^- concentration of 5 to 10 mol/l [Seidel et al., 1990]. The hydrogen formed in Reaction 16.6 can inhibit the reaction and surfactants may be added to displace the hydrogen (IBM, U.S. Patent 4,113,551, 1978). Additional support for the involvement of four water molecules (Reaction 16.5) comes from the experimentally observed correlation between the fourth power of the water concentration and the silicon etch rate for highly concentrated KOH solutions (Eq. (16.30) and Figure 16.27C). The weak dependence of the etching curve on the KOH concentration (~1/4 power) supports the assumption that the hydroxide ions involved in the oxidation reactions are mostly generated from water. A strong influence of water on the silicon etch rate was also observed for EDP solutions. In molar water concentrations of up to 60%, a large increase of the etch rate occurs [Finne and Klein, 1967]. The driving force for the overall Reaction 16.4 is given by the larger Si-O binding energy of 193 kcal/mol as compared to a Si-Si binding energy of only 78 kcal/mol. The role of cations, K^+, Na^+, Li^+, and even complicated cations such as $NH_2(CH_2)_2NH_3^+$ can probably be neglected [Seidel et al., 1990].

The four electrons in Reaction 16.5 are injected into the conduction band in two steps. In the case of {100} planes there are two ***dangling bonds*** per surface atom for the first two of the four hydroxide



Dangling bonds.

ions to react with, injecting two electrons into the conduction band in the process. As a consequence of the strong electronegativity of the oxygen atoms, the two bonded hydroxide groups on the silicon atom reduce the strength of the two ***silicon backbonds***. With two new hydroxide ions approaching, two more electrons (now stemming from the Si-Si backbonds) are injected into the conduction band and the silicon-hydroxide complex reacts with the two additional hydroxide ions. Seidel et al. (1990) claim that the step of activating the second two electrons from the backbonds into the conduction band is the rate-limiting step, with an associated thermal activation energy of about 0.6 eV for {100} planes. The electrons in the backbonds are associated with surface states within the bandgap (see Figure 16.37). The energy level of these surface states is assumed to be varying for different surface orientations, being lowest for {111} planes. The thermal activation of the backbonds corresponds to an excitation of the electrons out of these surface states into the conduction band. Since the energy for the backbond surface state level is the lowest within the bandgap for {111} planes, these planes will be hardest to etch. The {111} planes have only one dangling bond for a first hydroxide ion to react with. The second rate-limiting step involves breaking three lower energy backbonds. The lower energy of the backbond surface states for {111} Si atoms can be understood from the simple argument that their energy level is raised less by the electronegativity of a single binding hydroxide ion, compared to two in the case of the silicon atoms in {100} planes. The high etch rate generally observed on {110} surfaces is similarly explained by a high energy level of the backbond-associated surface states for these planes. Elwenspoek (1993) and Elwenspoek et al. (1994) do not accept this 'two vs. three backbonds' argument. They point out that the silicon atoms in the {110} planes also have three backbonds, and activation energy in these crystallographic directions should be comparable to that of {111} planes in contrast to experimental evidence. Seidel et al. would probably counter-argue here that the backbonds and the energy levels of the associated surface states is not necessarily the same for {111} and {110} planes, as that energy will also be influenced by the effect of the orientation of these bonds. Another argument in favor of the high etching rates of {110} planes is the easier penetrability of {110} surfaces for water molecules along channels in that plane.

The final step in the anisotropic etching is the removal of the reaction product $Si(OH)_4$ by diffusion. If the production of $Si(OH)_4$ is too fast, for solutions with a high water concentration, the $Si(OH)_4$ leads to the formation of a SiO_2-like complex before $Si(OH)_4$ can diffuse away. This might be observed experimentally as a white residue on the wafer surface [Wu et al., 1985]. The high pH values in anisotropic etching are required to obtain adequate solubility of the $Si(OH)_4$ reaction product and to remove the

native oxide from the silicon surface. From silicate chemistry it is known that for pH values above 12 the $Si(OH)_4$ complex will undergo the following reaction by the detachment of two protons:

$$Si(OH)_4 \rightarrow SiO_2(OH)_2^{2-} + 2H^+ \qquad \text{(Reaction 16.7)}$$

$$2H^+ + 2OH^- \rightarrow 2H_2O \qquad \text{(Reaction 16.8)}$$

Pyrocathechol in an ethylenediamine etchant acts as complexing agent for reaction products such as $Si(OH)_4$, converting these products into more complex anions:

$$Si(OH)_4 + 2OH^- + 3C_6H_4(OH)_2 \rightarrow Si(C_6H_4O_2)_3^{2-} + 6H_2O \qquad \text{(Reaction 16.9)}$$

There is evidence by Abu-Zeid et al. (1985) of diffusion control contribution to the etch rate in EDP, probably because the hydroxide ion must diffuse through the layer of complex silicon reaction products (see Reaction 16.9). The same authors also found that the etch rate depends on the effective Si area being exposed and on its geometry (crevice effect). That is why the silicon wafer is placed in a holder and the solution is vigorously agitated in order to minimize the diffusion layer thickness. For KOH solutions, no effect of stirring on etching rate was noticed. Stirring here is mainly used to decrease the surface roughness, probably through removal of hydrogen bubbles.

The influence of alcohol on the KOH etching rate in Eq. (16.30) mainly is due to a change in the relative water concentration and its concomitant pH change; it does not participate in the reaction (this was confirmed by Raman studies by Palik et al. [1983]). The reversal of etch rates for {110} and {100} planes through alcohol addition to KOH/water etchants can be understood by assuming that the alcohol covers the silicon surface [Palik et al., 1983], thus canceling the 'channeling advantage' of the {110} planes. In the case of EDP, alcohol has no effect, as the water concentration can be freely adjusted without significantly influencing the pH value due to the incomplete dissociation of EDP.

For the etching of SiO_2 shown in Figure 16.28, Seidel et al. propose the following reaction:

$$SiO_2 + 2OH^- \rightarrow SiO_2(OH)_2^{2-} \qquad \text{(Reaction 16.10)}$$

At KOH concentrations up to 35% a linear correlation occurs between etch rate and KOH concentration. The SiO_2 etch rate in KOH solutions exceeds those in EDP by close to three orders of magnitude. For higher concentrations, the etch rate decreases with the square of the water concentration, indicating that water plays a role in this reaction. Seidel et al. speculate that at high pH values the silicon electrode is highly negatively charged (the point of zero charge of SiO_2 is 2.8), repelling the hydroxide ions while water takes over as reaction partner. An additional reason for the decrease is that the hydroxide concentration does not continue to increase with increasing KOH concentration for very concentrated solutions. The decrease of the Si/SiO_2 etch rate ratio with increasing temperature and pH value of the solution follows out of the larger activation energy of the SiO_2 etch rate (0.85 eV) and its linear correlation with the hydroxide concentration, whereas the silicon etch rate mainly depends on the water concentration.

The effect of water concentration and pH value on the etching process in the Seidel et al. model is summarized in Table 16.10 [Seidel, 1990]. For aqueous KOH solutions within a concentration range from 10 to 60% the following empirical formula for the calculation of the silicon etch rate R proved to be in close agreement with the experimental data:

$$R = k_0[H_2O]^4[KOH]^{\frac{1}{4}} e^{-\frac{E_a}{kT}} \qquad (16.31)$$

The values for the fitting parameters were $E_a = 0.595$ eV and $k_0 = 2480$ µm/hr $(mol/l)^{-4.25}$; for a (100) wafer $E_a = 0.6$ and $k_0 = 4500$ µm/hr $(mol/l)^{-4.25}$. For the SiO_2 etch, an activation energy of 0.85 eV was used.

TABLE 16.10 Effect of Water Concentration and pH Value on the Characteristics of Silicon Etching [Seidel, 1990]

	$-H_2O+$	$-pH+$
SiO_2 etch rate	No effect	$- \Leftrightarrow +$
Si etch rate	$- \Leftrightarrow +$	Little effect
Solubility	No effect	$- \Leftrightarrow +$
Si/SiO_2 ratio	$- \Leftrightarrow +$	$+ \Leftrightarrow -$
Diffusion effects	$- \Leftrightarrow +$	$+ \Leftrightarrow -$
Residue formation	$- \Leftrightarrow +$	$+ \Leftrightarrow -$
p^+ etch stop	$- \Leftrightarrow +$	$+ \Leftrightarrow -$
p, n etch stop	$- \Leftrightarrow +$	$+ \Leftrightarrow -$

In the section on etch stop techniques, we will see that the Seidel et al. model also nicely explains why all alkaline etchants exhibit a strong reduction in etch rate at high boron dopant concentration of the silicon; at high doping levels the conduction band electrons for the rate-determining reduction step are not confined to the surface anymore and the reaction basically stops.

The key points of the Seidel et al. model can be summarized as follows (see also Table 16.10) [Seidel et al., 1990]:

1. The rate-limiting step is the water reduction.
2. Hydroxide ions required for oxidation of the silicon are generated through reduction of water at the silicon surface. The hydroxide ions in the bulk do not contribute to the etching, since they are repelled from the negatively charged surface. This implies that the silicon etch rate will depend on the molar concentration of water and that cations will have little effect on the silicon etch rate.
3. The dissolution of silicon dioxide is assumed to be purely chemical with hydroxide ions. The SiO_2 etch rate depends on the pH of the bulk electrolyte.
4. For boron concentrations in excess of 3×10^{19} cm^{-3}, the silicon becomes degenerate, and the electrons are no longer confined to the surface. This prevents the formation of the hydroxide ions at the surface and thus causes the etching to stop.
5. Anodic biases will prevent the confinement of electrons near the surface as well and lead to etch stop as in the case of a p^+ material.

Points 4 and 5 will become more clear when we discuss the workings of etch-stop techniques. This model applies well for lower index planes (i.e., {nnn} with $n < 2$) where high etch rates always correspond to low activation energies. But, for higher index planes (i.e., {n11} and {1nn} with $n = 2,3,4$), Herr and Baltes (1991) found no correlation between activation energies and etch rates. For higher index planes, we must rely mainly on empirical data.

The Si etching reactions suggested by Seidel et al. are only the latest; in earlier proposed schemes, according to Ghandhi (1968) and Kern (1978), the silicon oxidation reaction steps suggested were injection of holes into the Si (raising the oxidation state of Si), hydroxylation of the oxidized Si species, complexation of the silicon reaction products and dissolution of the reaction products in the etchant solution. In this reaction scheme, etching solutions must provide a source of holes as well as hydroxide ions and they must contain a complexing agent with soluble reacted Si species in the etchant solution, e.g., pyrocathechol forming the soluble $Si(C_6H_4O_2)_3^{2-}$ species. This older model still seems to be guiding the current thinking of many micromachinists, although Seidel et al.'s energy level based model of the silicon/electrolyte interface proves more satisfying.

16.5.2.3 Elwenspoek et al. Model

Elwenspoek (1993) and Elwenspoek et al. (1994) introduced an alternative model for anisotropic etching of Si, a model built on theories derived from crystal growth. According to these authors, the Seidel et al.

model does not clearly explain the fast etching of {110} planes. Those planes, having three backbonds like the {111} planes, should etch equally slowly. The activation energy of the anisotropic etch rate depends on the etching system used; for example, etching in KOH is faster than in EDP, even when the pH of the solution is the same. Seidel et al. attribute this dependence to diffusion that plays a greater role in EDP than in KOH solutions. But Elwenspoek et al. point out that, at least for slow etching, the etch rate should not be diffusion controlled but governed by surface reactions. With surface reactions, diffusion should have a minor effect, analogous to growth at low pressure in an LPCVD reactor [Madou, 1997, chap. 3]. Another comment focuses on the lack of understanding why certain etchants etch isotropically and others etch anisotropically.

Elwenspoek et al. note the parallels in the process of etching and growing of crystals; slowly growing crystal planes also etch slowly! A key to understanding both processes, growing or dissolution (etching), pertains to the concept of the energy associated with the creation of a critical nucleus on a single crystalline smooth surface, i.e., the free energy associated with the creation of an island (growth) or a cavity (etching). Etching or growing of a material starts at active kink sites on steps. Kink sites are atoms with as many bonds to the crystal as to the liquid. Kinetics depend critically on the number of such kink sites. This aspect remained neglected in the discussion of etch rates of single crystals up to now.

The free energy change, ΔG, involved in creating an island or digging a cavity (of circular shape in an isotropic material) of radius r on or in an atomically smooth surface, is given by:

$$\Delta G = -N\Delta\mu + 2\pi r\gamma \tag{16.32}$$

where N is the number of atoms forming the island or the number of atoms removed from the cavity, $\Delta\mu$ is the chemical potential difference between silicon atoms in the solid state and in the solution, and γ is the step free energy. The step free energy in Eq. (16.32) will be different at different crystallographic surfaces. This can easily be understood from the following example. A perfectly flat {111} surface in the Si diamond lattice has no kink positions (three backbonds, one dangling bond per atom), while on the {001} face every atom has two backbonds and two dangling bonds, i.e., every position is a kink position. Consequently, creating an adatom-cavity pair on {111} surfaces costs energy: three bonds must be broken and only one is reformed. In the case of {001} faces, the picture is quite different. Creating an adatom-cavity pair now costs no energy because one has to break two bonds in order to remove an atom from the {001} face, but one gets them back by placing the atom back on the surface. The binding energy ΔE of an atom in a crystal slice with orientation (hkl) divided by kT (Boltzmann constant times absolute temperature) is known as the α factor of Jackson of that crystal face [Jackson, 1966], or:

$$\alpha = \frac{\Delta E}{kT} \tag{16.33}$$

At sufficiently low temperature, where entropy effects can be ignored, $kT\alpha$ is proportional to the step free energy γ and the number of adatom-cavity pairs is proportional to exp $(-\alpha)$. This number is very small on the {111} silicon faces at low temperature, but 1 on the {001} silicon faces at any temperature. The consequence for {111} and {001} planes is that, at sufficiently low temperatures, the first are atomically smooth and the latter are atomically rough. N in Eq. (16.32) can be further written out as:

$$N = \pi r^2 h\rho \tag{16.34}$$

where h is the height of the step, r is the diameter of the hole or island and ρ is the density (atoms per cm^3) of the solid material. The result is

$$\Delta G = -\pi r^2 h\rho\Delta\mu + 2\pi r\gamma \tag{16.35}$$

where $\Delta\mu$ is counted positive and γ is positive in any case. In Figure 16.38 we show a plot of ΔG vs. r. Eq. (16.35) exhibits a maximum at:

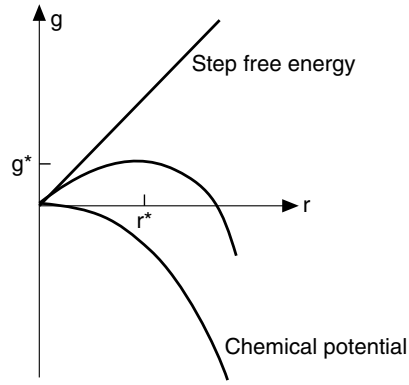


FIGURE 16.38 A plot of ΔG vs. r based on Eq. (16.35) exhibits a maximum.

$$r^* = \frac{\gamma}{h\rho\Delta\mu} \tag{16.36}$$

At r^* the free energy is

$$\Delta G^* = \Delta G(r^*) = \frac{\pi\gamma^2}{h\rho\Delta\mu} \tag{16.37}$$

Consequently, an island or an etch cavity of critical size exist on a smooth face. If by chance a cavity is dug into a crystal plane smaller than r^*, it will be filled rather than allowed to grow and an island that is too small will dissolve rather than continue to grow, since that is the easy way to decrease the free energy. With $r = r^*$, islands or cavities do not have any course of action, but in case of $r > r^*$ the islands or cavities can grow until the whole layer is filled or removed. In light of the above nucleation barrier theory, to remove atoms directly from flat crystal faces such as the {111} Si faces seems very difficult, since the created cavities increase the free energy of the system and filling of adjacent atoms is more probable than removal; in other words, a nucleation barrier has to be overcome. The growth and etch rates, R, of flat faces are proportional to:

$$R \sim \exp\left(-\frac{\Delta G^*}{kT}\right) \tag{16.38}$$

Since ΔG^* is proportional to γ^2, the activation energy is different for different crystallographic faces and both the etch rate and the activation energy are anisotropic. If $\Delta G^*/kT$ is large, the etch rate will be very small, as is the case for large step free energies and for small undersaturation (i.e., the 'chemical drive' or $\Delta\mu$ is small) (see Eq. (16.37)). Both $\Delta\mu$ and γ depend on the temperature and type of etchant and these parameters might provide clues to understanding the variation of etch rate, degree of anisotropy, temperature dependence etc., giving this model more bandwidth than the Seidel et al.'s model. According to Elwenspoek et al., the chemical reaction energy barrier and the transport in the liquid are isotropic and the most prominent anisotropy effect is due to the step free energy (absent on rough surfaces) rather than the surface free energy. The surface free energy and the step free energies are related, though, when comparing flat faces, those having a large surface free energy have a small step free energy, and vice versa. The most important difference in these two parameters is that the step-free energy is zero for a rough surface, whereas the surface energy remains finite.

Flat faces grow and etch with a rate proportional to ΔG^* which predicts that faces with a large free energy to form a step will grow and etch much slower than faces with smaller free energy. Elementary

analysis indicates that the only smooth face of the diamond lattice is the (111) plane. There may be other flat faces, but with lower activation energies, due to reconstruction and/or adsorption, prominent candidates in this category are {100} and {110} planes. On the other hand, a rough crystal face grows and etches with a rate directly proportional to $\Delta\mu$. The temperature at which γ vanishes and a face transitions from smooth to rough is called the roughening transition temperature T_R [Elwenspoek and van der Weerden, 1987; Bennema, 1984]. Above T_R, the crystal is rough on the microscopic scale. Because the step free energy is equal to zero, new Si units may be added or removed freely to the surface without changing the number of steps. Rough crystal faces grow and dissolve with a rate proportional to $\Delta\mu$ and therefore proceed faster than flat surfaces. Imperfect crystals, e.g., surfaces with screw dislocations, etch even faster with R proportional to $\Delta\mu^2$.

For the state of a surface slightly above or below the roughening temperature, T_R, thermal equilibrium conditions apply. Etching, in most practical cases, is far from equilibrium and kinetic roughening might occur. Kinetic roughening [Bennema, 1984] occurs if the super- or undersaturation of the solution is so large that the thermally created islands or cavities are the size of the critical nucleus. One can show that if the super- or undersaturation is larger than $\Delta\mu_c$, given by:

$$\Delta\mu_c = \frac{\pi f_0 \gamma^2}{kT} \tag{16.39}$$

(f_0 being the area one atom occupies in a given crystal plane), the growth and etch mechanism changes from a nucleation barrier-controlled mechanism to a direct growth/etch mechanism. The growth rate and etch rate again become proportional to the chemical potential difference. It can thus be expected that if the undersaturation becomes high enough, even the {111} faces could etch isotropically, as they indeed do in acidic etchants. If the undersaturation becomes so large that $\Delta G^* \ll kT$, the nucleation barrier breaks down. Each single-atom cavity acts as a nucleus made in vast numbers by thermal fluctuations. The face in question etches with a rate comparable to the etch rate of a rough surface. This situation is called kinetic roughening. If all faces are kinetically rough, the etch rate becomes isotropic.

Isotropic etching requires conditions of kinetic roughening, because the etch rate is no longer dominated by a nucleation barrier but by transport processes in solution and the chemical reaction. To test this aspect of the model, Elwenspoek et al. show that there is a transition from isotropic to anisotropic etching if the undersaturation becomes too small. This can occur if one etches with an acidic etchant very long or if one etches through very small holes in a mask (crevice effect). In both cases, anisotropic behavior becomes evident as aging or limited transport of the solution causes the undersaturation to become very small. No proof is available to indicate that acidic etchants are much more undersaturated than the alkaline etchants. Still, the above explains some phenomena that the Seidel et al.'s model fails to address. Another nice confirmation of the Elwenspoek et al. model is in the effect of misalignment on etch rate. A misalignment of the mask close to smooth faces implies steps; there is no need for nucleation in order to etch. Since the density of steps is proportional to the angle of misalignment, the etch rate should be proportional to the misalignment angle, provided the distance between steps is not too large. Nucleation of new cavities becomes very probable. This has indeed been observed for the etch rate close to the <111> directions [Seidel et al., 1990].

Where the Elwenspoek et al.'s model becomes a bit murky is in the classification of which surfaces are smooth and which ones are rough. Elementary analysis classifies only the {111} planes as smooth at low temperatures. At this stage the model does not explain anything more than other models; every model has an explanation for the slower {111} etch rate. But these authors invoke the possibility of surface reconstruction and/or adsorption of surface species which, by decreasing the surface-free energy, could make faces such as {001} and {110} flat as well but with lower activation energies. They also take heart in the fact that CVD experiments often end up showing flat {110}, {100}, {331} and, strongest of all, {111} planes. Especially where the influence of the etchant is concerned a lot more convincing thermodynamic data to estimate $\Delta\mu$ and γ are needed.

16.5.2.4 Isotropic vs. Anisotropic Etching of Silicon

In contrast to alkaline etching, with an acidic etchant such as HF, holes are needed for etching Si. An n-type Si electrode immersed in HF in the dark will not etch due to lack of holes. The same electrode in an alkaline medium etches readily. A p-type electrode in an HF solution, where holes are available under the proper bias, will etch even in the dark. For HF etchants one might assume that the Ghandi and Kern model [Kern, 1978; Jackson, 1966], relying on the injection of holes, applies. In terms of the band model, this must mean that the silicon/electrolyte interface in acidic solutions exhibits quite different energetics from the alkaline case. It is not directly obvious why the energetics of the silicon/electrolyte interface would be pH dependent. To the contrary, since the flatband potential of most oxide semiconductors as well as most oxide-covered semiconductors (such as Si) and the Fermi level of the H_2O/OH^- redox couple in an aqueous solution are both expected to change by 59 mV for each pH unit change [Madou and Morrison, 1989], one would expect the energetics of the interface to be pH independent. Since the electronegativity in a Si-F bond is higher than for a Si-OH bond, one might even expect the backbond surface states to be raised higher in an HF medium, making an electron injection mechanism even more likely than in alkaline media. To clarify this contradiction we will analyze the band model of a Si electrode in an acidic medium in more detail. The band model shown in Figure 16.39 was constructed on the basis of a set of impedance measurements on an n-type Si electrode in a set of aqueous solutions at different pH values. From the impedance measurements Mott-Schottky plots were constructed to determine the pH dependency of the flat-band potential. From that, the position of the conduction band and valence band edges (E_{cs} and E_{vs}, respectively) of the Si electrode in an acidic medium at a fixed pH of 2.2 (the point of zero charge) was calculated at 0.74 eV vs. SCE (saturated calomel electrode as reference) for E_{cs}, and –0.36 eV vs. SCE for E_{vs} [Madou et al., 1980; 1981].

We have assumed in Figure 16.39 that the bands are bent upwards at open circuit (see below for justification), so that holes in the valence band are driven to the interface where they can react with Si atoms or with competing reducing agents from the electrolyte. Since we want to etch Si, we are only interested in the reactions where Si itself is consumed. Reactions of holes with reducing agents are of great importance in photoelectrochemical solar cells [Madou et al., 1981]. For n-type Si, holes can be (1) injected by oxidants from the solution (e.g., by adding nitric acid to the HF solution), (2) supplied at the electrolyte/semiconductor interface by shining light on a properly biased n-Si wafer, or (3) created by impact ionization, i.e., Zener breakdown, of a sufficiently high reverse biased n-Si electrode [Levy-Clement et al., 1992]. With a p-Si wafer, a small forward bias supplies all the holes needed for the oxidation of the lattice even without light, as the conduction happens via a hole mechanism. An important

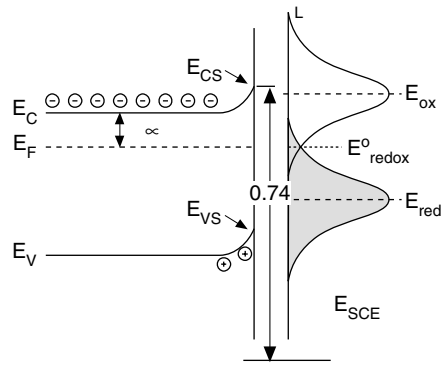


FIGURE 16.39 Band diagram for n-type Si in pH = 2.2 (no bias or illumination). Reference is the saturated calomel electrode (SCE). In Figure 16.37 no energy values were given; here we provide actual positions of the conduction band edge, E_{cs} = 0.74 eV vs. SCE, and the valence band edge, E_{vs} = 0.74 eV –1.1 eV = –0.36 eV vs. SCE (1.1 eV is the band gap of Si). These values were determined by means of Mott-Schottky plots [Madou et al., 1981]. The separation between the Fermi energy and the bottom of the conduction band is indicated by μ.

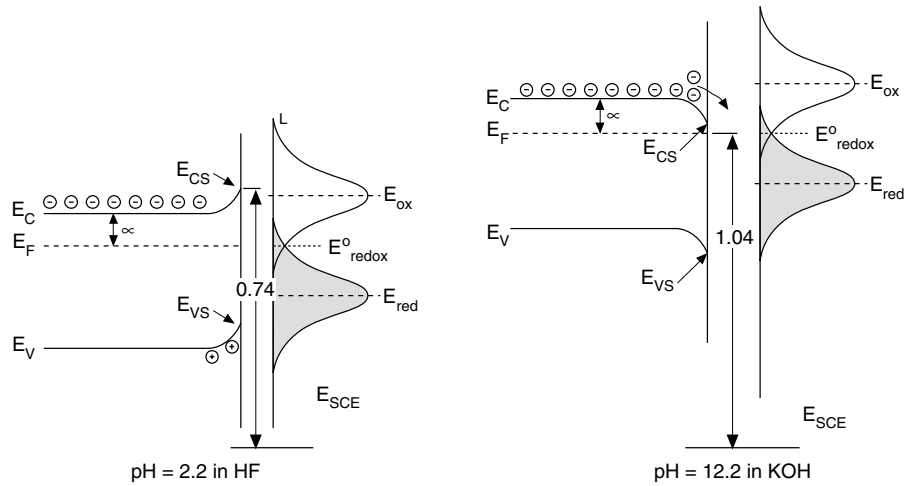


FIGURE 16.40 Band model comparison of the Si/electrolyte interface at low and high pH. Increasing the pH by 10 units shifts the redox-levels up by 600 mV, whereas the Si bands only move up by 300 mV. This leads to a different band-bending and a different reaction mechanism, i.e., electron injection in the alkaline media (anisotropic) and hole injection in acidic media (isotropic).

finding, explaining the different reaction paths in acidic and alkaline media comes from plotting the flat band potential as a function of pH. It was found that the band diagram of Si shifts with less than 59 mV per pH unit. Actually the shift is only about 30 mV per pH unit [Madou et al., 1981]. As shown in Figure 16.40, with increasing pH, the energy levels of the solution rise faster than the energy levels in the semiconductor. As a consequence it is more likely that electron injection takes place in alkaline media as the filled levels associated with the OH^- are closer to the conduction band, whereas in acidic media the filled levels of the redox system overlap better with the valence band, favoring a hole reaction. A lower position of the redox couple with respect to the conduction band edge, E_{cs}, in acidic media explains the upward bending of the bands as drawn in Figure 16.39. With isotropic etching in acidic media, the reaction starts with a hole in the valence band, equivalent to a broken Si-Si bond. In this case, the relative position of backbond related surface states in different crystal orientations are of no consequence and all planes etch at the same rate. A study of the interfacial energetics helps to understand why isotropic etching occurs in acidic media and anisotropic etching in alkaline media.

A few words of caution on our explanation for the reactivity difference between acidic and alkaline media are in order. Little is known about the width of the bell-shaped curves describing the redox levels in solution [Madou and Morrison, 1989]. Not knowing the surface concentrations of the reactive redox species involved in the etching reactions further hinders a better understanding of the surface energetics as the bell-shaped curves for oxidant and reductant will only be the same height (as they were drawn in Figures 16.39 and 16.40) if the concentration of oxidant and reductant are the same. Clearly, the above picture is oversimplified; several authors have found that the dissolution of Si in HF might involve both the conduction and valence band, a claim confirmed by photocurrent multiplication experiments [Matsumura and Morrison, 1983; Lewerenz et al., 1988]. These photomultiplication experiments showed that one or two holes generated by light in the Si valence band were sufficient to dislodge one Si [Brantley, 1973] unit, meaning that the rest of the charges were injected into the conduction band. Our contention here is only that the low pH dependence of the flat-band potential of a silicon electrode makes a conduction band mechanism more favorable with alkaline type etchants and a hole mechanism more favorable in acidic media.

Continued attempts at modeling the etch rates of all Si planes are under way. For example, Hesketh et al. (1993) attempted to model the etch rates of the different planes developing on silicon spheres in

etching experiments with KOH and CsOH by calculating the surface free energy. The number of surface bonds per centimeter square on a Si plane is indicative of the surface free energy, which can be estimated by counting the bond density and multiplying by the bond energy. Using the unit cell dimension "a" of Si of 5.431 Å, and a silicon-to-silicon bond energy of 42.2 kcal/mol, the surface free energy, ΔG, can be related to, N_B, the bond density, by the following expression:

$$\Delta G = \frac{N_B}{2} \times 2.94 \times 10^{-19} \frac{J}{m^2} \tag{16.40}$$

Although Hesketh et al. could not explain the etching differences observed between CsOH and KOH (these authors identified a cation effect on the etch rate!), a plot of the calculated surface free energy vs. orientation yielded minima for all low index planes such as {100}, {110} and {111}, as well as for the high index {522} planes. Fewer bonds per unit area on the low index planes produce a lower surface energy and lower etching rate. When Hesketh et al. added the in-plane bond density to the surface bond density, producing a total bond density, a correlation with the hierarchy of etch rates in CsOH and KOH was found, i.e., {311}, {522} > {100} > {111}. The surfaces with the higher bond density etched faster, suggesting that the etch rate might be a function of the number of electrons available at the surface. Hesketh et al. imply that their result falls in line with the Seidel et al.'s model, although it is unclear how the total bond density relates to surface state energies of backbonds. Moreover, Hesketh's model does not take into account the angles of the bonds, and in Elwenspoek's view, the surface free energy actually does not determine the anisotropy.

More research could focus on the modeling of Si etch rates. The semiconductor electrochemistry of corroding Si electrodes will be a major tool in further developments. Interested readers may consult Sundaram and Chang (1993) in an article on Si etching in hydrazine and Palik et al. (1985) on the etch-stop mechanism in heavily doped silicon; both explain in some detail the silicon/electrolyte energetics. A more generic treatise on semiconductor electrochemistry can be found in Morrison (1980).

16.6 Etching With Bias and/or Illumination of the Semiconductor

The isotropic and anisotropic etchants discussed so far require neither a bias nor illumination of the semiconductor. The etching in such cases proceeds at open circuit and the semiconductor is shielded from light. In a cyclic voltammogram, as shown in Figure 16.41, the operational potential is the rest potential, *Vr*, where anodic and cathodic currents are equal in magnitude and opposite in sign, resulting in the absence of flow of current in an external circuit. This does not mean that macroscopic changes do not occur at the electrode surface, since the anodic and cathodic currents may be part of different chemical reactions. Consider isotropic etching of Si in an HF/HNO_3 etchant at open circuit where the local anodic reaction is associated with corrosion of the semiconductor:

$$\text{Anode: } Si + 2H_2O + nh^+ \rightarrow SiO_2 + 4H^+ + (4 - n)e^- \qquad \text{(Reaction 16.11)}$$

$$SiO_2 + 6HF \rightarrow H_2SiF_6 + 2H_2O \qquad \text{(Reaction 16.12)}$$

(the involvement of holes 'h^+' in the acidic reaction was discussed in the preceding section), while the local cathodic reaction could be associated with reduction of HNO_3:

$$\text{Cathode: } HNO_3 + 3H^+ \rightarrow NO + H_2O + 3H^+ \qquad \text{(Reaction (16.13)}$$

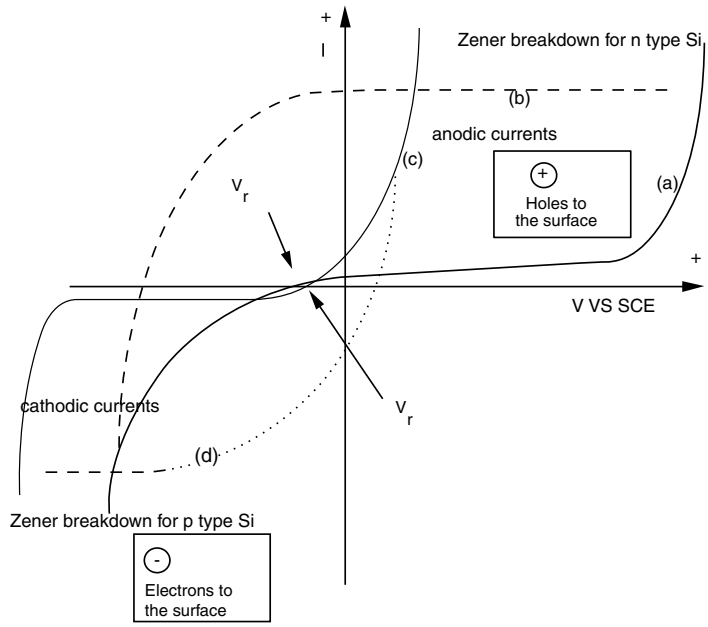


FIGURE 16.41 Basic cyclic voltammograms (I vs. V) for n- and p-type Si in an HF solution, in the absence of a hole injecting oxidant: (a) n-type Si without illumination; (b) n-type Si under illumination; (c) p-type Si without illumination; (d) p-type Si under illumination. If the reactions on the dark Si electrode determining the rest potential V_r for n- and p-type are the same, then V_r is expected to be the same as well. For the clarity of the figure we have chosen the V_rs different here; in practice, V_r for n- and p-type Si in HF are found to be identical.

We will now explore Si etching while illuminating and/or applying a bias to the silicon sample. To simplify the situation, we will first consider the case of an oxidant-free solution so that all the holes must come from within the semiconductor. Anodic dissolution of n-Si in an HF containing solution requires a supply of holes to the surface. For an n-type wafer under reverse bias, very few holes will show at the surface unless the high reverse (anodic) bias is sufficient to induce impact ionization or Zener breakdown (see Figure 16.41a). Alternatively, the interface can be illuminated, creating holes in the space charge region which the field pushes towards the semiconductor/electrolyte interface (Figure 16.41b). In the forward direction, electrons from the Si conduction band (majority carriers) reduce oxidizing species in the solution (e.g., reduction of protons to hydrogen). A p-type Si sample exhibits high anodic currents even without illumination at small anodic (forward) bias (Figure 16.41c). Here the current is carried by holes. A p-type electrode illuminated under reverse bias gives rise to a cathodic photocurrent (Figure 16.41d). At relatively low light intensities, the photocurrent plateaus for both n- and p-types (Figures 16.41b and 16.41d, respectively) depend linearly on light intensity. The photocurrent is cathodic for p-type Si (species are reduced by photoproduced electrons at the surface, e.g., hydrogen formation) and anodic for n-type Si (species are oxidized by photoproduced holes at the surface; either the lattice itself is consumed or reducing compounds in solution are). In Figure 16.42 we show the cyclic voltammograms of n-type and p-type Si in the presence of a hole-injecting oxidant. The most obvious effect is on the dark p-type Si electrode. The injection of holes in the valence band increases the cathodic dark current dramatically. The current level measured in this manner for varying oxidant concentration or different oxidants could be used to estimate the efficiency of different isotropic Si etchants; a pointer to the fact that semiconductor electrochemistry has been underutilized as a tool to study Si etching. When n-type Si is consumed under illumination, we experience photocorrosion (see Figure 16.41b). This photocorrosion phenomenon has been a major barrier to the long-term viability of photoelectrochemical cells [Madou et al., 1980]. In what follows, photocorrosion is put to use for electropolishing and formation of microporous and macroporous layers [Levy-Clement et al., 1992].

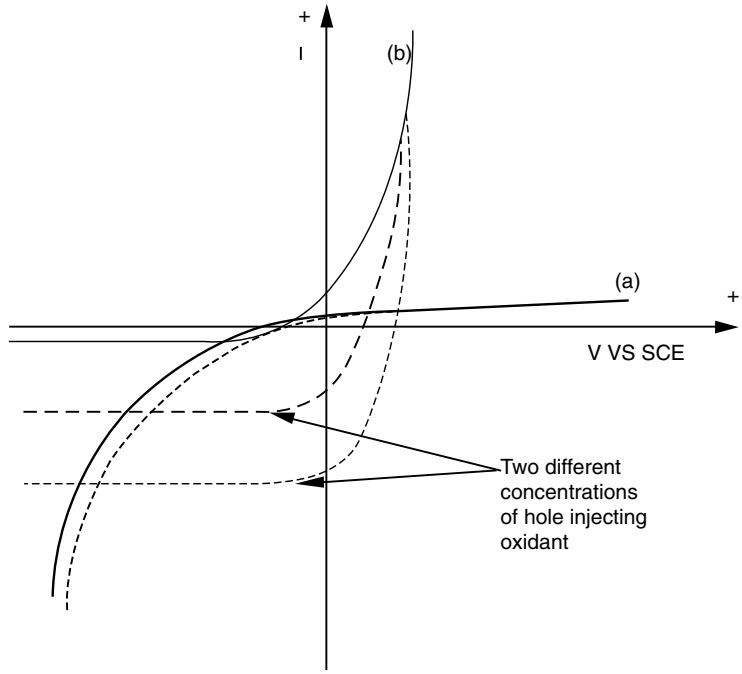


FIGURE 16.42 Basic cyclic voltammograms for n- and p-type Si in an HF solution and in the presence of a hole injecting oxidant, e.g., HNO_3: (a) n-type Si in the dark; (b) p-type Si in the dark. An increase of the cathodic dark current on the p-type electrodes is most obvious. The current level is proportional to the oxidant concentration.

16.6.1 Electropolishing and Microporous Silicon

16.6.1.1 Electropolishing

Photoelectrochemical etching (PEC-etching) involves photocorrosion in an electrolyte in which the semiconductor is generally chemically stable in the dark, i.e., no hole-injecting oxidants are present, as in the case of an HF solution (see Figure 16.41). For carrying out the experiments a set-up as shown in Figure 16.25 may be used with a provision to illuminate the semiconductor electrode. At high light intensities the anodic curves for n- and p-type Si are the same, except for a potential shift of a few hundred mV (see Figure 16.43). Because of this equivalence, several of the etching processes described apply for both forward biased p-type and n-type Si under illumination. The anodic curves in Figure 16.43 present two peaks, characterized by i_{CRIT} and i_{MAX}. At the first peak, i_{CRIT}, partial dissolution of Si in reactions such as:

$$Si + 2F^- + 2h^+ \rightarrow SiF_2 \qquad \text{(Reaction 16.14)}$$

$$SiF_2 + 2HF \rightarrow SiF_4 + H_2 \qquad \text{(Reaction 16.15)}$$

leads to the formation of porous Si while hydrogen formation occurs simultaneously. The porous Si typically forms when using low current densities in a highly concentrated HF solution—in other words, by limiting the oxidation of silicon due to a hole and OH^- deficiency. Above i_{CRIT}, the transition from the charge-supply-limited to the mass-transport-limited case, the porous film delaminates and bright electropolishing occurs at potentials positive of i_{MAX}. With dissolution of chemical reactants in the electrolyte rate limiting, HF is depleted at the electrode surface and a charge of holes builds up at the interface. Hills on the surface dissolve faster than depressions because the current density is higher on high spots. As a result, the surface becomes smoother, i.e., electropolishing takes place [Lehmann, 1993].

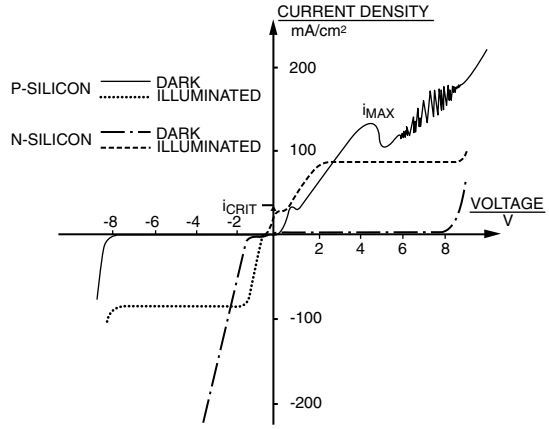


FIGURE 16.43 Cyclic voltammograms identifying porous Si formation regime and electropolishing regime. (From Levy-Clement, C. et al., *Electrochima Acta*, 37, 877–888, 1992. With permission.)

Electropolishing in this regime can be used to smooth silicon surfaces or to thin epitaxially grown silicon layers. The peak and oscillations in Figure 16.43 are explained as follows: at current densities exceeding i_{MAX} an oxide grows first on top of the silicon, leading to a decrease of the anodic photocurrent (explaining the i_{MAX} peak), until a steady state is reached in which dissolution of the oxide by HF through formation of a fluoride complex in solution (SiF_6^{2-}) equals the oxide growth rate. The oscillations observed in the anodic curve in Figure 16.43 can be explained by a nonlinear correlation between formation and dissolution of the oxide [Levy-Clement et al., 1992].

16.6.1.2 Porous Silicon

Introduction

The formation of porous Si was first discovered by Uhlir in 1956 [Uhlir, 1956]. His discovery is leading to all types of interesting new devices from quantum structures, permeable membranes, photoluminescent and electroluminescent devices to a basis for making thick SiO_2 and Si_3N_4 films [Bomchil et al., 1986; Smith and Collins, 1990]. Two types of pores exist: micropores and macropores. Their sizes can differ by three orders of magnitude and the underlying formation mechanism is quite different. Some important features of porous Si, as detailed later, are

- Pore sizes in a diameter range from 20 Å to 10 μm.
- Pores that follow crystallographic orientation [Chuang and Smith, 1988].
- Very high aspect ratio (~250) pores in Si maintained over several millimeters' distance [Lehmann, 1993].
- Porous Si is highly reactive, oxidizes and etches at very high rate.
- Porosity varies with the current density.

These important attributes contribute to the essential role porous Si plays in both micromachining [Barret et al., 1992] and the fashioning of quantum structures [Canham, 1990].

Microporous Silicon

Whether one is in the regime of electropolishing or porous silicon formation depends on both the anodic current density and the HF concentration. The surface morphology produced by the Si dissolution process critically depends on whether mass transport or hole supply is the rate-limiting step. Porous silicon formation is favored for high HF concentrations and low currents (weak light intensities for n-type Si), where the charge supply is limiting, while etching is favored for low HF concentration and high currents

(strong light intensity for n-type Si), where mass transport is limiting. For current densities below i_{MAX} (Figure 16.43) holes are depleted at the surface and HF accumulates at the electrode/electrolyte interface. As a result, a dense network of fine holes forms [Unagami, 1980; Watanabe et al., 1975]. The formation of a porous silicon layer (PSL) in this regime has been explained as a self-adjusting electrochemical reaction due to hole depletion by a quantum confinement in the microporous structure [Lehmann and Gosele, 1991]. The structure of the pores in PSL can best be observed by transmission electron microscopy (TEM) and its thickness can be monitored with an IR microscope. The structure of the porous layer primarily depends on the doping level of the wafer and on the illumination during etching. The pore sizes decrease when etching occurs under illumination [Levy-Clement et al., 1992]. The pores formed in p-type Si show much smaller diameters than n-type ones for the same formation conditions. It is believed that the porous silicon layer (PSL) consists of silicon hydrides and oxides. The pore diameter typically ranges from 40 to 200 Å [Lehmann, 1996; Yamana et al., 1990; Arita and Sunohara, 1977]. This very reactive porous material etches or oxidizes rapidly. Heat treatment in an oxidizing atmosphere (1100°C in oxygen for 30 minutes is sufficient to make a 4-μm thick film) leads to oxidized porous silicon (OPS). The oxidation occurs throughout the whole porous volume and several micrometers-thick SiO_2 layers can be obtained in times that correspond to the growth of a few hundred nanometers on regular Si surfaces. Porous silicon is low density and remains single crystalline, providing a suitable substrate for epitaxial Si film growth. These properties have been used to obtain dielectric isolation in ICs and to make silicon-on-insulator wafers [Watanabe et al., 1975].

Porous Si can also be formed chemically through Reactions 16.11 and 16.13. In this case the difference between chemical polishing and porous Si formation conditions is more subtle. In the chemical polishing case, all reacting surface sites switch constantly from being local anode (Reaction 16.11) to being local cathode (Reaction 16.13), resulting in nonpreferential etching. If surface sites do not switch fast between being local anode and cathode, charges have time to migrate over the surface. In this case, the original local cathode site remains a cathode for a longer time, and the corresponding local anode site, somewhere else on the surface, also remains an anode in order to keep the overall reaction neutral. A preferential etching results at the localized anode sites, making the surface rough and causing a porous silicon to form [Jung et al., 1993]. Any inhomogeneity, e.g., some oxide or a kink site at the surface might increase such preferential etching [Jung et al., 1993]. Unlike PSLs fabricated by electrochemical means, the chemically etched porous Si film thickness is self limiting.

Besides its use for dielectric isolation and the fabrication of SOI wafers, porous silicon has been introduced in a wide variety of other applications: Luggin capillaries for electrochemical reference electrodes, high surface area gas sensors, humidity sensors, sacrificial layers in silicon micromachining, etc. Recently PSL was shown to exhibit photoluminescent and electroluminescent behavior; light-emitting porous silicon (LEPOS) was demonstrated. Visible light emission from regular Si is very weak due to its indirect bandgap. Pumping porous Si with a green light laser (argon) caused it to emit a red glow. If a LEPOS device could be integrated monolithically with other structures on silicon, a big step in micro-optics, photon data transmission, and processing would be achieved. To explain the blue shift of the absorption edge of LEPOS of about 0.5 eV compared to bulk silicon [Lehmann and Gosele, 1991] and room temperature photoluminescence [Canham, 1990], Searson et al. (1993) have proposed an energy-level diagram for porous silicon where the valence band is lowered with res˙pect to bulk silicon to give a band-gap of about 1.8 eV. Not only may PSL formation, as seen above, be explained invoking quantum structures, but its remarkable optical properties may also be explained this way. Canham believes that the thin Si filaments may act as quantum wires. Significant quantum effects require structural sizes below 5 nm (see Madou [1997, chap. 7]) and the porous Si definitely can have structures of that size. By treatment of the porous Si with NH_3 at high temperatures, it is possible to make thick Si_3N_4 films. Even at 13 μm, these films show little evidence of stress in contrast to stoichiometric LPCVD nitride films [Smith and Collins, 1990].

Porous Si might represent a simple way of making the quantum structures of the future. Pore size of PSL can be influenced by both light intensity and current density. The quantum aspect adds significantly to the sudden big interest taken in porous Si.

Macroporous Silicon

In addition to micropores, well-defined macropores can also be made in Si by photo and/or bias etching in HF solutions. Macropores have sizes as large as 10 μm, visible with a scanning electron microscope (SEM) rather than TEM. The two types of pores often coexist, with micropores covering the walls of macropores. Sizes can differ by three orders of magnitude. This is not a matter of a broad fractal type distribution of pores, but the formation mechanism is quite different.

Electrochemical etching of macropores or macroholes has been reported for n-type silicon in 2.5 to 5% HF under high voltage (>10 V), low current density (10 $mAcm^{-2}$), under illumination, and in the dark [Levy-Clement et al., 1992]. In the latter case, Zener breakdown in silicon (electric field strength in excess of 3×10^5V/cm) causes the hole formation. The macropores are formed only with lightly doped n-silicon at much higher anodic potentials than those used for micropore formation [Zhang, 1991]. By using a pore initiation pattern the macropores actually can be localized at any desired location. This dramatic effect is illustrated by comparing Figures 16.44A and B [Lehmann, 1993; 1996]. Pores orthogonal to the surface with depths up to a whole wafer thickness can be made and aspect ratios as large as 250 become possible. The formation mechanism in this case cannot be explained on the basis of depletion of holes due to quantum confinement in the fine porous structures, given that these macropores exhibit sizes well beyond 5 nm. As with microporous Si, the surface morphology produced by the dissolution process depends critically on whether mass transport or charge supply is the rate-limiting step. For pore

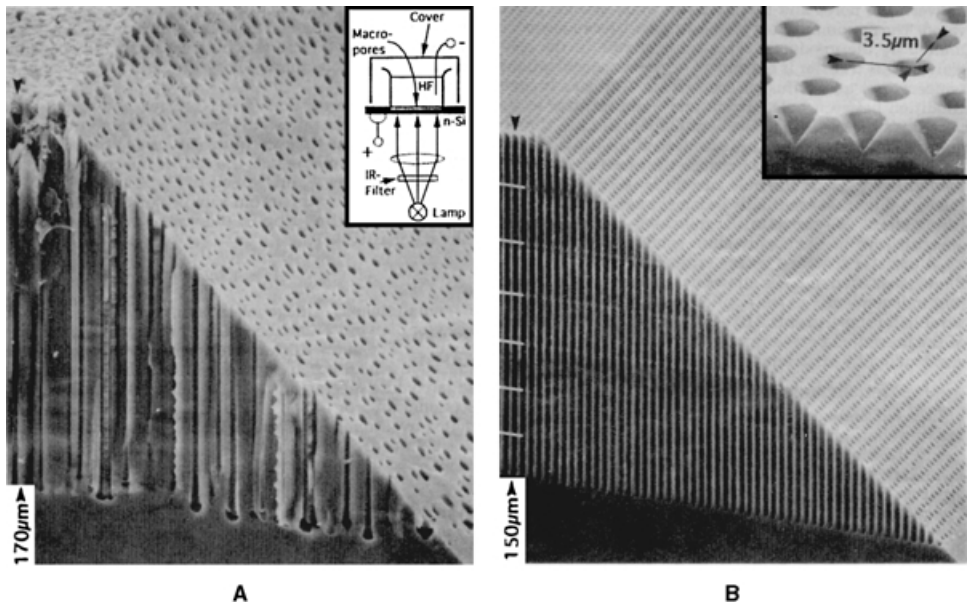


FIGURE 16.44 Macroporous Si; formation of random and localized macropores or macroholes. (A) Random: surface, cross section and a 45° bevel of an n-type sample ($10^{15}/cm^3$ phosphorus-doped) showing a random pattern of macropores. Pore initiation was enhanced by applying 10-V bias in the first minute of anodization followed by 149 min at 3 V. The current density was kept constant at 10 mA/cm^2 by adjusting the backside illumination. A 6% aqueous solution of HF was used as an electrolyte. The set-up used for anodization is sketched in the upper right corner. (B) Localized: surface, cross section and a 45° bevel of an n-type sample ($10^{15}/cm^3$ phosphorus-doped) showing a predetermined pattern of macropores (3 V, 350 min, 2.5% HF). Pore growth was induced by a regular pattern of pits produced by standard lithography and subsequent alkaline etching (inset upper right). To measure the depth dependence of the growth rate, the current density was kept periodically at 5 mA/cm^2 for 45 min and then reduced to 3.3 mA/cm^2 for 5 min. This reduction resulted in a periodic decrease of the pore diameter, as marked by white labels in the figure. (From Lehmann, V., *J. Electrochem. Soc.,* 140, 2836–2843, 1993. With permission.)

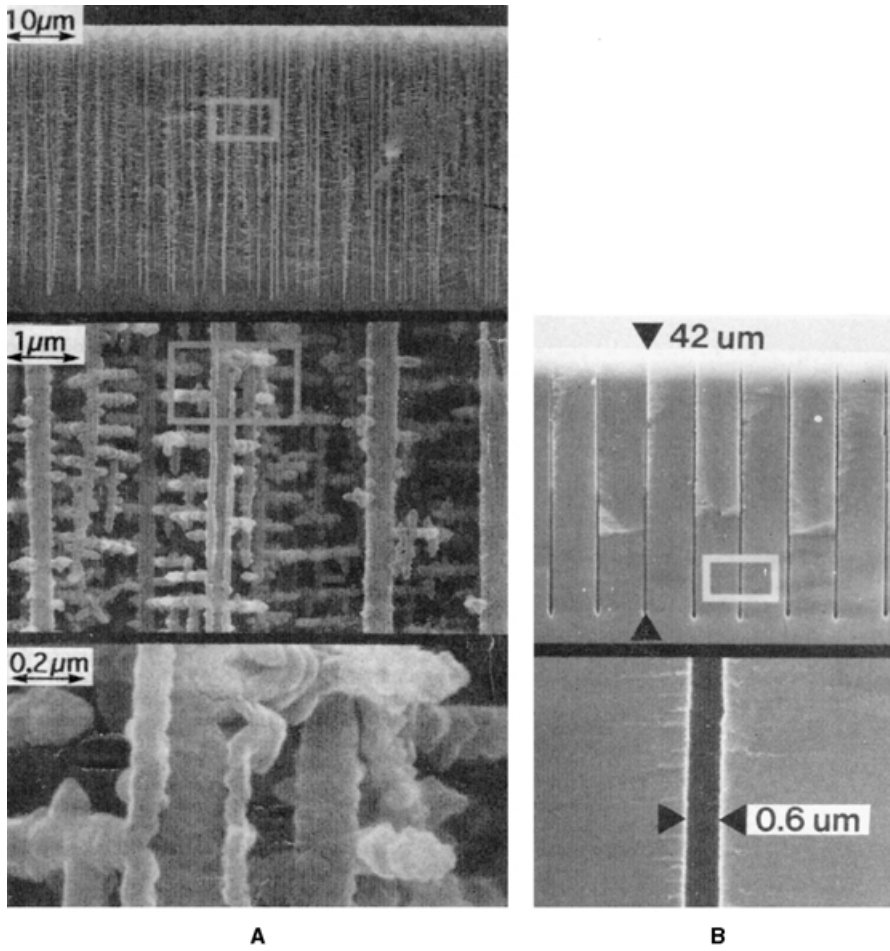


FIGURE 16.45 Comparison of macropores made with breakdown holes (A) and macropores made with light created holes (B). (A) An oxide replica of pores etched under weak backside illumination visualizes the branching of pores produced by generation of charge carriers due to electrical breakdown (5 V, 3% HF, room temperature, $10^{15}/cm^3$ phosphorus-doped). (From Lehmann, V., *J. Electrochem. Soc.*, 140, 2836–2844, 1993. With permission.) (B) Single pore associated with KOH pit. (From Lehmann, V. and H. Foll, *J. Electrochem. Soc.,* 137, 653–659, 1990. With permission.)

formation one must work again in a charge depletion mode. Macropore formation, as micropore formation, is a self-adjusting electrochemical mechanism. In this case, the limitation is due to the depletion of the holes in the pore walls in n-Si wafers causing them to passivate. Holes keep on being collected by the pore tip where they promote dissolution. No passivating layer is involved to protect the pore wall. The only decisive differences between pore tips and pore walls are their geometry and their location. Holes generated by light or Zener breakdown are collected at pore tips. Every depression or pit in the surface initiates pore growth because the electrical field at a curved pore bottom is much larger than that of a flat surface due to the effect of the radius of curvature. The latter leads to higher current and enhances local etching [Zhang, 1991]. Zener breakdown and illumination of n-Si lead to different types of pore geometry [Lehmann, 1993; Theunissen, 1972; Lehmann and Foll, 1990]. Branched pores with sharp tips form if holes are generated by breakdown (see Figure 16.45A) [Lehmann, 1993]. Unbranched pores with larger tip radii result from holes created by illumination (see Figure 16.45B) [Lehmann and Foll, 1990]. The latter difference can be understood as follows: the electric field strength is a function of bias, doping

density and geometry. High doping level density or sharp pore tips will lower the required bias for breakdown, so macropores will tend to follow pores with the sharpest tips. Since every tip causes a new breakdown and hole generation, the position of the original pore tip becomes independent of the other pores, branching of the pores is possible, and fir-tree type pores can be observed. With illumination the pore radius may be larger as the breakdown field strength is not necessary to generate charge carriers, so the pores remain unbranched.

The Si anisotropy common with alkaline etchants surprisingly shows up here with an isotropic etchant such as HF. For example, with breakdown-supplied holes, <100>-directed macroholes with <110> branches form (see also Figure 16.45A) [Lehmann, 1993], leading to a complex network of caverns beneath the silicon surface. Pyramidal pore tips [Lehmann, 1993] also were observed when the current density was limited by the bias ($i < i_{CRIT}$). Isotropic pore pits form when the current is larger than the critical current density, i.e., isotropy in HF etching can be changed into anisotropy when the supply of holes is limited. We refer here to the Elwenspoek et al. model (see above) which predicts that in confined spaces etching will tend to be more anisotropic, even when using a normally isotropic etchant such as HF. It was also determined that macrohole formation depends on the wavelength of the light used. No hole formation occurs below about 800 nm. Depending on the wavelength, the shape of the hole can be manipulated as well [Lehmann and Foll, 1990]. For wavelengths above 867 nm, the depth profile of the holes changed from conical to cylindrical. The latter was interpreted in terms of the influence of the local minority carrier generation rate. Carriers generated deep in the bulk would promote the hole growth at the tips, whereas near-surface generation would lead to lateral growth.

Cahill et al. (1993) reported in 1993 the creation of 1- to 5-μm-size pores with pore spacings (center-to-center) from 200 to 1000 μm. Until this finding, the pores typically formed were spaced in the range of 4 to 30 μm center-to-center, while being 0.6 to 10 μm in diameter. Making highly isolated pores presents quite another challenge. In the previous work, the relative close spacing of the pores allowed the authors to conclude that the regions between the pores were almost totally depleted and that practically all carriers were collected by the pore tips. In such a case, neither the pore side walls nor the wafer surface etched as all holes were swept to the pore tips. Since the surface was not attacked by pore-forming holes, the quality of the pore initiation mask lost its relevance. In Cahill et al.'s case, on the other hand, a long-lived mask (>20 hours) needed to be developed to help prevent pore formation everywhere except at initiation pits. The mask eventually used is shown in Figure 16.46; it shows a SiC layer sandwiched between two layers of silicon nitride. The silicon nitride directly atop the silicon served to insulate the silicon carbide from the underlying substrate. As the silicon carbide proves very resistant to HF, loss of thickness did not show during the procedure. The top nitride served to protect the carbide during anisotropic pit formation. By lowering the bias to less than two volts with respect to a saturated calomel electrode (SCE) side-branching was avoided.

It seems very likely that this macropore formation phenomenon could extend to all types of n-type semiconductors. Some evidence with InP and GaAs supports this statement [Lehmann, 1993].

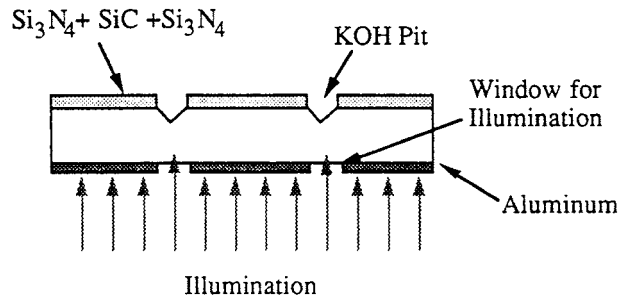


FIGURE 16.46 Long-lived macropore initiation mask.

16.7 Etch-Stop Techniques

16.7.1 Introduction

In many cases it is desirable to stop etching in silicon when a certain cavity depth or a certain membrane thickness is reached. Nonuniformity of etched devices due to nonuniformity of the silicon wafer thickness can be quite high. Taper of double-polished wafers, for example, can be as high as 40 μm [Lambrechts and Sansen, 1992]! Even with the best wafer quality the wafer taper is still around 2 μm. The taper and variation in etch depth lead to intolerable thickness variations for many applications. Etch-rate control typically requires monitoring and stabilization of:

- Etchant composition
- Etchant aging
  - Stabilization with N_2 sparging (especially with EDP and hydrazine)
  - Taking account of the total amount of material etched (loading effects)
- Etchant temperature
- Diffusion effects (constant stirring is required, especially for EDP)
  - Stirring also leads to a smoother surface through bubble removal
  - Trenching (also pillowing) and roughness decrease with increased stirring rate
- Light may affect the etch rate (especially with n-type Si)
- Surface preparation of the sample can have a big effect on etch rate (the native oxide retards etch start; a dip in dilute HF is recommended)

With good temperature, etchant concentration, and stirring control the variation in etch depth typically is 1% (see Figure 16.47) [Lambrechts and Sansen, 1992]. A good pretreatment of the surface to be etched is a standard RCA clean combined with a 5% HF dip to remove the native oxide immediately prior to etching in KOH.

In the early days of micromachining, one of the following techniques was used to etch a Si structure anisotropically to a predetermined thickness. In the simplest mode the etch time was monitored (Table 16.9 lists some etch rates for different etchants) or a bit more complex; the infrared transmittance was followed. For thin membranes the etch stop cannot be determined by a constant etch time method with sufficient precision. The spread in etch rates becomes critical if one etches membranes down to thicknesses of less than 20 μm; it is almost impossible to etch structures down to less than 10 μm with a timing technique. In the V-groove technique, V-grooves with precise openings (see Eq. (16.2)) were used such that the V-groove stopped etching at the exact moment a desired membrane thickness was reached (see Figure 16.48) [Samaun et al., 1973]. One can also design wider mask openings on the wafer's edge so that the wafer is etched through at those sites at the moment the membrane has reached the appropriate thickness. Although Nunn and Angell (1975) claimed that an accuracy of about 1 μm could be obtained using the V-groove method, none of the mentioned techniques are found to be production worthy. Nowadays the above methods are almost completely replaced by etch-stop techniques based on a change in etch rate dependant on doping level or chemical nature of a stopping layer. High resolution silicon micromachining relies on the availability of effective etch-stop layers. It is actually the existence of impurity-based etch stops in silicon that has allowed micromachining to become a high-yield production process.

16.7.2 Boron Etch Stop

The most widely used etch-stop technique is based on the fact that anisotropic etchants, especially EDP, do not attack boron-doped (p+) Si layers heavily. This effect was first noticed by Greenwood (1969). He assumed that the presence of a p-n junction was responsible.

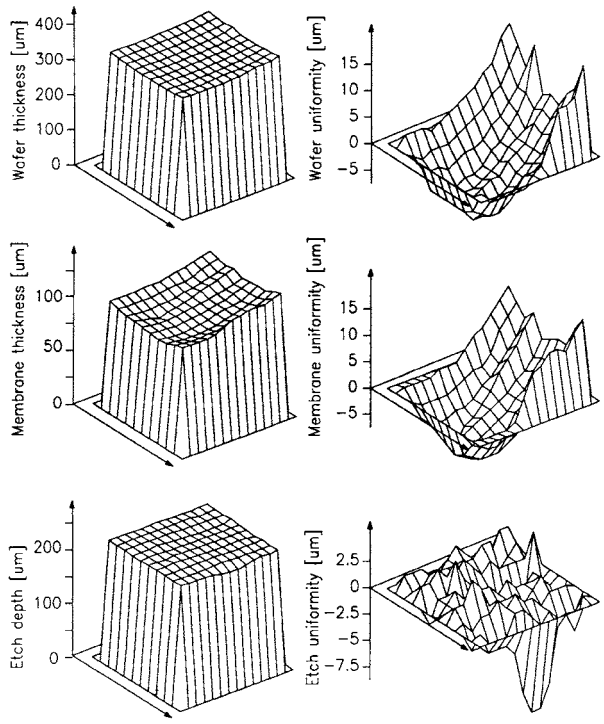


FIGURE 16.47 A map of the wafer thickness, the membrane thickness and the etch depth. (From Lambrechts, S.W. and W. Sansen, *Biosensors: Microelectrochemical Devices*, Institute of Physics Publishing, 1992. With permission.)

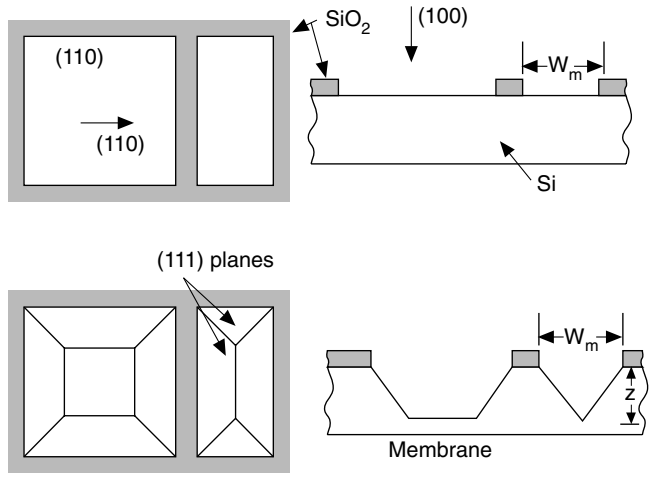


FIGURE 16.48 V-groove technique to monitor the thickness of a membrane. At the precise moment the V-groove is developed, the membrane has reached the desired thickness.

Bogh (1971) found that at an impurity concentration of about $7 \times 10^{19}/\text{cm}^3$ resulted in the etch rate of Si in EDP dropping sharply (see also Table 16.9), but without any requirement for a p-n junction. For KOH-based solutions, Price (1973) found a significant reduction in etch rate for boron concentrations above 5×10^{18} cm^{-3}. The model by Seidel et al., discussed above, provides an elegant explanation for the etch stop at high boron concentrations. At moderate dopant concentration, we saw that the electrons

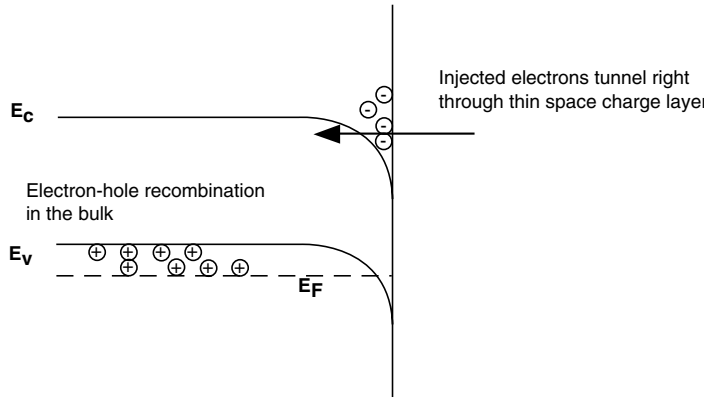


FIGURE 16.49 Si/electrolyte interface energetics at high doping level explaining etch-stop behavior.

injected into the conduction band stay localized near the semiconductor surface due to the downward bending of the bands (Figure 16.37). The electrons there have a small probability of recombining with holes deeper into the crystal even for p-type Si. This situation changes when the doping level in the silicon increases further. At a high dopant concentration, silicon degenerates and starts to behave like a metal. For a degenerate p-type semiconductor, the space charge thickness shrinks and the Fermi level drops into the valence band as indicated in Figure 16.49. The injected electrons shoot (tunnel) right through the thin surface charge layer into deeper regions of the crystal where they recombine with holes from the valence band. Consequently, these electrons are not available for the subsequent reaction with water molecules (Reaction 16.5), the reduction of which is necessary for providing new hydroxide ions in close proximity to the negatively charged silicon surface. These hydroxide ions are required for the dissolution of the silicon as $Si(OH)_4$. The remaining etch rate observed within the etch stop region is then determined by the number of electrons still available in the conduction band at the silicon surface. This number is assumed to be inversely proportional to the number of holes and thus the boron concentration. Experiments show that the decrease in etch rate is nearly independent of the crystallographic orientation and the etch rate is proportional to the inverse fourth power of the boron concentration in all alkaline etchants.

From the above it follows that a simple boron diffusion or implantation, introduced from the front of the wafer, can be used to create beams and diaphragms by etching from the back. The boron etch-stop technique is illustrated in Figure 16.50 for the fabrication of a micromembrane nozzle [Brodie and Muray, 1982]. The SiO_2 mesa in Figure 16.50b leads to the desired boron p^+ profile. The anisotropic etch from the back clears the lightly doped p-Si (Figure 16.50d). Layers of p^+ silicon having a thickness of 1 to 20 μm can be formed with this process. The boron etch stop constitutes a very good etch stop; it is not very critical when the operator takes the wafer out of the etchant. One important practical note is that the boron etch stop may become badly degraded in EDP solutions that were allowed to react with atmospheric oxygen. Since boron atoms are smaller than silicon, a highly doped, freely suspended membrane or diaphragm will be stretched; the boron-doped silicon is typically in tensile stress and the microstructures are flat and do not buckle. While doping with boron decreases the lattice constant, doping with germanium increases the lattice constant. A membrane doped with B and Ge still etches much slower than undoped silicon, and the stress in the layer is reduced. A stress-free, dislocation-free and slow etching layer (±10 nm/min) is obtained at doping levels of 10^{20} cm^{-3} boron and 10^{21} cm^{-3} germanium [Seidel et al., 1990; Heuberger, 1989]. One disadvantage with this etch-stop technique is that the extremely high boron concentrations are not compatible with standard CMOS or bipolar techniques, so they can only be used for microstructures without integrated electronics. Another limitation of this process is the fixed number and angles of (111) planes one can accommodate. The etch stop is less effective in KOH compared to EDP. Besides boron, other impurities have been tried for use in an etch stop in anisotropic

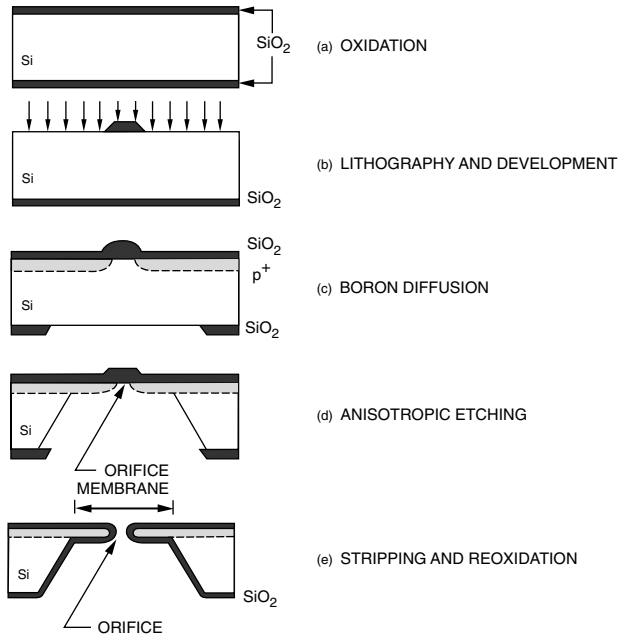


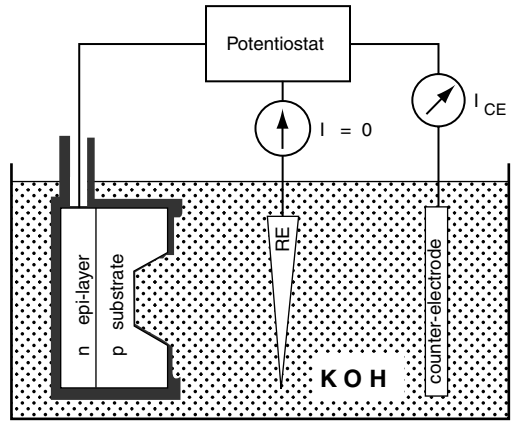
FIGURE 16.50 Illustration of the boron etch stop in the fabrication of a membrane nozzle. (From Brodie, I. and J. J. Muray, *The Physics of Microfabrication*, Plenum Press, New York, 1982. With permission.)

etchants. Doping Si with germanium has hardly any influence on the etch rate of either the KOH or EDP solutions. At a doping level as high as 5×10^{21} cm^{-3} the etch rate is barely reduced by a factor of two [Seidel et al., 1990].

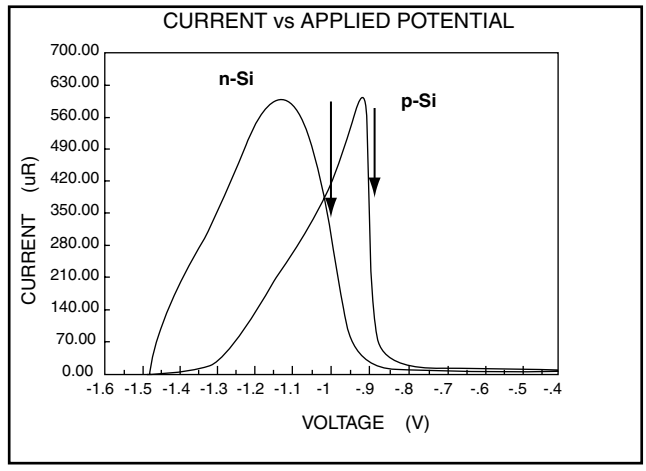
By burying the highly doped boron layer under an epitaxial layer of lighter doped Si the problem of incompatibility with active circuitry can be avoided. A ±1% thickness uniformity is possible with modern epilayer deposition equipment (see, for example, *Semiconductor International*, July 1993, pp. 80–83). A widely used method of automatically measuring the epi thickness is with infrared (IR) instruments, especially Fourier transform infrared (FTIR) [Rehrig, 1990]; see also Epitaxy later in this chapter and in Madou (1997, chap. 5).

16.7.3 Electrochemical Etch-Stop Technique

For the fabrication of piezoresistive pressure sensors, the doping concentration of the piezo resistor must be kept smaller than 1×10^{19} cm^{-3} because the piezoresistive coefficients drop considerably above this value and reverse breakdown becomes an issue. Moreover, high boron levels compromise the quality of the crystal by introducing slip planes and tensile stress and prevent the incorporation of integrated electronics. As a result, a boron stop often cannot be used to produce well-controlled thin membranes unless, as suggested above, the highly doped boron layer is buried underneath a lighter doped Si epi layer. Alternatively, a second etch-stop method, an electrochemical technique, can be used. In this case, a lightly doped p-n junction is used as an etch stop by applying a bias between the wafer and a counter electrode in the etchant. This technique was first proposed by Waggener (1970). Other early work on electrochemical etch-stops with anisotropic etchants such as KOH and EDP was performed by Palik et al. (1982), Jackson et al. (1981), Faust and Palik (1983) and Kim and Wise (1983). In electrochemical anisotropic etching a p-n junction is made, for example, by the epitaxial growth of an n-type layer (phosphorus-doped, 10^{15} cm^{-3}) on a p-type substrate (boron-doped, 30 Ωcm). This p-n junction forms a large diode over the whole wafer. The wafer is usually mounted on an inert substrate, such as a sapphire plate, with an acid-resistant wax and is partly or wholly immersed in the solution. An ohmic contact to the n-type epilayer is connected to one pole of a voltage source and the other pole of the voltage source is connected



A



B

FIGURE 16.51 Electrochemical etch stop. (A) Electrochemical etching set-up with potentiostatic control (three-electrode system). Potentiostatic control, mainly used in research studies, enables better control of the potential as it is referenced now to a reference electrode such as a saturated calomel electrode (SCE). In industrial settings, electrochemical etching is often carried out in a simpler two-electrode system, i.e., a Pt counter electrode and Si working electrode [Kloeck et al., 1989]. (B) Cyclic voltammograms of n- and p-type silicon in an alkaline solution at 60°C. Flade potentials are indicated with an arrow.

via a current meter to a counterelectrode in the etching solution (see Figure 16.51A). In this arrangement the p-type substrate can be selectively etched away and the etching stops at the p-n junction, leaving a membrane with a thickness solely defined by the thickness of the epilayer. The incorporation of a third electrode (a reference electrode) in the three-terminal method depicted in Figure 16.51A allows for a more precise determination of the silicon potential with respect to the solution than a two-terminal set-up as we illustrated in Figure 16.25.

At the Flade potential in Figure 16.51B, the oxide growth rate equals the oxide etch rate; a further increase of the potential results in a steep fall of the current due to complete passivation of the silicon surface. At potentials positive of the Flade potential, all etching stops. At potentials below the Flade potential, the current increases as the potential becomes more positive. This can be explained by the formation of an oxide which etches faster than it forms, i.e., the silicon is etched away. Whereas electrochemists like to talk about the Flade potential, physicists like to discuss matters in terms of the flat-band

potential. The flat-band potential is that applied potential at which there are no more fields within the semiconductor, i.e., the energy band diagram is flat throughout the semiconductor. The passivating SiO_2 layer is assumed to start growing as soon as the negative surface charge on the silicon electrode is cancelled by the externally applied positive bias, a bias corresponding to the flat band potential. At these potentials, the formation of $Si(OH)_x$ complexes does not lead to further dissolution of silicon, because two neighboring Si-OH HO-Si groups will react by splitting of water, leading to the formation of Si-O-Si bonds. As can be learned from Figure 16.51B, the value of the Flade potential depends on the dopant type. Consequently, if a wafer with both n and p regions exposed to the electrolyte is held at a certain potential in the passive range for n-type and the active range for p-type, the p-regions are etched away, whereas the n-regions are retained. In the case of the diode shown in Figure 16.51A, where at the start of the experiment only p-type Si is exposed to the electrolyte, one starts by applying a positive bias to the n-type epilayer (V_n). This reverse biases the diode, and only a reverse bias current can flow. The potential of the p-type layer in this regime is negative of the flat-band potential and active dissolution takes place. At the moment that the p-n junction is reached, a large anodic current can flow and the applied positive potential passivates the n-type epilayer. Etching continues on the areas where the wafer is thicker until the membrane is reached there, too. The thickness of the silicon membrane is thereby solely defined by the thickness of the epilayer; neither the etch uniformity nor the wafer taper will influence the result. A uniformity of better than 1% can be obtained on a 10-μm-thick membrane. The current vs. time curve can be used to monitor the etching process; at first, the current is relatively low, i.e., limited by the reverse bias current of the diode, then as the p-n junction is reached a larger anodic current can flow until all the p-type material is consumed and the current falls again to give a plateau. The plateau indicates we have reached the current associated with a passivated n-type Si electrode. The etch procedure can be stopped at the moment that the current plateau has been reached, and since the etch stop is thus basically one of anodic passivation one sometimes terms it an anodic oxidation etch stop. Registering an I vs. V curve as in Figure 16.51B will establish an upper limit on the applied voltage, V_n [McNeil et al., 1990] and such curves are used for *in situ* monitoring and controlling of the etch stop. A crude endpoint monitoring can be accomplished by the visual observation of cessation of hydrogen bubble formation accompanying Si etching. Palik et al. presented a detailed characterization of Si membranes made by electrochemical etch stop [Palik et al., 1988].

Hirata et al. (1988), using the same anodic oxidation etch stop in a hydrazine-water solution at 90 ± 5°C and a simple two-terminal electrochemical cell, obtained a pressure sensitivity variation of less than 20% from wafer to wafer (pressure sensitivity is inversely proportional to the square of membrane thickness). A great advantage of this etch-stop technique is that it works with Si with low doping levels of the order of 10^{16} cm^{-3}. Due to the low doping levels, it is possible to fabricate structures with a very low, or controllable, intrinsic stress. Moreover, active electronics and piezo membranes can be built into the Si without problems. A disadvantage is that the back of the wafer with the aluminum contact has to be sealed hermetically from the etchant solution which requires complex fixturing and manual wafer handling. The fabrication of a suitable etch holder is no trivial matter. The holder must (1) protect the epi-contact from the etchant, (2) provide a low-resistance ohmic contact to the epi and (3) must not introduce stress into wafers during etching [Peeters, 1994; Elwenspoek et al., 1994]. Stress introduced by etch holders easily leads to diaphragm or wafer fracture and etchant seepage through to the epi-side.

Using a four-electrode electrochemical cell, controlling the potentials of both the epitaxial layer and the silicon wafer, as shown in Figure 16.52, can further improve the thickness control of the resulting membrane by directly controlling the p/n bias voltage. The potential required to passivate n-type Si can be measured using the three-electrode system in Figure 16.51A, but this system does not take into account the diode leakage. If the reverse leakage is too large, the potential of the n-Si, V_n, will approach the potential of the p-Si, V_p. If there is a large amount of reverse diode leakage, the p-region may passivate prior to reaching the n-region and etching will cease. In the four-electrode configuration, the reverse leakage current is measured separately via a p-region contact, and the counter-electrode current may be monitored for end-point detection. The four-electrode approach allows etch stopping on lower

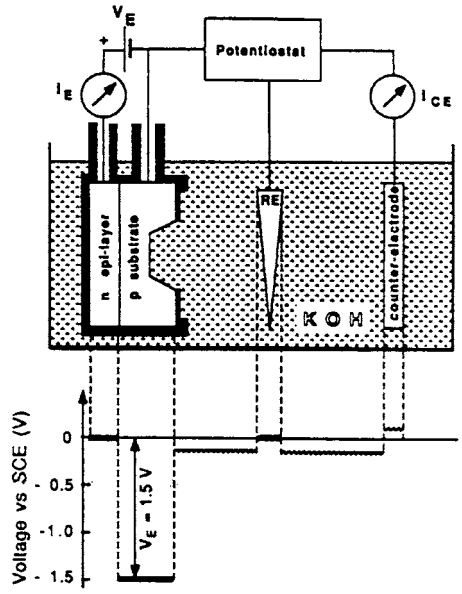


FIGURE 16.52 Four-electrode electrochemical etch-stop configuration. Voltage distribution with respect to the SCE reference electrode (RE) for the four-electrode case. The fourth electrode enables an external potential to be applied between the epitaxial layer and the substrate, thus maintaining the substrate at etching potentials. (From Kloeck et al., *IEEE Trans. Electron. Dev.*, 36, 663–669, 1989. With permission.)

quality epis (larger leakage current) and should also enable etch stopping of p-epi on n-substrates. Kloeck et al. (1989) demonstrated that using such an electrochemical etch-stop technique and with current monitoring, the sensitivity of pressure sensors fabricated on the same wafer could be controlled to within 4% standard deviation. These authors used a 40% KOH solution at 60 ± 0.5°C. Without the etch stop, the sensitivity from sensor to sensor on one wafer varied by a factor of 2.

The etching solution used in electrochemical etching can either be isotropic or anisotropic. Electrochemical etch stop in isotropic media was discussed above. In this case one uses HF/H_2O mixtures to etch the highly doped regions of p^+p, n^+n, n^+p, and p^+n systems [Theunissen et al., 1970; Meek, 1971; Theunissen, 1972; Wen and Weller, 1972; van Dijk, 1972]. The rate-determining step in etching with isotropic etchants does not involve reducing water with electrons from the conduction band as it does in anisotropic etchants and the etch stop mechanism, as we learned earlier is obviously different. In isotropic media, the etch stop is simply a consequence of the fact that higher conductivity leads to higher corrosion currents and the etch slows down on lower conductivity layer. A major advantage of the KOH electrochemical etch is that it retains all of the anisotropic characteristics of KOH without needing a heavily doped p^+ layer to stop the etch [Saro and van Herwaarden, 1986].

In Figure 16.53, we review the etch-stop techniques discussed so far: diffused boron etch stop, buried boron etch stop and electrochemical etch stop [Wise, 1985]. A comparison of the boron etch stop and the electrochemical etch stop reveals that the IC compatibility and the absence of built-in stresses, both due to the low dopant concentration, are the main assets of the electrochemical etch stop.

16.7.4 Photo-Assisted Electrochemical Etch Stop (for n-Type Silicon)

A variation on the electrochemical diode etch-stop technique is the photo-assisted electrochemical etch-stop method illustrated in Figure 16.54 [Mlcak et al., 1993]. An n-type silicon region on a wafer may be selectively etched in an HF solution by illuminating and applying a reverse bias across a p-n junction, driving the p-layer cathodic and the n-layer anodic. Etch rates up to 10 μm/min for the n-type material and a high resolution etch stop render this an attractive potential micromachining process. Advantages

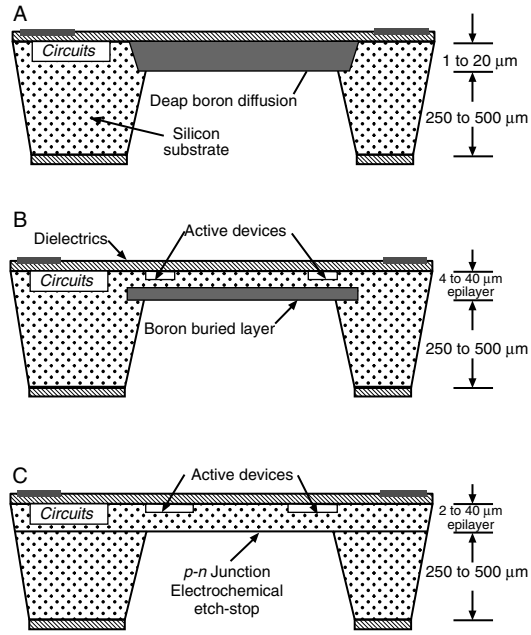


FIGURE 16.53 Typical cross sections of bulk micromachined wafers with various methods for etch-stop formation shown. (A) Diffused boron etch stop. (B) Boron etch stop as a buried layer. (C) Electrochemical etch stop. (From Wise, K.D., in *Silicon Micromachining and Its Application to High Performance Integrated Sensors,* Fung, C.D., Ed., Elsevier, New York, 1985. With permission.)

also include the use of lightly doped n-Si, bias- and illumination intensity-controlled etch rates, *in situ* process monitoring using the cell current and the ability to spatially control etching with optical masking or laser writing. Using this method [Mlcak et al., 1993] prepared stress-free cantilever beam test samples. They diffused boron into a 10^{15}-cm^{-3} (100) n-Si substrate through a patterned oxide mask, leaving exposed a small n-type region which defines two p-type cantilever beams (see Figure 16.54).

The boron diffusion resulted in a junction 3.3 μm underneath the surface. An ohmic contact on the backside of the wafer was used to apply a variable voltage across the p-n junction, and both p and n areas were exposed to the HF electrolyte. The exposed n-region was etched to a depth of 150 μm by shining light on the whole sample. The resulting n-type Si surface was at first found to be rough, as porous Si up to 5 μm in height forms readily in HF solutions. The Si surface could be made smoother by etching at higher bias (4.3 V vs. SCE) and higher light intensity (2 W/cm^2) to a finish with features of the order of 0.4 μm in height. Smoothing could also be accomplished by a 5-second dip in HNO_3:HF:H_3COOH or a 30-second dip in 25 wt%, 25°C, KOH. Yet another way of removing unwanted porous Si is a 1000°C wet oxidation to make oxidized porous Si (OPS) followed by an HF etch (see next section) [Yoshida et al., 1992].

16.7.5 Photo-Induced Preferential Anodization, PIPA (for p-Type Silicon)

Electrochemical etching requires the application of a metal electrode to apply the bias. The application of such a metal electrode often induces contamination and constitutes at least one extra process step, and extra fixturing is needed. With photo-induced preferential anodization (PIPA) it is not necessary to deposit metal electrodes. Here one relies on the illumination of a p-n junction to bias the p-type Si anodically, and the p-Si converts automatically into porous Si while the n-type Si acts as a cathode for the reaction. The principle of photo-biasing for etching purposes was known and patented by Shockley as far back as 1963 [Shockley, 1963]. In U.S. patent 3,096,262, he writes " … light can be used in place of electrical connections … for biasing of the sample …." This means a small isolated area of p-type

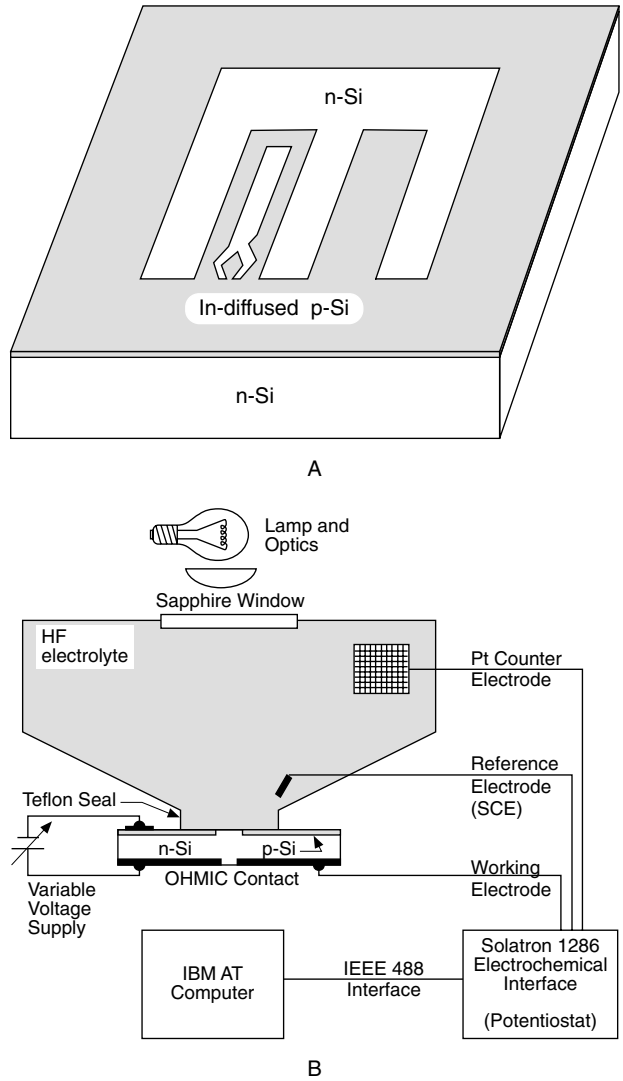


FIGURE 16.54 Photoelectrochemical etching. (A) Schematic of the photoeletrochemical etching experiment apparatus. (B) Schematic of the spatial geometry of the diffused p-Si layer into n-Si used to form cantilever beam structures. (From Mlcak, R. et al., Photo-Assisted Electromechanical Machining of Micromechanical Structures, presented at Micro Electromechanical Systems, Ft. Lauderdale, FL, 1993. With permission.)

material on an n-type body may be preferentially biased for removal of material beyond the junction by etching." The method was reinvented by Yoshida et al. (1992) and Peeters et al. (1993a; 1993b). The latter group called the method 'PHET' for photovoltaic electrochemical etch-stop technique, and the former group coined the PIPA acronym.

In PIPA, etch rates of up to 5 μm/min result in the formation of porous layers readily removed with Si etching solutions. An important advantage of the technique is that very small and isolated p-type islands can be anodized at the same time. The method also lends itself to fabricate three-dimensional structures using p-type Si as sacrificial layers [Yoshida et al., 1992]. A disadvantage of the technology is that one cannot control the process very well, as the current cannot be measured for endpoint detection. Application of PIPA to form a microbridge is shown in Figure 16.55. First, a buried p-Si layer doped to

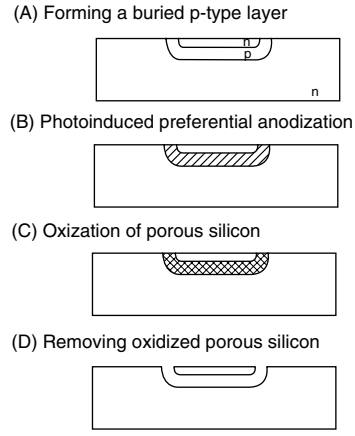


FIGURE 16.55 Photo-assisted electrochemical etch stop (for n-type Si). Fabrication process for a microbridge and SEM picture of Si structure before and after PIPA. (From Yoshida et al., Photo-Induced Preferential Anodization for Fabrication of Monocrystalline Micro-mechanical Structures, presented at Micro Electromechanical Systems, Travemunde, 1992. With permission.)

10^{18} cm^{-3} and an n-type layer doped to 10^{15} cm^{-3} are formed on an n-type substrate using epitaxy (Figure 16.55a). Then p-type is preferentially anodized in 10% HF solution under 30 mW/cm^2 light intensity for 180 minutes (Figure 16.55b), forming porous Si. The porous Si is then oxidized in wet oxygen at 1000°C (Figure 16.55c). Finally, the sacrificial layer of oxidized porous silicon is etched and removed with an HF solution (Figure 16.55d). The resulting surfaces of the n-type silicon are very smooth. It is interesting to consider making complicated three-dimensional structures by going immediately to the electropolishing regime instead. Yoshida et al. (1992) believe that porous silicon as a sacrificial intermediate is more suitable for fabricating complicated structures. The authors are probably referring to the fact that electropolishing is much more aggressive and could not be expected to lead to the same retention of the shape of the buried, sacrificial p-layers. Peeters et al. (1993) carry out their photovoltaic etching in KOH, thus skipping the porous Si stage of Yoshida et al. They, like Yosida et al., stress the fact that in one single etch step this technique can make a variety of complex shapes that would be impossible with electrochemical etching techniques. These authors found it necessary to coat the n-Si part of the wafer with Pt to get enough photovoltaic drive for the anodic dissolution; this metallization step makes the process more akin to the photoelectrochemical etching and some of the advantage of the photobiasing process is being lost.

16.7.6 Etch Stop at Thin Films-Silicon on Insulator

Yet another distinct way (the fourth) to stop etching is by employing a change in composition of material. An example is an etch stopped at a Si_3N_4 diaphragm. Silicon nitride is very strong, hard and chemically inert and the stress in the film can be controlled by changing the Si/N ratio in the LPCVD deposition process. The stress turns from tensile in stoichiometric films to compressive in silicon-rich films (for details see later in this chapter). A great number of materials are not attacked by anisotropic etchants. Hence, a thin film of such a material can be used as an etch stop.

Another example is the SiO_2 layer in a silicon-on-insulator structure (SOI). A buried layer of SiO_2, sandwiched between two layers of crystalline silicon, forms an excellent etch stop because of the good selectivity of many etchants of Si over SiO_2. The oxide does not exhibit the good mechanical properties of silicon nitride and is consequently used rarely as a mechanical member in a microdevice. As with the photoinduced preferential anodization (PiPA), no metal contacts are needed with an SOI etch stop, greatly simplifying the process over an electrochemical etch stop technique.

16.8 Problems with Wet Bulk Micromachining

16.8.1 Introduction

Despite the introduction of better controllable etch-stop techniques, bulk micromachining remains a difficult industrial process to control. It is also not an applicable submicron technology, because wet chemistry is not able to etch reliably on that cale. For submicron structure definition dry etching is required (dry etching is also more environmentally safe). We will look now into some of the other problems associated with bulk micromachining, such as the extensive real estate consumption and difficulties in etching at convex corners, and detail the solutions that are being worked on to avoid, control or alleviate those problems.

16.8.2 Extensive Real Estate Consumption

16.8.2.1 Introduction

Bulk micromachining involves extensive real estate consumption. This quickly becomes a problem in making arrays of devices. Consider the diagram in Figure 16.56, illustrating two membranes created by etching through a <100> wafer from the backside until an etch stop, say a Si_3N_4 membrane, is reached. In creating two of these small membranes a large amount of Si real estate is wasted and the resulting device becomes quite fragile.

16.8.2.2 Real Estate Gain by Etching from the Front

One solution to limiting the amount of Si to be removed is to use thinner wafers, but this solution becomes impractical below 200 μm as such wafers break too often during handling. A more elegant solution is to etch from the front rather than from the back. Anisotropic etchants will undercut a masking material an amount dependent on the orientation of the wafer with respect to the mask. Such an etchant will etch any <100> silicon until a pyramidal pit is formed, as shown in Figure 16.57. These pits have sidewalls with a characteristic 54.7° angle with respect to the surface of a <100> silicon wafer, since the

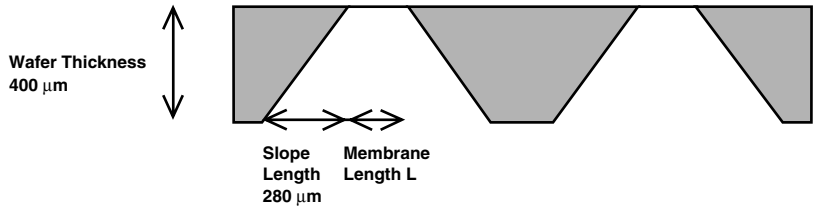


FIGURE 16.56 Two membranes formed in a <100>-oriented silicon wafer.

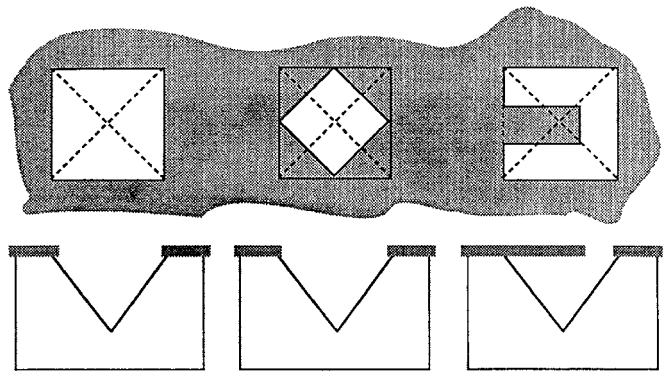


FIGURE 16.57 Three anisotropically etched pits etched from the front in a <100>-oriented silicon wafer.

delineated planes are {111} planes. This etch property makes it possible to form cantilever structures by etching from the front side, as the cantilevers will be undercut and eventually will be suspended over a pyramidal pit in the silicon. Once this pyramidal pit is completed, the etch rate of the {111} planes exposed is extremely slow and practically stops. Process sequences, which depend on achieving this type of a final structure, are therefore very uniform across a wafer and very controllable. The upper drawings in Figure 16.57 represent patterned holes in a masking material: a square, a diamond and a square with a protruding tab. The drawings immediately below represent the etched pit in the silicon produced by the anisotropic etchant. Note in the first drawing that the square mask produces a four-sided pyramidal pit. In the second drawing, a similar shape oriented at 45° produces an etched pit which is oriented parallel to the pit etched in the first drawing. In the second drawing the corners of the diamond are undercut by the etchant as it produces the final etch pit. The third drawing illustrates that any protruding member is eventually undercut by the anisotropic etchant, leaving a cantilever structure suspended over the etch pit.

16.8.2.3 Real Estate Gain by Using Silicon Fusion-Bonded Wafers

Using silicon fusion-bonded (SFB) wafers rather than conventional wafers also makes it possible to fabricate much smaller microsensors. The process is clarified in Figure 16.58 for the fabrication of a gauge pressure sensor [Bryzek et al., 1990]. The bottom, handle wafer has a standard thickness of 525 μm and is anisotropically etched with a square cavity pattern. Next, the etched handle wafer is fusion bonded to a top sensing wafer (see SFB and surface micromachining later in this chapter, and packaging in Madou [1997, chap. 8]). The sensor wafer consists of a p-type substrate with an n-type epilayer corresponding to the required thickness of the pressure-transducing membrane. The sensing wafer is thinned all the way to the epilayer by electrochemical etching and resistors are ion implanted. The handle wafer is ground and polished to the desired thickness. For gauge measurement, the anisotropically etched cavity is truncated by the polishing operation, exposing the backside of the diaphragm. For an absolute pressure sensor the cavity is left enclosed. With the same diaphragm dimensions and the same overall thickness of the chip, an SFB device is almost 50% smaller than a conventional machined device (see Figure 16.59).

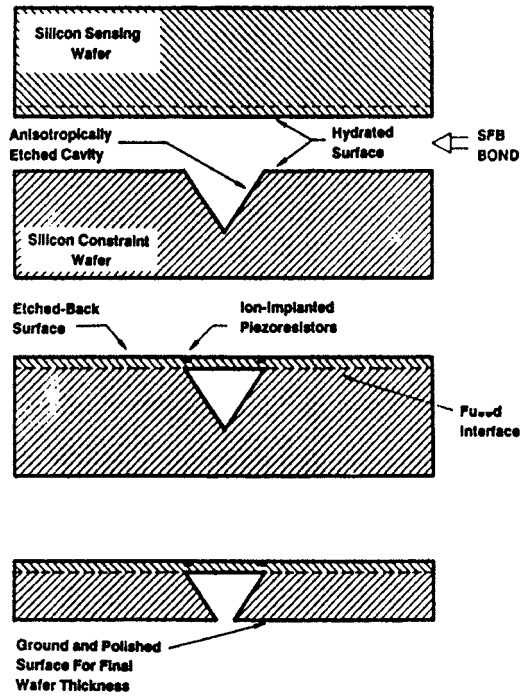


FIGURE 16.58 Fabrication process of an SFB-bonded gauge pressure sensor. (From Bryzek, J. et al., *Silicon Sensors and Microstructures*, Novasensor, Fremont, CA, 1990. With permission.)

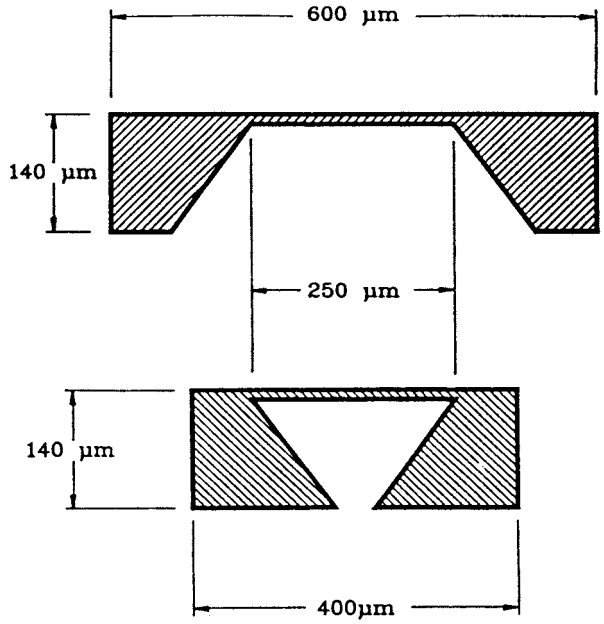


FIGURE 16.59 Comparison of conventional and SFB processes. The SFB process results in a chip which is at least 50% smaller than the conventional chip. (From Bryzek, J. et al., *Silicon Sensors and Microstructures*, Novasensor, Fremont, CA, 1990. With permission.)

16.8.3 Corner Compensation

16.8.3.1 Underetching

Underetching of a mask which contains no convex corners, i.e., corners turning outside in, in principle stems from mask misalignment and/or from a finite etching of the {111} planes. Peeters measured the widening of {111}-walled V-grooves in a (100) Si wafer after etching in 7 *M* KOH at 80 ± 1° over 24 hours as 9 ± 0.5 µm [Peeters, 1994]. The sidewall slopes of the V-groove are a well-defined 54.74°, and the actual etch rate R_{111} is related to the rate of V-groove widening R_v through:

$$R_{111} = \frac{1}{2}\sin(54.74°)R_v \qquad \text{or} \qquad R_{111} = 0.408 \cdot R_v \tag{16.41}$$

with R_{111} the etch rate in nm/min and R_v the groove widening, also in nm/min. The V-groove widening experiment then results in a R_{111} of 2.55 ± 0.15 nm/min. In practice, this etch rate implies a mask underetching of only 0.9 µm for an etch depth of 360 µm. For a 1-mm-long V-groove and a 1° misalignment angle, a total underetching of 18 µm is theoretically expected, with 95% due to misalignment and only 5% due to etching of the {111} sidewalls [Peeters, 1994]. The total underetching will almost always be determined by misalignment, rather than by etching of {111} walls.

Mask underetching with masks that do include convex corners is usually much larger than the underetching just described, as the etchant tends to circumscribe the mask opening with {111} walled cavities. This is usually called undercutting rather than underetching. It is advisable to avoid mask layouts with convex corners. Often mesa-type structures are essential, though, and in that case there are two possible ways to reduce the undercutting. One is by chemical additives, reducing the undercut at the expense of a reduced anisotropy ratio, and the other is by a special mask compensating the undercut at the expense of more lost real estate.

16.8.3.2 Undercutting

When etching rectangular convex corners, deformation of the edges occurs due to undercutting. This is an unwanted effect, especially in the fabrication of, say, acceleration sensors, where total symmetry and perfect 90° convex corners on the proof mass are mandatory for good device prediction and specification. The undercutting is a function of etch time and thus directly related to the desired etch depth. An undercut ratio is defined as the ratio of undercut to etch depth (δ/H).

Saturating KOH solutions with isopropanol (IPA) reduces the convex corner undercutting; unfortunately, this happens at the cost of the anisotropy of the etchant. This additive also often causes the formation of pyramidical or cone-shaped hillocks [Peeters, 1994; Gravesen, 1986]. Peeters claims that these hillocks are due to carbonate contamination of the etchant and he advises etching under inert atmosphere also and stock-piling all etchant ingredient under an inert nitrogen atmosphere [Peeters, 1994].

Undercutting can also be reduced or even prevented by so-called corner compensation structures which are added to the corners in the mask layout. Depending on the etching solution, different corner compensation schemes are used. Commonly used are square corner compensation (EDP or KOH) and rotated rectangle corner compensation methods (KOH). In Figure 16.60, these two compensation methods are illustrated. In the square corner compensation case, the square of SiO_2 in the mask, outlining the square proof mass feature for an accelerometer, is enhanced by adding an extra SiO_2 square to each corner (Figure 16.60a). Both the proof mass and the compensation squares are aligned with their sides parallel to the <110> direction. In this way, two concave corners are created at the convex corner to be protected. Thus, direct undercutting is prevented. The three 'sacrificial' convex corners at the protective square

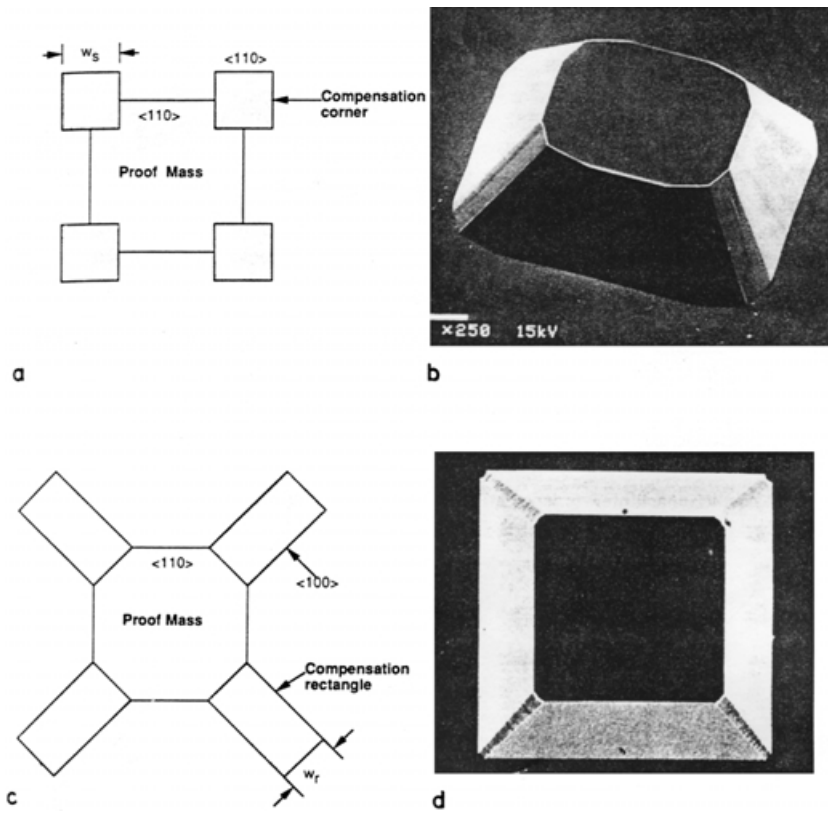


FIGURE 16.60 Formation of a proof mass by silicon bulk micromachining. (a,b) Square corner compensation method, using EDP as the etchant. (c,d) Rotated rectangle corner compensation method, using KOH as the etchant.

are undercut laterally by the fast etching planes during the etch process. The dimension of the compensation square, w_s, for a 500-μm-thick wafer (4 in.) is about 500 μm. The resulting mesa structure after EDP or KOH etching is shown in Figure 16.60b. In the rotated rectangle corner compensation method shown in Figure 16.60c, a properly scaled rectangle (w_r should be twice the thickness of the wafer) is added to each of the mask corners. The four sides of the mesa square are still aligned along the <110> direction, but the compensation rectangles are rotated (45°) with their longer sides along the <100> directions. Using KOH as an etchant reveals the mesa shown in Figure 16.60d. A proof mass is frequently dislodged by simultaneously etching from the front and the back. Corner compensation requires significant amount of space around the corners, making the design less compact, and the method is often only applicable for simple geometries.

Different groups around the world have been using different corner compensation schemes and they all claim to have optimized spatial requirements. For an introduction to corner compensation, refer to Puers and Sansen (1990), and Sandmaier et al. (1991) for KOH etching use <110>-oriented beams, <110>-oriented squares and <010>-oriented bands for corner compensation. They found that spatial requirements for compensation structures could be reduced dramatically by combining several of these compensation structures. The mask layouts for some of the different compensation schemes used by Sandmaier et al. are shown in Figure 16.61. To understand the choice and dimensioning of these compensation structures, as well as those in Figure 16.60, we will first look at the planes emerging at convex corners during KOH

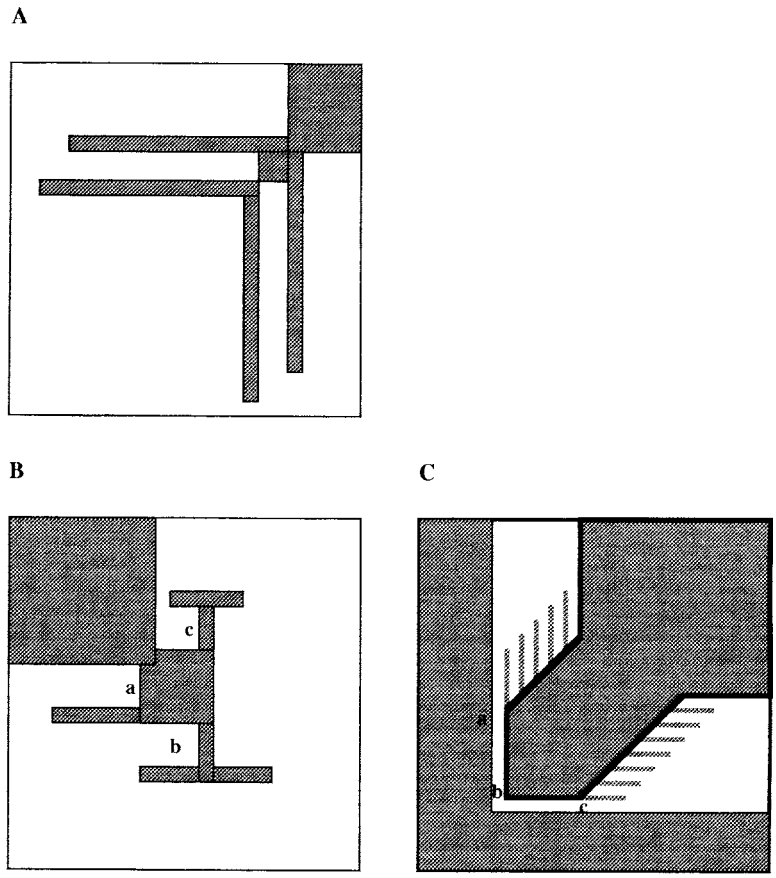


FIGURE 16.61 Mask layout for various convex corner compensation structures. (From Sandmaier, H. et al., Corner Compensation Techniques in Anisotropic Etching of (100) Silicon Using Aqueous KOH, presented at Transducers '91, San Francisco, CA, 1991. With permission.)

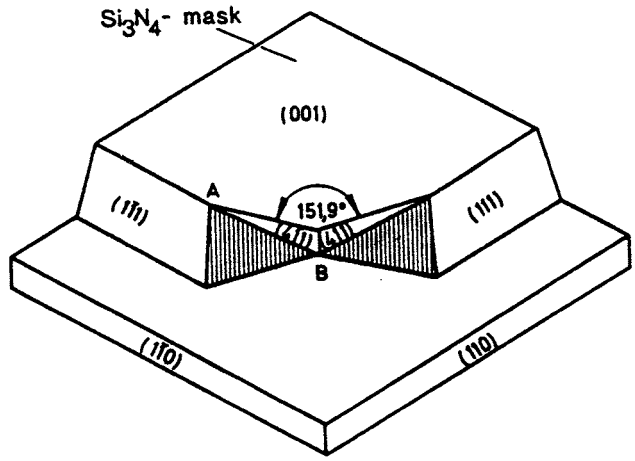


FIGURE 16.62 Planes occurring at convex corners during KOH etching. (From Mayer, G.K. et al., *J. Electrochem. Soc.*, 137, 3947–3951, 1990. With permission.)

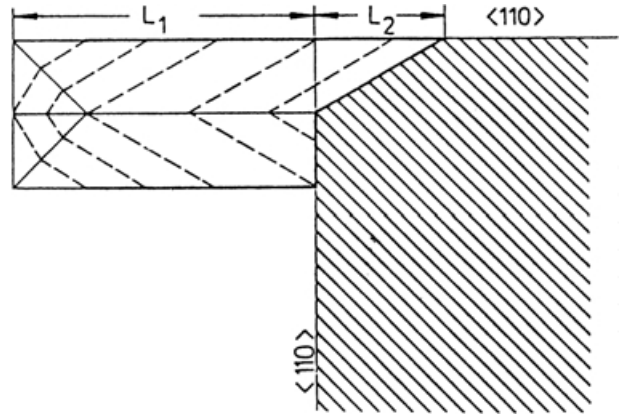


FIGURE 16.63 Dimensioning of the corner compensation structure with a <110>-oriented beam. (From Sandmaier, H. et al., Corner Compensation Techniques in Anisotropic Etching of (100) Silicon Using Aqueous KOH, presented at Transducers '91, San Francisco, CA, 1991. With permission.)

etching. Mayer et al. (1990) found that the undercutting of convex corners in pure KOH etch is determined exclusively by {411} planes. The {411} planes of the convex underetching corner, as shown in Figure 16.62, are not entirely laid free, however; rugged surfaces, where only fractions of the main planes can be detected, overlap the {411} planes under a diagonal line shown as AB in this figure. The ratio of {411} to {100} etching does not depend on temperature between 60 and 100°C. The value does decline with increasing KOH concentration from about 1.6 at 15% KOH to 1.3 at above 40% where the curve flattens out [Mayer et al., 1990]. Ideally one avoids rugged surfaces and searches for well-defined planes bounding the convex corner. In Figure 16.63 it is shown how a <110> beam is added to the convex corner to be etched. The fast etching {411} planes, starting at the two convex corners, are laterally underetching a <110>-oriented beam (broken lines in Figure 16.63). It is clear that the longer this <110>-oriented beam is, the longer the convex corner is protected from undercutting. It is essential that by the end of the etch the beam has disappeared to maintain a minimum of rugged surface at the convex edge. On the other hand, as is obvious from Figure 16.63, a complete disappearance of the beam

leads to a beveling at the face of the convex corner. The dimensioning of the compensating <110> beam works then as follows: the length of the compensating beam is calculated primarily from the required etch depth (H) and the etch rate ratio $R\{411\}/R\{100\}$ ($\approx\delta/H$), at the concentration of the KOH solution used:

$$L = L_1 - L_2 = 2H\frac{R\{411\}}{R\{100\}} - \frac{B_{<110>}}{2\tan(30.9°)} \tag{16.42}$$

with H the etch depth; $B_{<110>}$ the width of the <110>-oriented beam; tan (30.9°) the geometry factor [Mayer et al., 1990]. The factor 2 is the first term of this equation results as the etch rate of the {411} plane is determined normal to the plane and has to be converted to the <110> direction. The second term in Eq. (16.42) takes into account that the <110> beam needs to disappear completely by the time the convex corner is reached. The resulting beveling in Figure 16.63 can be reduced by further altering the compensation structures. This is done by decelerating the etch front, which largely determines the corner undercutting. One way to accomplish this is by creating more concave shapes right before the convex corner is reached. In Figure 16.61A, splitting of the compensation beam creates such concave corners, and by arranging two such double beams a more symmetrical final structure is achieved. By using these split beams, the bevelling at the corner is reduced by a factor of 1.4 to 2 and leads to bevel angles under 45°.

Corner compensation with <110>-oriented squares (as shown in Figure 16.60A) features considerably higher spatial requirements than the <110>-oriented beams. Since these squares are again undercut by {411} planes that are linked to the rugged surfaces described above, the squares do not easily lead to sharp {111}-defined corners. Dimensioning of the compensation square is done by using Eq. (16.42) again, where L_1 is half the side length of the square, and for $B_{<110>}$ the side length is used. All fast-etching planes have to reach the convex corner at the same time. As before, the spatial requirements of this compensation structure can be reduced if it is combined with <110>-oriented beams. Such a combination is shown in Figure 16.61B. The three convex corners of the compensation square are protected from undercutting by the added <110> beams. During the first etch step, the <110>-oriented side beams are undercut by the etchant. Only after the added beams have been etched does the square itself compensate the convex corner etching. The dimensioning of this combination structure is carried out in two steps. First the <110>-oriented square is selected with a size that is permitted by the geometry of the device to be etched. From these dimensions, the etch depth corresponding to this size is calculated from Eq. (16.42). For the remaining etch depth the <110>-oriented beams are dimensioned like any other <110>-oriented beam. If the side beam on corner b is selected about 30% longer than the other two side beams, the quality of the convex corner can be further improved. In this case, the corner is formed by the etch fronts starting at the corners a and b (Figure 16.61B).

A drawback to all the above proposed compensation schemes is the impossibility, due to rugged surfaces always accompanying {411} planes, of obtaining a clean corner in both the top and the bottom of a convex edge. Buser and de Rooij (1988) introduced a compensation scenario where a convex corner was formed by two {111} planes which were well defined all the way from the mask to the etch bottom. No rugged, undefined planes show in this case. The mask layout to create such an ideal convex corner has bands that are added to convex corners in the <100> direction (see Figure 16.61C and Figure 16.60c and d). These bands will be underetched by vertical {100} planes from both sides. With suitable dimensioning of such a band, a vertically oriented membrane results, thinning, and eventually freeing the convex edge shortly before the final intended etch depth is reached. In contrast to compensation structures undercut by {411} planes, posing problems with undefined rugged surfaces (see above), this compensation structure is mainly undercut by {100} planes. Over the temperature range of 50 to 100°C and KOH concentrations ranging from 25 to 50 wt%, no undefined surfaces could be detected in the case of structures undercut by {100} planes [Sandmaier et al., 1991]. The width of these <010>-oriented compensation beams, which determines the minimum dimension of the structures to etch,

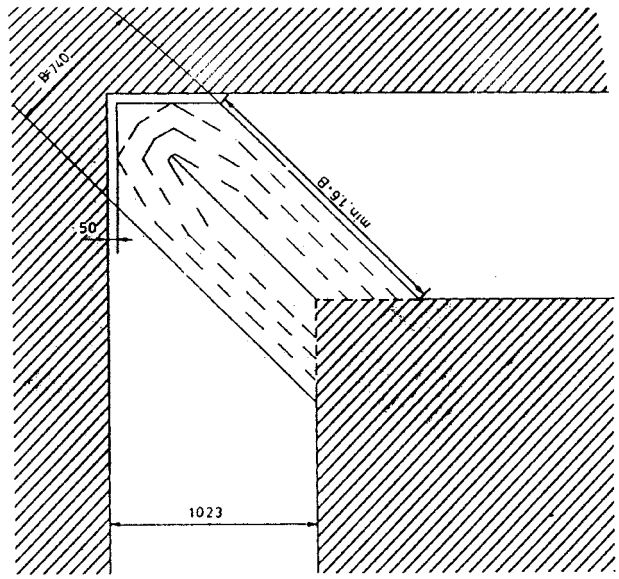


FIGURE 16.64 Beam structure open on one side. The beam is oriented in the <010> direction. Dimensions in microns. B is the width of the beam.

has to be twice the etching depth. These beams can either connect two opposite corners and protect both from undercutting simultaneously, or they can be added to the individual convex corners (open beam). With an open beam approach (see Figure 16.64) one has to be certain that the {100} planes reach the corner faster than the {411} planes. For that purpose the beams have to be wide enough to avoid complete underetching by {411} planes moving in from the front side, before they are completely underetched by {100} planes moving in from the side. For instance, in a 33% KOH etchant a ratio between beam length and width of at least 1.6 is required. To make these compensation structures smaller while at the same time maintaining {100} undercutting to define the final convex corner, Sandmaier et al. remarked that the shaping {100} planes do not need to be present at the beginning of the etching process. These authors implement delaying techniques by adding fan-like <110>-oriented side beams to a main <100>-oriented beam (see Figure 16.61C). As described above, these narrow beams are underetched by {411} planes and the rugged surfaces they entail until reaching the <100>-oriented beam. Then the {411} planes are decelerated in the concave corners between the side beams by the vertical {100} planes with slower etching characteristics. The length of the <110>-oriented side beams is calculated from:

$$L_{\langle 110\rangle} = \left(H - \frac{B_{\langle 010\rangle}}{2}\right)\frac{R\{411\}}{R\{100\}} \tag{16.43}$$

with H being the etching depth at the deepest position of the device.

The width of the side beams does not influence the calculation of their required length. In order to avoid the rugged surfaces at the convex corner, the width of the side beams as well as the spaces between them should be kept as small as possible. For an etching depth of 500 μm, a beam width of 20 μm and a space width of 2 μm are optimal [Sandmaier et al., 1991].

Depending on the etchant, different planes are responsible for undercutting. From the above we learned that in pure KOH solutions undercutting, according to Mayer et al. (1990) and Sandmaier et al. (1991), mainly proceeds through {411} planes or {100} planes. That the {411} planes are the fastest undercutting

planes was confirmed by Seidel (1986); at the wafer surface, the sectional line of a (411) and a (111) plane point in the <410> direction, forming an angle of 30.96° with the <110> direction, and it was in this direction that he found a maximum in the etch rate. In KOH and EDP etchants Bean (1978) identified the fast undercutting planes as {331} planes. Puers and Sansen (1990), for alkali/alcohol/water, identified the fast underetching planes as {331} planes, as well. Mayer et al. (1990), working with pure KOH, could not confirm the occurrence of such planes. Lee indicated that in hydrazine-water the fastest underetching planes are {211} planes [Lee, 1969]. Abu-Zeid (1984) reported that the main beveling planes are {212} planes in ethylene-diamine-water solution (no added pyrocatechol). Wv and Ko (1989) found the main beveling planes at undercut corners to be {212} planes whether using KOH, hydrazine, or EPW solutions are used. In view of our earlier remarks on the sensitivity of etching rates of higher index rates on a wide variety of parameters (temperature, concentration, etching size, stirring, cation effect, alcohol addition, complexing agent, etc.) these contradictory results are not too surprising. Along the same line, Wu and Ko (1989) and Peurs et al. (1990) have suggested triangles to compensate for underetching, but Mayer et al. (1997) found them to lead to rugged surfaces at the convex corner. Combining a chemical etchant with more limited undercutting (IPA in KOH) with Sandmaier's reduced compensation structure schemes could further decrease the required size of the compensation features while retaining an acceptable anisotropy.

Corner compensation for <110>-oriented Si was explored by Ciarlo [1987]. Ciarlo comments that both corner compensation and corner rounding can be minimized by etching from both surfaces so as to minimize the etch time required to achieve the desired features. This requires accurate front-to-back alignment and double-sided polished wafers.

Employing corner compensation offers access to completely new applications such as rectangular solids, orbiting V-grooves, truncated pyramids with low cross-sections on the wafer surface, bellow structures for decoupling mechanical stresses between micromechanical devices and their packaging, etc. [Sandmaier et al., 1991].

16.9 Wet Bulk Micromachining Examples

Example 1. Dissolved Wafer Process

Figure 16.65 illustrates the dissolved wafer process Cho is optimizing for the commercial production of low-cost inertial instruments [Cho, 1995]. This process, also in use by Draper Laboratory [Greiff, 1995; Weinberg et al., 1996] for the same application, involves a sandwich of a silicon sensor anodically bonded to a glass substrate. The preparation of the silicon part requires only two masks and three processing steps. A recess is KOH-etched into a p-type (100) silicon wafer (step 1 with mask 1), followed by a high-temperature boron diffusion (step 2 with no mask). In step one RIE may be used as well. Cho claims that by maintaining a high-temperature uniformity in the KOH etching bath (±0.1°C), the accuracy and absolute variation of the etch across the wafer, wafer-to-wafer, and lot-to-lot, can be maintained to <0.1 μm using pre-mixed, 45 wt% KOH. Cho is also using low-defect oxidation techniques (e.g., nitrogen annealing and dry oxidation) to form defect-free silicon surfaces. In the boron diffusion the key is optimizing the oxygen content. In general, the optimal flow of oxygen is on the order of 3 to 5% of the nitrogen flow, in which case the doping uniformity is on the order of ±0.2 μm. Varying the KOH etch depth and the shallow boron diffusion time, a wide variety of operating ranges and sensitivities for sensors can be obtained. Next, the silicon is patterned for a reactive ion etching (RIE) etch (step 3 with mask 2). Aspect ratios above 10 are accessible. Using some of the newest dry etching techniques depths in excess of 500 μm at rates above 4 μm/min (with a SF_6 chemistry) are now possible [Craven and Pandhumsporn, 1995]. The glass substrate (#7740 Corning glass) preparation involves etching a recess, depositing and in a one-mask step patterning a multi-metal system of Ti/Pt/Au. The electrostatic bonding of glass to silicon takes place at 335°C with a potential of 1000 V applied between the two parts (electrostatic or anodic bonding is explained in detail in Madou [1997, chap. 8]). Commercial bonders have alignment accuracies on the order of <1 μm. The lightly doped silicon is dissolved in an EDP solution at 95°C. The keys to uniform EDP etching are temperature uniformity

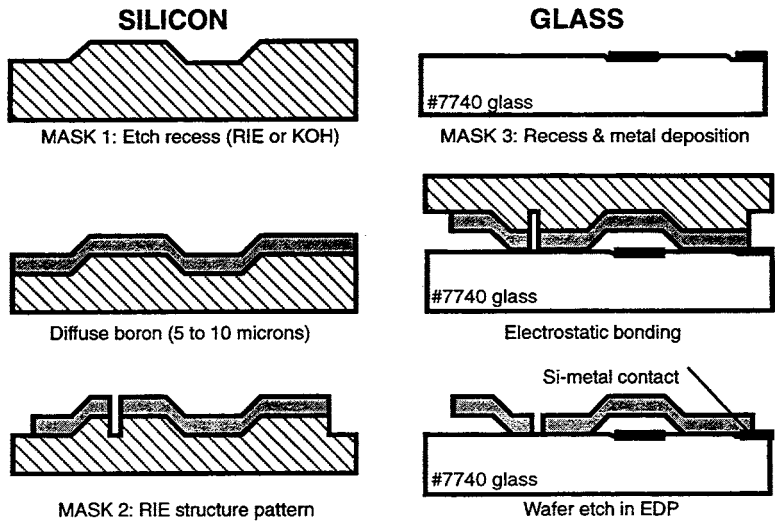


FIGURE 16.65 Dissolved wafer process. (From Greiff, P., SOI-Based Micromechanical Process, presented at Micromachining and Microfabrication Process Technology, Austin, TX, 1995. With permission.)

and suppression of etchant depletion through chemical aging or restricted flow (e.g., through bubbles). These effects can be minimized by techniques that optimize temperature control and reduce bubbling (e.g., proper wafer spacing, lower temperature, large bath). The structures are finally rinsed in DI water and a hot methanol bath.

Draper Laboratory, although obtaining excellent device results with the dissolved wafer process, is now exploring an SOI process as an alternative. The latter yields an all-silicon device while preserving many of the dissolved wafer process advantages (see also "SOI Surface Micromachining" later in this chapter).

Example 2. An Electrochemical Sensor Array Measuring pH, CO_2, and O_2 in a Dual Lumen Catheter

This sensor array developed by the author is shown in Figure 16.66, packaged and ready for *in vivo* monitoring of blood pH, CO_2 and O_2. The linear electrochemical array fits inside a 20-gauge catheter (750 μm in diameter) without taking up so much space as to distort the pressure signal monitored by a pressure sensor outside the catheter. A classical (macro) reference electrode, making contact with the blood through the saline drip, was used for the pH signal, while the CO_2 and O_2 had their own internal reference electrodes. The high impedance of the small electrochemical probes makes a close integration of the electronics mandatory; otherwise, the high impedance connector leads, in a typical hospital setting, act as antennas for the surrounding electronic noise. As can be seen from the computer-aided design (CAD) picture in Figure 16.67, the thickness of the sensor comes from two silicon pieces, the top piece containing electrochemical cells and the bottom piece containing the active electronics. Each wafer is 250 μm thick. The individual electrochemical cells are etched anisotropically into the top silicon wafer. The bottom piece is fabricated in a custom IC housing using standard IC processes. The process sequence to build a generic electrochemical cell in a 250-μm-thick Si wafer with one or more electrodes at the bottom of each well is illustrated in Figure 16.68. Electrochemical wells are etched from the front of the wafer and, after an oxidation step, access cavities for the metal electrodes are also etched from the back. The etching of the vias stops at the oxide-covered bottoms of the electrochemical wells (Figure 16.68A). Next, the wafers are oxidized a second time with the oxide thickness doubling everywhere except in the suspended window areas where no more Si can feed further growth (Figure 16.68B). The desired electrode metal is subsequently deposited from the back of the wafer into the access cavities and against the oxide window

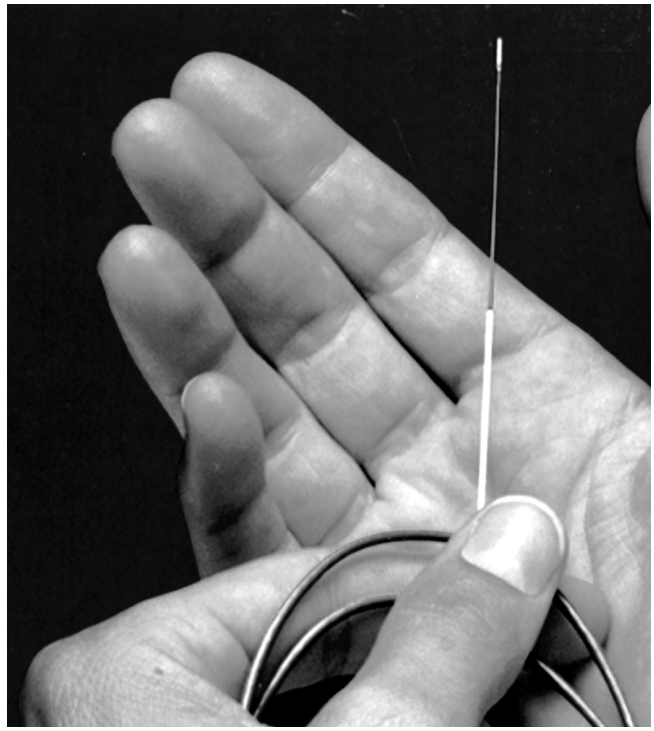


FIGURE 16.66 An *in vivo* pH, CO_2 and O_2 sensor based on a linear array of electrochemical cells.

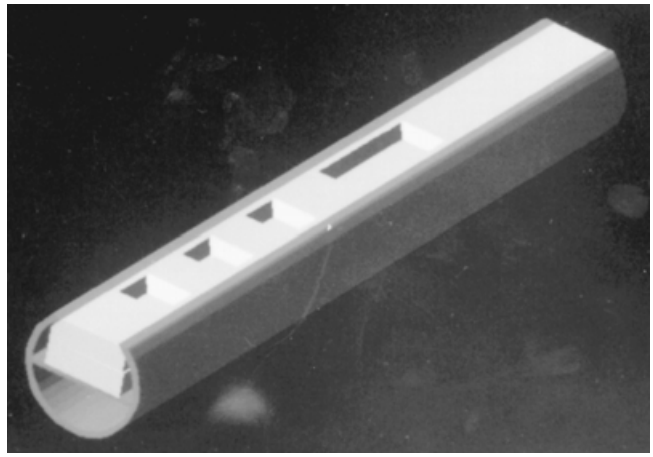


FIGURE 16.67 CAD of the electrochemical sensor array showing two pieces of Si (each 250 μm thick) on top of each other, mounted in a dual lumen catheter. The bottom part of the catheter is left open so pressure can be monitored and blood samples can be taken.

(Figure 16.68C). Finally, a timed oxide etch removes the sacrificial oxide window from above the underlying metal, while preserving the thicker oxide layer in the other areas on the chip (Figure 16.68D) [Joseph et al., 1989; Madou and Otagawa, 1989; Holland et al., 1988]. An SEM micrograph demonstrating step D in Figure 16.68 is shown in Figure 16.69. The electrodes in the electrochemical cells of the top wafer are further connected to the bottom wafer electronics by solder balls in the access vias of the top silicon wafer (see Figure 16.70). Separating the chemistry from the electronics in this way provides extra

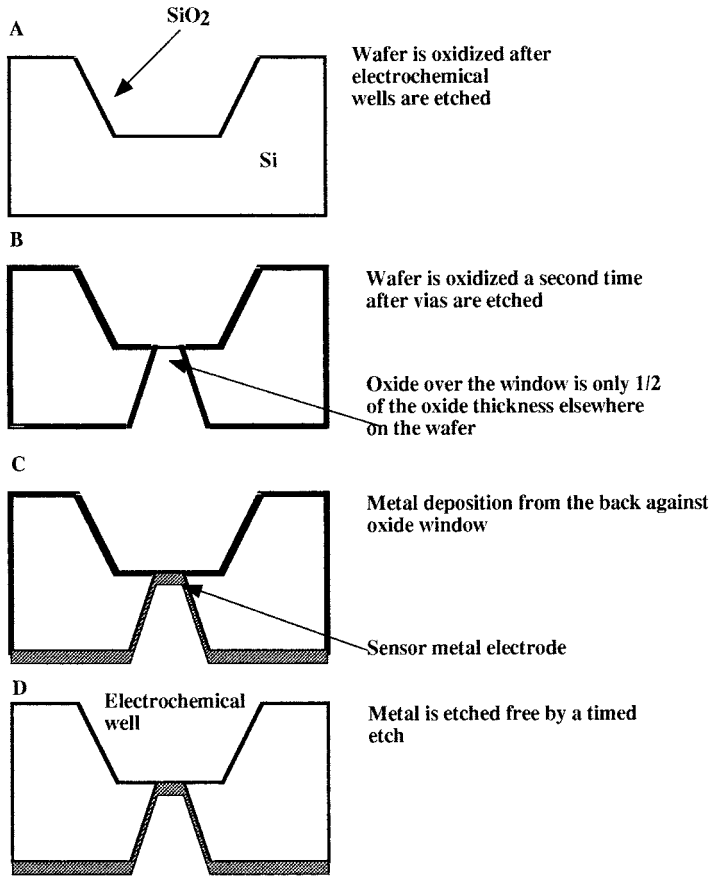


FIGURE 16.68 Fabrication sequence for a generic electrochemical cell in Si. Depth of the electrochemical well, number of electrodes and electrode materials can be varied.

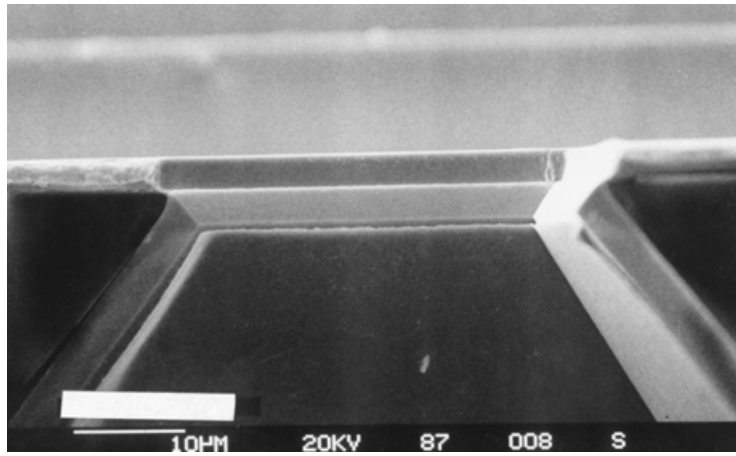


FIGURE 16.69 SEM micrograph illustrating process step D from Figure 16.67. A 30 × 30-µm Pt electrode is shown at the bottom of an electrochemical well. This Pt electrode is further contacted to the electronics from the back.

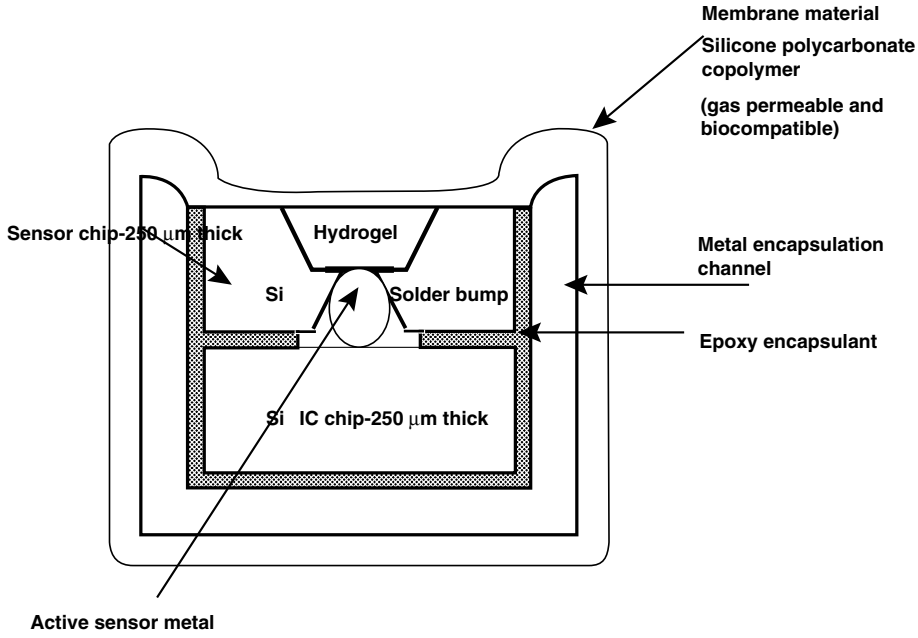


FIGURE 16.70 Schematic of the bonding scheme between sensor wafer and IC. The schematic is a cut-through of the catheter.

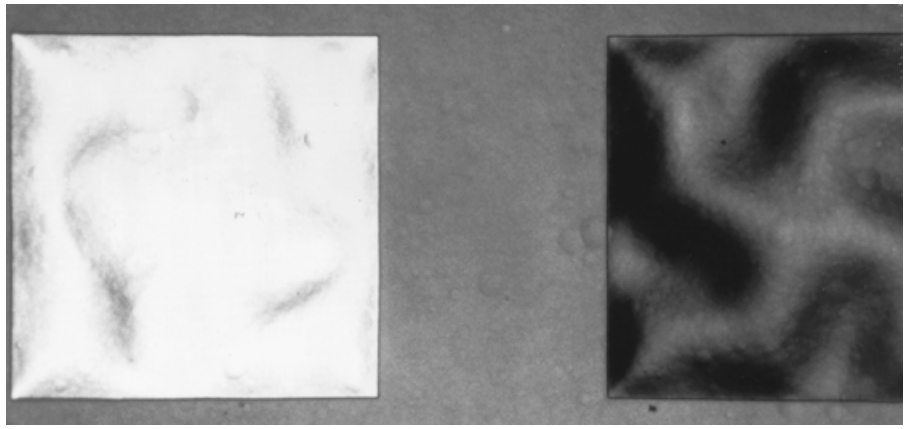


FIGURE 16.71 SEM micrograph of an Ag/AgCl (left) and an IrO_x (right) electrode at the bottom of an anisotropically etched well in Si. This electrochemical cell forms the basis for a Severinghaus CO_2 sensor.

protection for the electronics from the electrolyte as well as from the electronics, and chemical sensor manufacture can proceed independently. Depending on the type of sensor element, one or more electrodes are fabricated at the bottom of the electrochemical cells. For example, shown in Figure 16.71 is an almost completed (Severinghaus) CO_2 sensor with an Ag/AgCl electrode as the reference electrode (left in the figure) and an IrOx pH-sensitive electrode, both at the bottom of one electrochemical well. The metal electrodes are electrically isolated from each other by the SiO_2 passivation layer over the surface of the silicon wafer. To complete the CO_2 sensor, we silk-screen a hydrogel containing an electrolytic medium into the silicon sensor cavity and dip-coat the sensor into a silicone-polycarbonate rubber solution to form the gas-permeable membrane. For hydrogel inside the micromachined well, we use poly(2-hydroxyethyl)methacrylate (PHEMA) or polyvinylalcohol (PVA).

The concept of putting the sensor chemistries and the electronics on opposite sides of a substrate is a very important design feature we decided upon several years ago in view of the overwhelming problems encountered in building chemical sensors based on ISFETs or EGFETs [Madou and Morrison, 1989].

16.10 Surface Micromachining: Introduction

Bulk micromachining means that three-dimensional features are etched into the bulk of crystalline and noncrystalline materials. In contrast, surface micromachined features are built up, layer by layer, on the surface of a substrate (e.g., a single crystal silicon wafer). Dry etching defines the surface features in the x,y plane and wet etching releases them from the plane by undercutting. In surface micromachining, shapes in the x,y plane are unrestricted by the crystallography of the substrate. For illustration, in Figure 16.72 we compare an absolute pressure sensor based on poly-Si and made by surface micromachining with one made by bulk micromachining in single crystal Si.

The nature of the deposition processes involved determines the very flat surface micromachined features (Hal Jerman from EG&G's ICSensors called them 2.5 D features [Jerman, 1994]). Specifically, low-pressure chemical vapor deposited (LPCVD) polycrystalline silicon (poly-Si) films generally are only a few microns high (low z). In contrast with wet bulk micromachining only the wafer thickness limits the feature height. A low z may mean a drawback for some sensors. For example, it will be difficult to fashion a large inertial mass

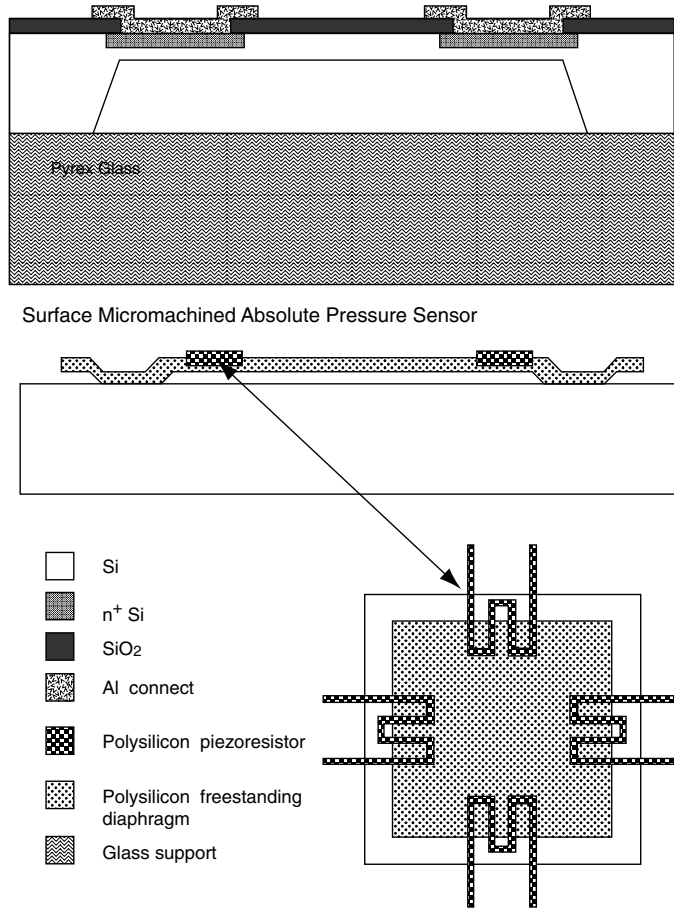


FIGURE 16.72 Comparison of bulk micromachined and surface micromachined absolute pressure sensors equipped with piezoresistive elements. (Top) Bulk micromachining in single crystal Si. (Bottom) Surface micromachining with poly-Si.

for an accelerometer from those thin poly-Si plates. Not only do many parameters in the LPCVD polysilicon process need to be controlled very precisely, subsequent high temperature annealing (say, at temperatures of about 580°C) is needed to transform the as-deposited amorphous silicon into polysilicon—the main structural material in surface micromachining. Even with the best possible process control, polysilicon has some material disadvantages over single crystal Si. For example, it generates a somewhat smaller yield strength (values between 2 and 10 times smaller have been reported) [Biebl and von Philipsborn, 1993; Greek et al., 1995] and has a lower piezoresistivity [Le Berre et al., 1996]. Moreover, since a grain diameter may constitute a significant fraction of the thickness of a mechanical member, the effective Young's modulus may exhibit significant variability from sensor to sensor [Howe, 1995]. An important positive attribute of poly-Si is that its material properties, although somewhat inferior to single crystal, are far superior compared to those of metal films, and, most of all, since they are isotropic, design is rendered dramatically simpler than with single crystal material. Dimensional uncertainties are of greater concern than material issues. Although absolute dimensional tolerances obtained with lithography techniques may be submicron, relative tolerances are poor, perhaps 1% on the length of a 100-μm-long feature. The situation becomes critical with yet smaller feature sizes [Madou, 1997, chap. 7, Figure 7.1]. Although the relatively coarse dimensional control in the microdomain is not specific to surface micromachining, there is no crystallography to rely on for improved dimensional control as in the case of wet bulk micromachining. Moreover, since the mechanical members in surface micromachining tend to be smaller, more post-fabrication adjustment of the features is required to achieve reproducible characteristics. Finally, the wet process for releasing structural elements from a substrate tends to cause sticking of suspended structures to the substrate, so-called stiction, introducing another disadvantage associated with surface micromachining.

Some of the mentioned problems associated with surface micromachining have recently been resolved by process modifications and/or alternative designs, and the technique has rapidly gained commercial interest, mainly because it is the most IC-compatible micromachining process developed to date. Moreover, in the last 5 to 10 years, processes such as silicon on insulator (SOI) [Diem et al., 1993], hinged poly-Si [Pister, 1992], Keller's molded milli-scale polysilicon [Keller and Ferrari, 1994], thick poly-Si (10 μm and beyond) [Lange et al., 1995], as well as LIGA[1] and LIGA-like processes, have further enriched the surface micromachining arsenal. Some preliminary remarks on each of these surface micromachining extensions follow.

Silicon crystalline features, anywhere between fractions of a micron to 100 μm high, can readily be obtained by surface micromachining of the epi-silicon or fusion-bonded silicon layer of SOI wafers [Noworolski et al., 1995]. Structural elements made from these single crystalline Si layers result in more reproducible and reliable sensors. SOI machining combines the best features of surface micromachining (i.e., IC compatibility and freedom in x,y shapes) with the best features of bulk micromachining (superior single crystal Si properties). Moreover, SOI surface micromachining frequently involves fewer process steps and offers better control over the thickness of crucial building blocks. Given the poor reproducibility of mechanical properties and generally poor electronic characteristics of polysilicon films, SOI machining may surpass the poly-Si technology for fabricating high performance devices.

The fabrication of poly-Si planar structures for subsequent vertical assembly by mechanical rotation around micromachined hinges dramatically increases the plethora of designs feasible with poly-Si [Pister, 1992]. Today, erecting these poly-Si structures with the probes of an electrical probe station or, occasionally, assembly by chance in the HF etch or DI water rinse [Chu et al., 1995] represents too complicated or unreliable postrelease assembly methods for commercial acceptance.

At the University of California at Berkeley, Keller introduced a combination of surface micromachining and LIGA-like molding processes [Keller and Ferrari, 1994] in the so-called HEXSIL[2] process, a technology enabling the fabrication of tall three-dimensional microstructures without postrelease assembly. Using CVD processes one can generally only deposit thin films (~2 to 5 μm) on flat surfaces. If however, these surfaces are the opposing faces of deep narrow trenches, the growing films will merge to form solid beams. Releasing

[1] LIGA is the acronym for the German Lithographie, Galvanoformung, Abformung (see chap. 17).

[2] HEXSIL is the acronym for HEXagonal honeycomb polySILicon.

of such polysilicon structures and the incorporation of electroplating steps expand the surface micromachining bandwidth in terms of choice of materials and accessible feature heights. In this fashion, high aspect ratio structures normally associated with LIGA can now also be made of CVD polysilicon.

Applying classical LPCVD to obtain poly-Si deposition is a slow process. For example, a layer of 10 μm typically requires a deposition time of 10 hours. Consequently, most micromachined structures are based on layer thicknesses in the 2- to 5-μm range. Based on dichlorosilane (SiH_2Cl_2) chemistry, Lange et al. (1995) developed a CVD process in a vertical epitaxy batch reactor with deposition rates as high as 0.55 μm/min at 1000°C. The process yields acceptable deposition times for thicknesses in the 10-μm range. The highly columnar poly-Si films were deposited on sacrificial SiO_2 layers and exhibit low internal tensile stress making them suitable for surface micromachining.

Finally, thick layers of polyimide and other new UV resists also receive a lot of attention as important new extensions of surface micromachining. Due to their transparency to exposing UV light, they can be transformed into tall surface structures with LIGA-like high aspect ratios. They may be both electroplated and molded.

In this part of the chapter, we first review thin film material properties in general, focusing on significant differences with bulk properties of the same material, followed by a review of the main surface micromachining processes. Next, we clarify the recent extensions of the surface micromachining technique listed above. Because of the complexity of the many parameters influencing thin film properties, we then present a set of case studies on the most commonly used thin film materials.

In the surface micromachining examples at the end of this chapter, we first look at a lateral resonator. Resonators have found an important industrial application in accelerometers introduced by Analog Devices. The other example concerns a micromotor: an electrostatic linear motor with a slider stepping between two poly-Si rails. Micromotors may lack practical use as of yet, but, just as the ion-sensitive field effect transistor (ISFET) galvanized the chemical sensor community in trying out new chemical sensing approaches, micromotors energized the micromachining research community to fervently explore miniaturization of a wide variety of mechanical sensors and actuators. Micromotors also brought about the christening of the micromachining field into 'Microelectromechanical Systems' or MEMS.

16.11 Historical Note

The first example of a surface micromachine for an electro-mechanical application consisted of an underetched metal cantilever beam for a resonant gate transistor made by Nathanson (1967). By 1970, a first suggestion for a magnetically actuated metallic micromotor emerged [Dutta, 1970]. Because of fatigue problems metals rarely are counted on as mechanical components. The surface micromachining method as we know it today was first demonstrated by Howe and Muller in the early 1980s and relied on polysilicon as the structural material [Howe and Muller, 1982]. These pioneers and Guckel [Guckel and Burns, 1985], an early contributor to the field, produced free-standing LPCVD polysilicon structures by removing the oxide layers on which the polysilicon features were formed. Howe's first device consisted of a resonator designed to measure the change of mass upon adsorption of chemicals from the surrounding air. A gas sensor does not necessarily represent a good application of a surface micromachined electrostatic structure since humidity and dust foul the thin air gap of such an unencapsulated microstructure in a minimal amount of time. Later mechanical structures, especially hermetically sealed mechanical devices, provided proof that the IC revolution could be extended to electromechanical systems [Howe, 1995]. In these structures, the height (z-direction) typically is limited to less than 10 μm, ergo the name surface micromachining.

The first survey of possible applications of poly-Si surface micromachining was presented by Gabriel et al. (1989). Microscale movable mechanical pin joints, springs, gears, cranks, sliders, sealed cavities and many other mechanical and optical components have been demonstrated in the laboratory [Muller, 1987; Fan et al., 1987]. In 1991, Analog Devices announced the first commercial product based on surface micromachining, namely, the ADXL-50, a 50-g accelerometer for activating air-bag deployment [Editor, 1991]. A new wave of major commercial applications for surface micromachining could be based on

Texas Instruments' Digital Micromirror Device™. This surface micromachined movable mirror is a digital light switch that precisely controls a light source for projection display and hard copy applications [Hornbeck, 1995]. The commercial acceptance of this application will likely determine the staying power of the surface micromachining option.

16.12 Mechanical Properties of Thin Films

16.12.1 Introduction

Thin films in surface micromachines must satisfy a large set of rigorous chemical, structural, mechanical and electrical requirements. Excellent adhesion, low residual stress, low pinhole density, good mechanical strength and chemical resistance all may be required simultaneously. For many microelectronic thin films, the material properties depend strongly on the details of the deposition process and the growth conditions. In addition, some properties may depend on post-deposition thermal processing, referred to as annealing. Furthermore, the details of thin-film nucleation and/or growth may depend on the specific substrate or on the specific surface orientation of the substrate. Although the properties of a bulk material might be well characterized, its thin-film form may have properties substantially different from those of the bulk. For example, thin films generally display smaller grain size than bulk materials. An overwhelming reason for the many differences stem from the properties of thin films, which exhibit a higher surface-to-volume ratio than large chunks of material and are strongly influenced by the surface properties.

For more details on deposition techniques in general, refer to Madou (1997, chap. 3); now we focus on the physical characteristics of the resulting thin deposits. Some terminology characterizing thin films and their deposition is introduced in Table 16.11.

Since thin films were not intended for load-bearing applications, their mechanical properties have largely been ignored. The last 10 years saw the development of a strong appreciation for understanding the mechanical properties as essential for improving the reliability and life-time in thin films, even in nonstructural applications [Vinci and Braveman, 1991]. Surface micromachining contributes heavily to this understanding. One of the most influential long-term contributions of surface micromachining might well lie in the elucidation of stress mechanism in thin films.

16.12.2 Adhesion

One cannot stress enough the importance of adhesion of various films to one another and to the substrate in overall IC performance and reliability. As mechanical pulling forces might be involved, adhesion is even more crucial in micromachining. If films lift from the substrate under a repetitive, applied mechanical force, the device will fail. Classical adhesion tests include the scotch tape test, abrasion method, scratching, deceleration (ultrasonic and ultracentrifuge techniques), bending, pulling etc. [Campbell, 1970]. Micromachined structures, because of their sensitivity to thin-film properties, enable some innovative new ways of *in situ* adhesion measurement. Figure 16.73 illustrates how a suspended membrane may be used for adhesion measurements. Figure 16.73A shows the membrane suspended but still adherent to the substrate. Figure 16.73B shows the membrane after it has been peeled from its substrate by an applied load (gas pressure). Figure 16.73C illustrates the accompanying P(ressure)-V(olume) cycle, in which the membrane is inflated, peeled and then deflated. The shaded portion of Figure 16.73C illustrates the P-V work creating the new surface, which equals the average work of adhesion for the film-substrate interface times the area peeled during the test [Senturia, 1987].

Cleanliness of a substrate is a *condition sine qua non* for good film adhesion. Roughness, providing more bonding surface area and mechanical interlocking further improve it. Adhesion also improves with increasing adsorption energy of the deposit and/or increasing number of nucleation sites in the early growth stage of the film. Sticking energies between film and substrate range from less than 10 kcal/mole in physisorption to more than 20 kcal/mole for chemisorption. The weakest form of adhesion involves van der Waals forces only (see also Table 16.11).

TABLE 16.11 Thin Film Terms Used in Characterizing Deposition

Term	Remark
Physisorbed film	Bond energy < 10 kcal/mole
Chemisorbed film	Bond energy > 20 kcal/mole
Nucleation	Adatoms forming stable clusters
Condensation	Initial formation of nuclei
Island formation	Nuclei grow in three dimensions, especially along the substrate surface
Coalescence	Nuclei contact each other and larger, rounded shapes form
Secondary nucleation	Areas between islands are filled in by secondary nucleation, resulting in a continuous film
Grain size of thin film	Generally smaller than for bulk materials and function of deposition and annealing conditions (higher T, larger grains)
Surface roughness	Lower at high temperatures except when crystallization starts; at low temperature the roughness is higher for thicker films; also oblique deposition and contamination increase roughness
Epitaxial and amorphous films	Very low surface roughness
Density	More porous deposits are less dense; density reveals a lot about the film structure
Crystallographic structure	Adatom mobility: amorphous, polycrystalline, single crystal or fiber texture, or preferred orientation

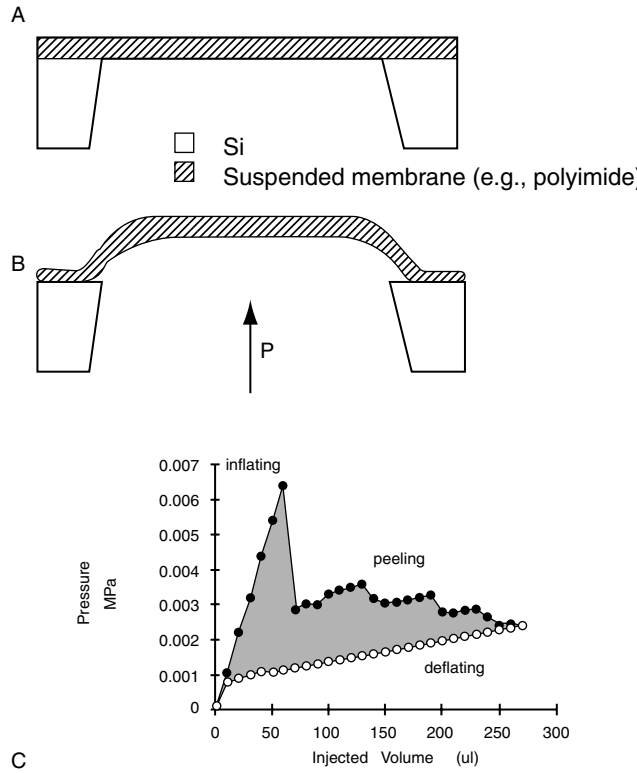


FIGURE 16.73 Micromachined structure to evaluate adhesion. (A) Suspended membrane. (B) Partially detached membrane-outward peel. (C) Pressure-volume curve during inflate-deflate cycle. (From Senturia, S., Can We Design Microrobotic Devices Without Knowing the Mechanical Properties of Materials?, presented at Micro Robots and Tekoperators Workshop, Hyannis, MA, 1987. With permission.)

It is highly advantageous to include a layer of oxide-forming elements between a metal and an oxide substrate. These adhesion layers, such as Cr, Ti, Al etc., provide good anchors for subsequent metallization. Intermediate film formation allowing a continuous transition from one lattice to the other results in the best adhesion. Adhesion also improves when formation of intermetallic metal alloys takes place.

16.12.3 Stress in Thin Films

16.12.3.1 Stress in Thin Films—Qualitative Description

Film cracking, delamination and void formation may all be linked to film stress. Nearly all films foster a state of residual stress, due to mismatch in the thermal expansion coefficient, nonuniform plastic deformation, lattice mismatch, substitutional or interstitial impurities and growth processes. Figure 16.74 lists stress-causing factors categorized as either intrinsic or extrinsic [Krulevitch, 1994]. The intrinsic stresses (also growth stresses) develop during the film nucleation. Extrinsic stresses are imposed by unintended external factors such as temperature gradients or sensor package-induced stresses. Thermal stresses, the most common type of extrinsic stresses, are well understood and often easy to calculate (see below). They arise either in a structure with inhomogeneous thermal expansion coefficients subjected to a uniform temperature change or in a homogeneous material exposed to a thermal gradient [Krulevitch, 1994]. Intrinsic stresses in thin films often are larger than thermal stresses. They usually are a consequence of the nonequilibrium nature of the thin-film deposition process. For example, in chemical vapor deposition, depositing atoms (adatoms) may at first occupy positions other than the lowest energy configuration. With too high a deposition rate and/or too low adatom surface mobility, these first adatoms may become pinned by newly arriving adatoms, resulting in the development of intrinsic stress. Other types of intrinsic stresses illustrated in Figure 16.74 include: transformation stresses occurring when part of a material under-

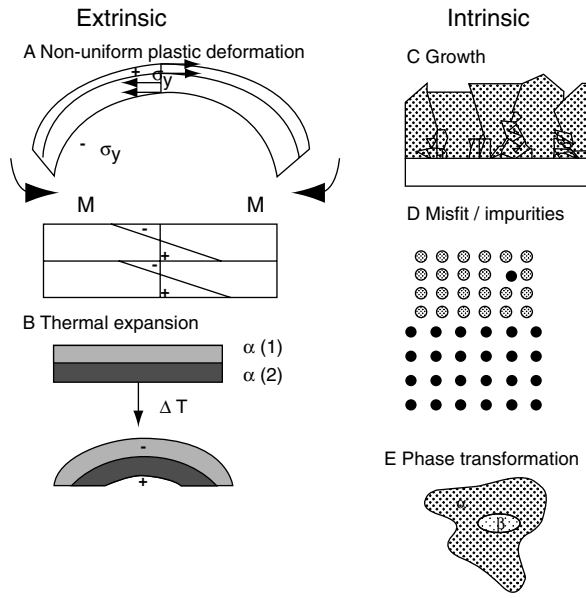


FIGURE 16.74 Examples of intrinsic and extrinsic residual stresses. (A) Nonuniform plastic deformation results in residual stresses upon unloading. M = bonding moment. (B) Thermal expansion mismatch between two materials bonded together. α (1) and α (2) are thermal expansion coefficients. (C) Growth stresses evolve during film deposition. (D) Misfit stresses due to mismatches in lattice parameters in an epitaxial film and stresses from substitutional or interstitial impurities. (E) Volume changes accompanying phase transformations cause residual stresses [Vinci and Braveman, 1991]. (After Krulevitch, P.A., Micromechanical Investigations of Silicon and Ni-Ti-Cu Thin Films, Ph.D. thesis, University of California, Berkeley, 1994.)

goes a volume change during a phase transformation, misfit stresses arising in epitaxial films due to lattice mismatch between film and substrate, and impurities either interstitial or substitutional which cause intrinsic residual stresses due to the local expansion or contraction associated with point defects. Intrinsic stress in a thin film does not suffice to result in delamination unless the film is quite thick. For example, to overcome a low adsorption energy of 0.2 eV, a relatively high stress of about 5×10^9 dyn cm^{-2} (10^7 dyn/cm^2 = 1 MPa) is required [Campbell, 1970]. High stress can result in buckling or cracking of films.

The stress developing in a film during the initial phases of a deposition may be compressive (i.e., the film tends to expand parallel to the surface), causing buckling and blistering or delamination in extreme cases (especially with thick films). Alternatively, thin films may be in tensile stress (i.e., the film tends to contract), which may lead to cracking if forces high enough to exceed the fracture limit of the film material are present. Subsequent rearrangement of the atoms, either during the remainder of the deposition or with additional thermal processing, can lead to further densification or expansion, decreasing remaining tensile or compressive stresses, respectively.

The mechanical response of thin-film structures is affected by the residual stress, even if the structures do not fail. For example, if the residual stress varies in the direction of film growth, the resulting built-in bending moment will warp released structures, such as cantilever beams. The presence of residual stress also alters the resonant frequency of thin-film, resonant microstructures (see Eq. (16.59) below) [Pratt et al., 1992]. Also, residual stress can lead to degradation of electrical characteristics and yield loss through defect generation, such as {311} defects [Krulevitch, 1994]. Another observation found the resistivity of stressed metallic films to be higher than that of their annealed counterparts. In a few cases residual stress has been used advantageously, such as in self-adjusting microstructures [Judy et al., 1991], and for altering the shape-set configuration in shape memory alloy films [Krulevitch, 1994].

In general, the stresses in films, by whatever means produced, are in the range of 10^8 to 5×10^{10} dyn/cm^{-2} and can be either tensile or compressive. For normal deposition temperatures (50 to a few hundred degrees C), the stress in metal films typically ranges from 10^8 to 10^{10} dyn cm^{-2} and is tensile, the refractory metals at the upper end, the soft ones (Cu, Ag, Au, Al) at the lower end. At low substrate temperatures, metal films tend to exhibit tensile stress. This often decreases in a linear fashion with increasing substrate temperature, finally going through zero or even becoming compressive. The changeover to compressive stress occurs at lower temperatures for lower melting point metals. The mobility of the adatoms is key to understanding the ranking for refractory and soft metals. A metal such as aluminum has a low melting temperature and a corresponding high diffusion rate even at room temperature, thus usually it is fairly stress free. By comparison, tungsten has a relatively high melting point and a low diffusion rate and tends to accumulate more stress when sputter-deposited. With dielectric films, stresses often are compressive and have slightly lower values than commonly noted in metals.

Tensile films result, for example, when a process by-product is present during deposition and later driven off as a gas. If the deposited atoms are not sufficiently mobile to fill in the holes left by these departing byproducts, the film will contract and go in tension. Nitrides deposited by plasma CVD usually are compressive due to the presence of hydrogen atoms in the lattice. By annealing, driving the hydrogen out, the films can turn highly tensile. Annealing also has a dramatic effect on most oxides. Oxides often are porous enough to absorb or give off a large amount of water. Full of water, they are compressive; devoid of water they are tensile. Thermal SiO_2 is compressive, though, even when dry. If atoms are jammed in place (such as with sputtering) the film tends to act compressively. The stress in a thin film also varies with depth. The RF power of a plasma-enhanced CVD (PECVD) deposition influencss stress, e.g., a thin film may start out tensile, decrease as the power increases, and finally become compressive with further RF power increase. CVD equipment manufacturers concentrate on building stress-control capabilities into new equipment by controlling plasma frequency (see also Madou [1997, chap. 3]).

16.12.3.2 Stress in Thin Films on Thick Substrates—Quantitative Analysis

The total stress in a thin film typically is given by:

$$\sigma_{tot} = \sigma_{th} + \sigma_{int} + \sigma_{ext} \tag{16.44}$$

i.e., the sum of any intentional external applied stress (σ_{ext}), the thermal stress (σ_{th}, an unintended external stress) and different intrinsic components (σ_{int}). With constant stress through the film thickness, the stress components retain the form of

$$\begin{aligned} \sigma_x &= \sigma_x(x, y) \\ \sigma_y &= \sigma_y(x, y) \\ \tau_{xy} &= \tau_{xy}(x, y) \\ \tau_{xz} &= \tau_{yz} = \sigma_z = 0 \end{aligned} \tag{16.45}$$

That is, the three nonvanishing stress components are functions of x and y alone. No stress occurs in the direction normal to the substrate (z). With x, y as principal axes, the shear stress τ_{xy} also vanishes [Chou and Pagano, 1967] and Eq. (16.45) reduces to the following strain–stress relationships:

$$\begin{aligned} \varepsilon_x &= \frac{\sigma_x}{E} - \frac{\nu\sigma_y}{E} \\ \varepsilon_y &= \frac{\sigma_y}{E} - \frac{\nu\sigma_x}{E} \\ \sigma_z &= 0 \end{aligned} \tag{16.46}$$

In the isotropic case $\varepsilon = \varepsilon_x = \varepsilon_y$ so that $\sigma_x = \sigma_y = \sigma$, or:

$$\sigma = \left(\frac{E}{1-\nu}\right)\varepsilon \tag{16.47}$$

where the Young's modulus of the film and the Poissons's ratio of the film act independently of orientation. The quantity $E/1 - \nu$ often is called the biaxial modulus. Uniaxial testing of thin films is difficult, prompting the use of the biaxial modulus, rather than Young's uniaxial modulus. Plane stress, as described here, presents a good approximation several thicknesses away from the edge of the film (say, three thicknesses from the edge).

Thermal Stress

Thermal stresses develop in thin films when high temperature deposition or annealing are involved, and usually are unavoidable due to mismatch of thermal expansion coefficients between film and substrate. The problem of a thin film under residual thermal stress can be modeled by considering a thought experiment involving a stress-free film at high temperature on a thick substrate. Imagine detaching the film from the high-temperature substrate and cooling the system to room temperature. Usually, the substrate dimensions undergo minor shrinkage in the plane while the film's dimensions may reduce significantly. In order to reapply the film to the substrate with complete coverage, the film needs stretching with a biaxial tensile load to a uniform radial strain ε, followed by perfect bondage to the rigid substrate and load removal. The film stress is assumed to be the same in the stretched and free-standing film as in the film bonded to the substrate, i.e., no relaxation occurs in the bonding process. To calculate the thermal residual stress from Eq. (16.47) the elastic moduli of the film must be known, as well as the volume change associated with the residual stress, i.e., the thermal strain, ε_{th}, resulting from the difference in the coefficients of thermal expansion between the film and the substrate.

Let us now consider whether, qualitatively, the above assumptions apply to the measurement of thin films on Si wafers. Such films typically measure 1 μm thick and are deposited on 4-in. wafers nominally

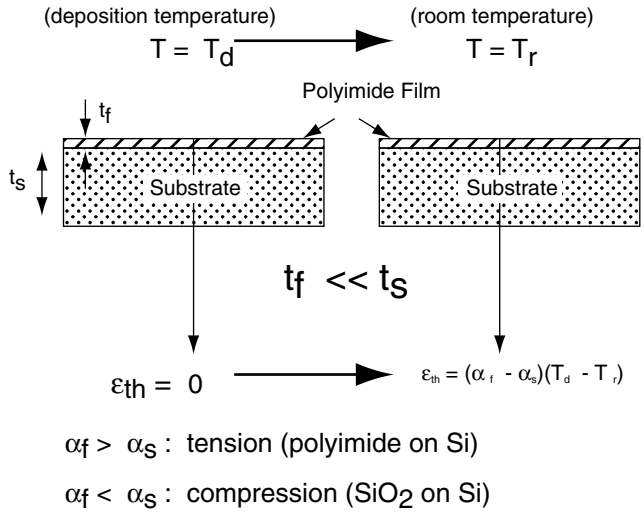


FIGURE 16.75 Thermal stress. Tension and compression are determined by the relative size of thermal expansion coefficients of film and substrate. Suppose a strain-free film at deposition temperature, T_d, is cooled to room temperature, T_r, on a substrate with a different coefficient of thermal expansion.

550 μm thick. In this case, the substrate measures nearly three orders of magnitude thicker than the film, and, because the bending stiffness is proportional to the thickness cubed, the substrate essentially is rigid relative to the film. The earlier assumptions clearly apply.

Figure 16.75 portrays a quantitative example where a polyimide film, strain-free at the deposition temperature (T_d) of 400°C, is cooled to room temperature T_r (25°C) on an Si substrate with a different coefficient of thermal expansion. The resulting strain is given by:

$$\varepsilon_{th} = \int (\alpha_f(T) - \alpha_s(T))\, dt \tag{16.48}$$

where α_f and α_s represent the coefficients of thermal expansion for the polyimide film and the Si substrate, respectively. The thermal strain can be of either sign, based on the relative values of α_f and α_s: positive is tensile, negative is compressive. Polyimide features a thermal expansion ($\alpha_f = 70 \times 10^{-6}°C^{-1}$) larger than the thermal expansion coefficient of Si ($\alpha_s = 2.6 \times 10^{-6}°C^{-1}$); hence, a tensile stress is expected. With SiO_2 grown or deposited on silicon at elevated temperatures, a compressive component [α_f ($0.35 \times 10^{-6}°C^{-1}$) < α_s ($2.6 \times 10^{-6}°C^{-1}$)] is expected. Assuming that the coefficients of thermal expansion are temperature independent, Eq. (16.48) simplifies to:

$$\varepsilon_{th} = (\alpha_f - \alpha_s)(T_d - T_r) \tag{16.49}$$

The calculated thermal strain ε_{th} for polyimide on Si then measures 25×10^{-3} at room temperature. The biaxial modulus ($E/1 - \nu$), with $E = 3$ GPa and $\nu = 0.4$, equals 5 GPa, and the residual stress σ, from Eq. (16.47), is 125 MPa and tensile.

Intrinsic Stress

The intrinsic stress, σ_i, reflects the internal structure of a material and is less clearly understood than the thermal stress which it often dominates [Guckel et al., 1988]. Several phenomena may contribute to σ_i, making its analysis very complex. Intrinsic stress depends on thickness, deposition rate (locking in defects), deposition temperature, ambient pressure, method of film preparation, type of substrate used (lattice mismatch), incorporation of impurities during growth etc. Some semiquantitative descriptions of various intrinsic stress-causing factors follow:

- Doping ($\sigma_{int} > 0$ or $\sigma_{int} < 0$): When doping Si, the atomic or ionic radius of the dopant and the substitutional site determine the positive or negative intrinsic stress ($\sigma_{int} > 0$ or tensile, and $\sigma_{int} < 0$ or compressive). With boron-doped poly-Si, an atom small compared to Si, the film is expected to be tensile ($\sigma_{int} > 0$); with phosphorous doping, an atom large compared to Si, the film is expected to be compressive ($\sigma_{int} < 0$).
- Atomic peening ($\sigma_{int} < 0$): Ion bombardment by sputtered atoms and working gas densifies thin films, rendering them more compressive. Magnetron sputtered films at low working pressure (<1 Pa) and low temperature often exhibit compressive stress.
- Microvoids ($\sigma_{int} > 0$): Microvoids may arise when byproducts during deposition escape as gases and the lateral diffusion of atoms evolves too slowly to fill all the gaps, resulting in a tensile film.
- Gas entrapment ($\sigma_{int} < 0$): As an example we can cite the hydrogen trapped in Si_3N_4. Annealing removes the hydrogen, and a nitride film, compressive at first, may become tensile if the hydrogen content is sufficiently low.
- Shrinkage of polymers during cure ($\sigma_{int} > 0$): The shrinkage of polymers during curing may lead to severe tensile stress, as becomes clear in the case of polyimides. Special problems are associated with measuring the mechanical properties of polymers as they exhibit a time-dependent mechanical response (viscoelasticity), a potentially significant factor in the design of mechanical structures where polymers are subjected to sustained loads [Maseeh and Senturia, 1990].
- Grain boundaries ($\sigma_{int} = ?$): Based on intuition one expects that the interatomic spacing in grain boundaries differs depending on the amount of strain, thus contributing to the intrinsic stress. But the origin of, for example, the compressive stress in polysilicon and how it relates to the grain structure and interatomic spacing are not yet completely clear (see also below on coarse and fine-grated Si).

For further reading on thin-film stress, refer to Hoffman (1975; 1976).

16.12.3.3 Stress-Measuring Techniques

Introduction

A stressed thin film will bend a thin substrate by a measurable degree. A tensile stress will bend and render the surface concave; a compressive stress renders the surface convex. The most common methods for measuring the stress in a thin film are based on this substrate bending principle. The deformation of a thin substrate due to stress is measured either by observing the displacement of the center of a circular disk or by using a thin cantilevered beam as a substrate and calculating the radius of curvature of the beam and hence the stress from the deflection of the free end. More sophisticated local stress measurements use analytical tools such as X-ray [Wong, 1978], acoustics, Raman spectroscopy [Nishioka et al., 1985], infrared spectroscopy [Marco et al., 1991], and electron-diffraction techniques. Local stress does not necessarily mean the same as the stress measured by substrate bending techniques, since stress is defined microscopically, while deformations are induced mostly macroscopically. The relation between macroscopic forces and displacements and internal differential deformation, therefore, must be modeled carefully. Local stress measurements may also be made using *in situ* surface micromachined structures such as strain gauges made directly out of the film of interest itself [Mehregany et al., 1987]. The deflections of thin suspended and pressurized micromachined membranes may be measured by mechanical probe [Jaccodine and Schlegel, 1966], laser [Bromley et al., 1983], or microscope [Allen et al., 1987]. Intrinsic stress influences the frequency response of microstructures (see Eq. (16.59)) which can be measured by laser [Zhang et al., 1991], spectrum analyzer [Pratt et al., 1991], or stroboscope. Whereas residual stress can be determined from wafer curvature and microstructure deflection data, material structure of the film can be studied by X-ray diffraction and transmission electron microscopy (TEM). Krulevitch, among others, attempted to link the material structure of poly-Si and its residual strain [Krulevitch, 1994]. Following, we will review stress-measuring techniques, starting with the more traditional ones and subsequently clarifying the problems and opportunities in stress measuring with surface micromachined devices.

Disk Method

For all practical purposes only stresses in the x and y directions are of interest in determining overall thin-film stress, as a film under high stress can only expand or contract by bending the substrate and deforming it in a vertical direction. Vertical deformations will not induce stresses in a substrate because it freely moves in that direction. The latter condition enables us to obtain quite accurate stress values by measuring changes in bow or radius of curvature of a substrate. The residual stresses in thin films are large and sensitive optical or capacitive gauges may measure the associated substrate deflections.

The disk method, most commonly used, is based on a measurement of the deflection in the center of the disk substrate (say, a Si wafer) before and after processing. Since any change in wafer shape is directly attributable to the stress in the deposited film, it is relatively straightforward to calculate stress by measuring these changes. Stress in films using this method is found through the Stoney equation [Hoffman, 1976], relating film stress to substrate curvature:

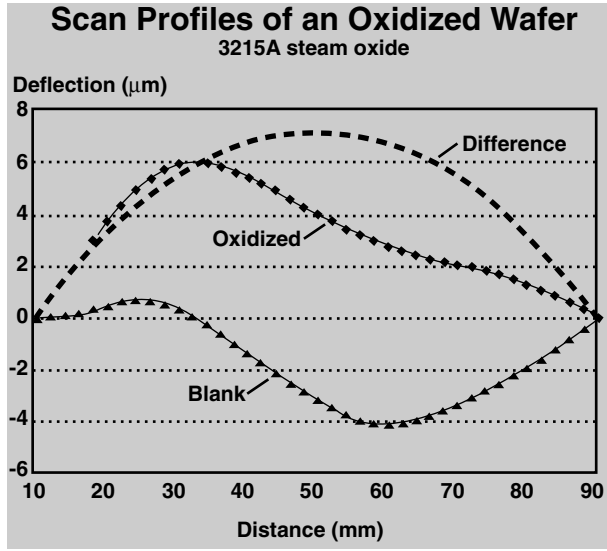
$$\sigma = \frac{1}{R}\frac{E}{6(1-\nu)}\frac{T^2}{t} \tag{16.50}$$

where R represents the measured radius of curvature of the bent substrate, $E/(1-\nu)$ the biaxial modulus of the substrate, T the thickness of the substrate, and t the thickness of the applied film [Singer, 1992]. The underlying assumptions include:

- The disc substrate is thin and has transversely isotropic elastic properties with respect to the film normal.
- The applied film thickness is much less than the substrate thickness.
- The film thickness is uniform.
- Temperature of the disk substrate/film system is uniform.
- Disc substrate/film system is mechanically free.
- Disc substrate without film has no bow.
- Stress is equi-biaxial and homogeneous over the entire substrate.
- Film stress is constant through the film thickness.

For most films on Si we assume that $t \leq T$; for example, t/T measures $\sim 10^{-3}$ for thin films on Si. The legitimacy of the uniform thickness, homogeneous, and equi-biaxial stress assumptions depend on the deposition process. Chemical vapor deposition (CVD) is such a widely used process as it produces relatively uniform films; however, sputter-deposited films can vary considerably over the substrate. In regard to the assumption of stress uniformity with film thickness, residual stress can vary considerably through the thickness of the film. Eq. (16.50) only gives an average film stress in such cases. In cases where thin films are deposited onto anisotropic single crystal substrates, the assumption of a substrate with transversely isotropic elastic properties with respect to the film normal is not always satisfied. Using single crystal silicon substrates possessing moderately anisotropic properties (Eq. (16.20)) (<100>- or <111>-oriented wafers) satisfies the transverse isotropy argument. Any curvature inherent in the substrate must be measured before film deposition and algebraically added to the final measured radius of curvature. To give an idea of the degree of curvature, 1 μm of thermal oxide may cause a 30-μm warp of a 4-in. silicon wafer, corresponding to a radius of curvature of 41.7 m.

Presently, five companies offer practical disk method-based instruments to measure stress on wafers: ADE Corp. (Newton, MA), GCA/Tropel (Fairport, NY), Ionic Systems (Salinas, CA), Scientific Measurements Systems, Inc. (San Jose, CA), and Tencor Instruments (Mountain View, CA) [Singer, 1992]. Figure 16.76A illustrates the sample output from Tencor's optical stress analysis system. Figure 16.76B represents the measuring principle of Ionic Systems' optical stress analyzer. None of the above tech-



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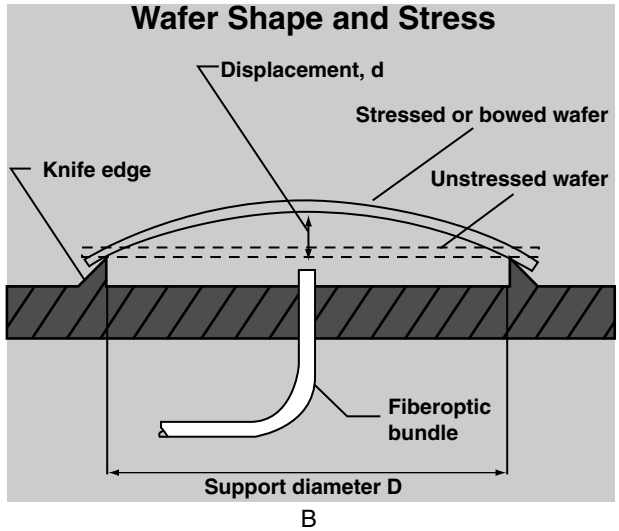


B

FIGURE 16.76 Curvature measurement for stress analysis. (A) Sample output from Tencor's FLX stress analysis instrument, showing how stress is derived from changes in wafer curvature. (B) The reflected light technique, used by Ionic Systems to measure wafer curvature. (From Singer, P., *Semicond. Int.*, 15, 54–58, 1992. With permission.)

niques satisfies the need for measuring stress in low modulus materials such as polyimide. For the latter applications the suspended membrane approach (see below) is more suited.

Uniaxial Measurements of Mechanical Properties of Thin Films

Many problems associated with handling thin films in stress test equipment may be bypassed by applying micromachining techniques. One simple example of problems encountered with thin films is the measurement of uniaxial tension to establish the Young's modulus. This method, effective for macroscopic samples, proves problematic for small samples. The test formula is illustrated in Figure 16.77A. The gauge length L in this figure represents the region we allow to elongate and the area A (=W × H) is the cross section of the specimen. A stress F/A is applied and measured with a load cell; the strain δL/L is measured

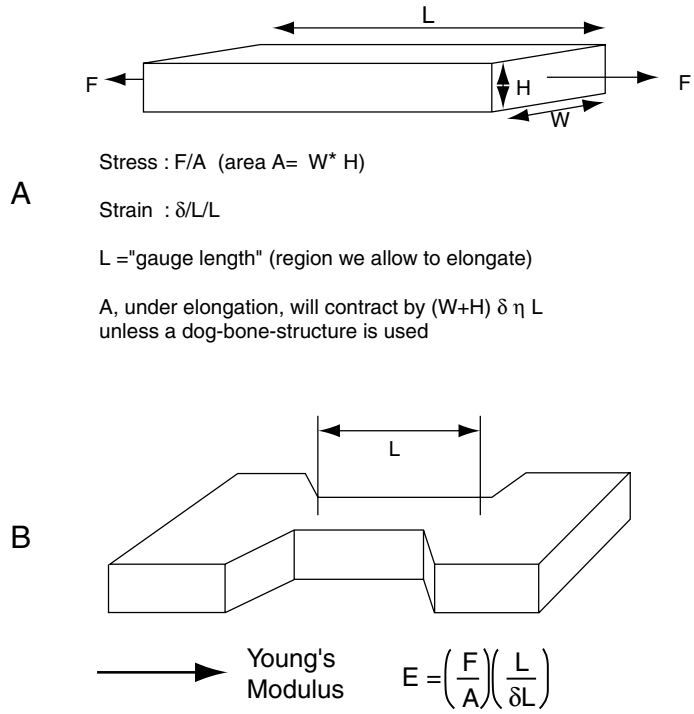


FIGURE 16.77 Measuring Young's modulus. (A) With a bar-shaped structure. (B) With a dog-bone, Instron specimen. (After Senturia and Howe, 1990.)

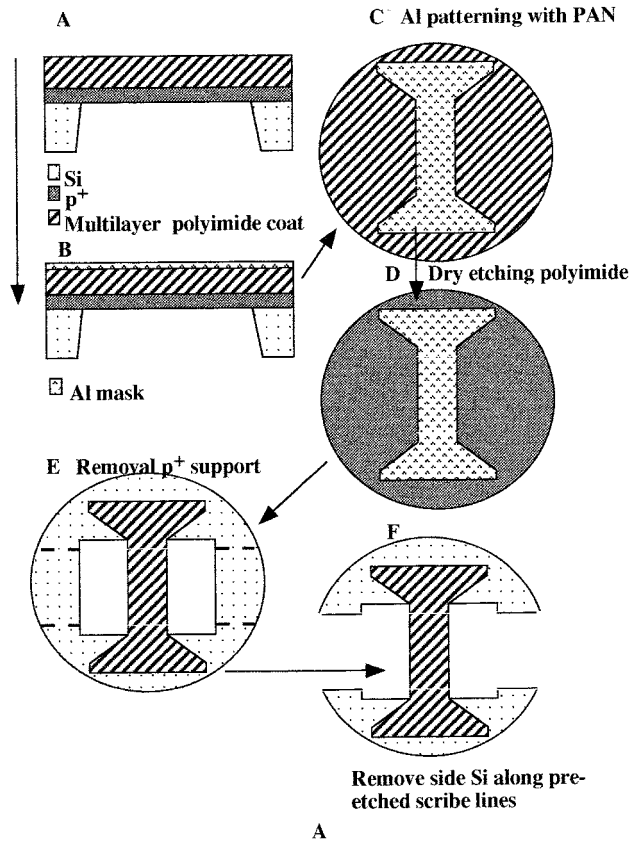
with an LVDT or another displacement transducer (a typical instrument used is the Instron 1123). The Young's modulus is then deduced from:

$$E = \left(\frac{F}{A}\right)\left(\frac{L}{\delta L}\right) \tag{16.51}$$

The obvious problem, for small or large samples, is how to grip onto the sample without changing A. Under elongation, A will indeed contract by $(w + H)\delta\nu L$. In general, making a dog-bone shaped structure (Instron specimen) solves that problem as shown in Figure 16.77B. Still, the grips introduced in an Instron sample can produce end effects and uncertainties in determining L. Making Instron specimens in thin films is even more of a challenge since the thin film needs to be removed from the surface, possibly changing the stress state, while the removal itself may modify the film.

As in the case of adhesion, some new techniques for testing stress in thin films, based on micromachining, are being explored. These microtechniques prove more advantageous than the whole wafer disc technique in that they are able to make local measurements.

The fabrication of micro-Instron specimens of thin polyimide samples is illustrated in Figure 16.78A. Polyimide is deposited on a p^+ Si membrane in multiple coats. Each coat is prebaked at 130°C for 15 min. After reaching the desired thickness the film is cured at 400°C in nitrogen for 1 hr (A). The polyimide is then covered with a 3000-Å layer of evaporated aluminum (B). The aluminum layer is patterned by wet etching (in phosphoric-acetic-nitric solution referred to as PAN etch) to the Instron specimen shape (C). Dry etching transfers the pattern to the polyimide (D). After removing the Al mask by wet etching, the p^+ support is removed by a wet isotropic etch (HNA) or a SF_6 plasma etch (E), and finally the side silicon is removed along four pre-etched scribe lines, releasing the residual stress (F). The remaining silicon acts as supports for the grips of the Instron [Meseeh-Tehrani, 1990]. The resulting structure can



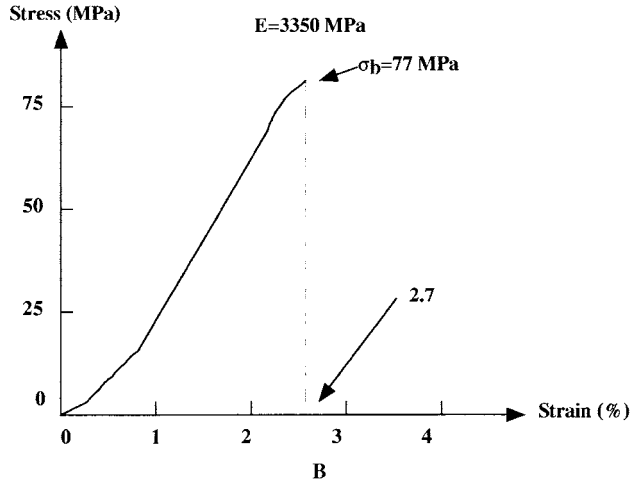


FIGURE 16.78 Uniaxial stress measurement. (A) Fabrication process of a dog bone sample for measurement of uniaxial strain. (B) Stress vs. strain for Du Pont's 2525 polyimide. (Courtesy of Dr. F. Maseeh-Tehrani.)

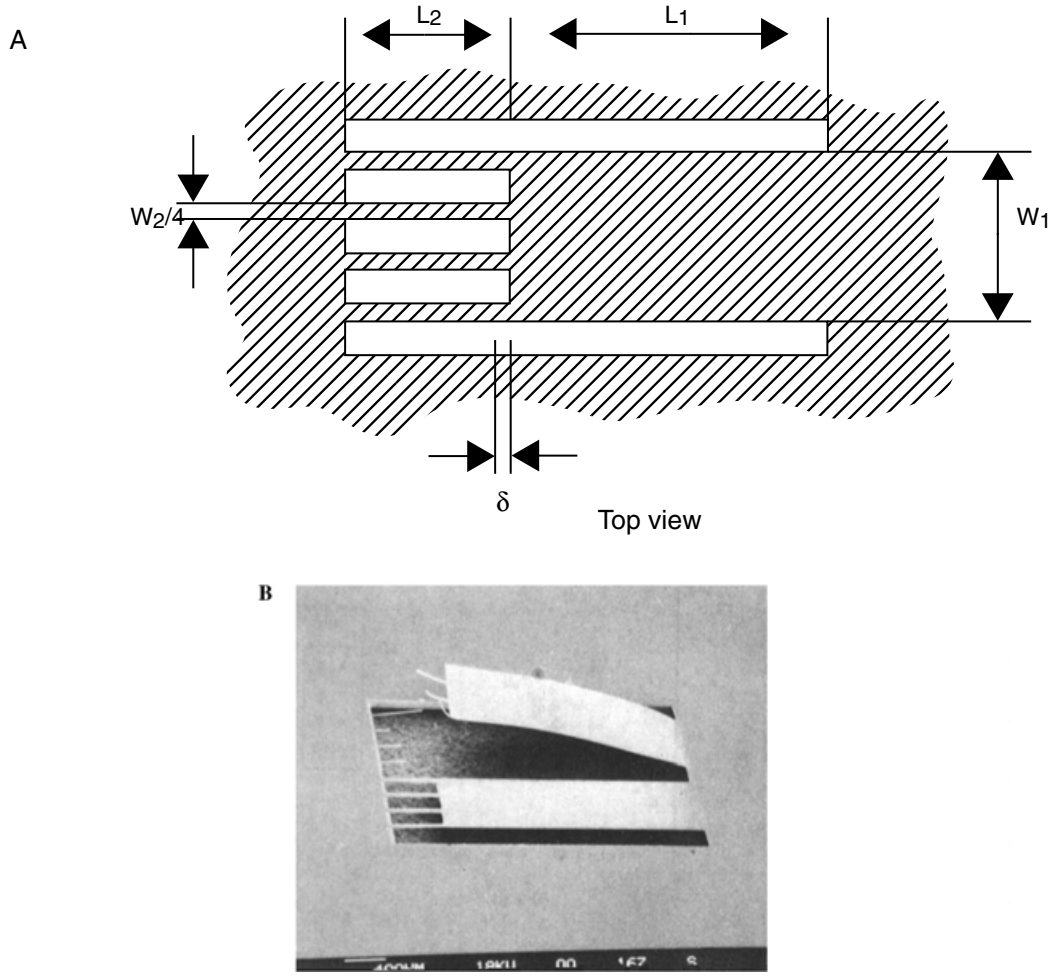


FIGURE 16.79 Ultimate strain. (A) Test structures for stress-to-modulus (strain) and ultimate stress measurements. (B) Two released structures, one of which has exceeded the ultimate strain of the film, resulting in fracture of the necks. (From Senturia, S., Can We Design Microbiotic Devices without Knowing the Mechanical Properties of the Materials?, presented at Micro Robots and Teleoperators Workshop, Hyannis, MA, 1987. With permission.)

be manipulated as any macrosample without the need for removal of the film from its substrate. This technique enables the gathering of stress/strain data for a variety of commercially available polyimides [Maseeh and Senturia, 1989]. A typical measurement result for Dupont's polyimide 2525, illustrated in Figure 16.78B, gives a break stress and strain of 77 MPa (σ_b) and 2.7% (ε_b), respectively, and 3350 MPa for the Young's modulus.

Figure 16.79A illustrates a micromachined test structure able to establish the strain and the ultimate stress of a thin film [Senturia, 1987]. A suspended rectangular polymer membrane is patterned into an asymmetric structure before removing the thin supporting Si. Once released, the wide suspended strip (width w_1) pulls on the thinner necks (total width w_2), resulting in a deflection δ from its original mask position toward the right to its final position after release. The residual tensile stress in the film drives the deformation δ as shown in Figure 16.79A. By varying the geometry, it is possible to create structures exhibiting small strain in the thinner sections as opposed to others that exceed the ultimate strain of the film. For structures where the strain is small enough to be modeled with linear elastic behavior, the deflection δ can be related to the strain as follows:

$$\varepsilon = \frac{\sigma}{E} = \frac{\delta\left(\frac{W_1}{L_1} + \frac{W_2}{L_2}\right)}{W_1 - W_2} \tag{16.52}$$

where the geometries are defined as illustrated in Figure 16.79A. Figure 16.79B displays a photograph of two released structures: one with thicker necks, the other with necks so thin that they fractured upon release of the film. Based on the residual tensile strain of the film and the geometry of the structures that failed, the ultimate strain of the particular polyimide used was determined to be 4.5%.

Using similar micromachined tensile test structures [Biebl and von Philipsborn, 1993] measured the fracture strength of undoped and doped polysilicon and found 2.84 ± 0.09 GPa for undoped material and 2.11 ± 0.10 GPa in the case of phosphorous doping, 2.77 ± 0.08 GPa for boron doping and 2.70 ± 0.09 GPa for arsenic doping. No statistically significant differences were observed between samples released using concentrated HF or buffered HF. However, a 17% decrease of the fracture stress was observed for a 100% increase in etching time. These data contrast with Greek et al. (1995) *in situ* tensile strength test result of 768 MPa for an undoped poly-Si film. A mean tensile strength almost ten times less than that of single crystal Si (6 GPa) [Ericson and Schweitz, 1990]. We normally expect polycrystalline films to be stronger than single crystal films (see below under Strength of Thin Films). Greek et al. (1995) explain this discrepancy for poly-Si by pointing out that their polysilicon films have a very rough surface compared to single crystal material, containing many locations of stress concentration where a fracture crack can be initiated.

Biaxial Measurements of Mechanical Properties of Thin Films: Suspended Membrane Methods

We noted earlier that none of the disk stress-measuring techniques is suitable for measuring stress in low modulus tensile materials such as polyimides. Suspended membranes are very convenient for this purpose. The same micromachined test structure used for adhesion testing, sometimes called the blister test, as shown in Figure 16.73, can measure the tensile stress in low modulus materials. This type of test structure ensues from shaping a silicon diaphragm by conventional anisotropic etching, followed by applying the coating, and, finally, removing the supporting silicon from the back with an SF_6 plasma [Senturia, 1987]. By pressurizing one side of the membrane and measuring the deflection, one can extract both the residual stress and the biaxial modulus of the membrane. Pressure to the suspended film can be applied by a gas or by a point-load applicator [Vinci and Braveman, 1991]. The load-deflection curve at moderate deflections (strains less than 5%) answers to:

$$p = C_1\frac{\sigma t d}{a^2} + C_2\left(\frac{E}{1-\nu}\right)\frac{t d^3}{a^4} \tag{16.53}$$

where p represents the pressure differential across the film; d, the center deflection; a, the initial radius; t, the membrane thickness; and σ, the initial film stress. In the simplified Cabrera model for circular membranes the constants C_1 and C_2 equal 4 respectively 8/3. For more rigorous solutions for both circular and rectangular membranes and references to other proposed models, refer to Maseeh-Tehrani [Maseeh-Tehrani, 1990]. The relation in Eq. (16.53) can simultaneously determine σ and the biaxial modulus $E/1 - \nu$; plotting pa^2/dt vs. $(d/a)^2$ should yield a straight line. The residual stress can be extracted from the intercept and the biaxial modulus from the slope of the least-squares-best-fit line [Senturia, 1987]. A typical result obtained via such measurements is represented in Figure 16.80. For the same Dupont polyimide 2525, measuring a Young's modulus of 3350 MPa in the uniaxial test (Figure 16.78B), the measurements give 5540 MPa for the biaxial modulus and 32 MPa for the residual stress. The residual stress-to-biaxial modulus ratio, also referred to as the residual biaxial strain, thus reaches 0.6%. The latter quantity must be compared to the ultimate strain when evaluating potential reliability problems associated with cracking of films. By loading the membranes to the elastic limit point, yield stress and strain can be determined as with the uniaxial test.

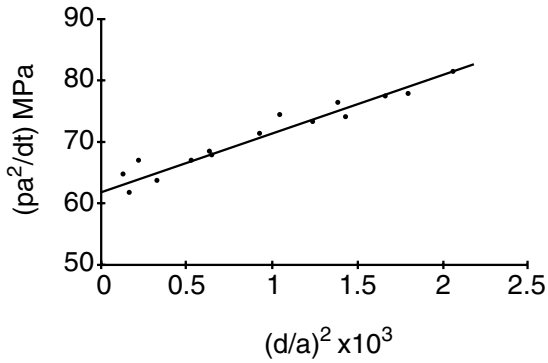


FIGURE 16.80 Load deflection data of a polyimide membrane (Du Pont 2525). From the intercept, a residual stress of 32 MPa was calculated and from the slope, a biaxial modulus of 5540 MPa. (From Senturia, S., Can We Design Microbiotic Devices without Knowing the Mechanical Properties of the Materials?, presented at Micro Robots and Teleoperators Workshop, Hyannis, MA, 1987. With permission.)

Poisson Ratio for Thin Films

The Poisson ratio for thin films presents us with more difficulties to measure than the Young's modulus as thin films tend to bend out of plane in response to in-plane shear. Maseeh and Senturia (1989) combine uniaxial and biaxial measurements to calculate the in-plane Poisson ratio of polyimides. For example, for the Dupont polyimide 2525, they determined 3350 MPa for E and 5540 MPa for the biaxial modulus ($E/1 - \nu$) leading to 0.41 ± 0.1 for the Poisson's ratio (ν). The errors on both the biaxial and uniaxial measurements need to be reduced in order to develop more confidence in the extracted value of the Poisson's ratio. At present, the precision on the Poisson's ratio is limited to about 20%.

Other Surface Micromachined Structures to Gauge Intrinsic Stress

Various other surface micromachined structures have been used to measure mechanical properties of thin films. We will give a short review here, but the interested reader might want to consult the original references for more details.

Clamped-Clamped Beams. Several groups have used rows of clamped-clamped beams (bridges) with incrementally increasing lengths to determine the critical buckling load and hence deduce the residual compressive stress in polysilicon films (Figure 16.81A) [Sekimoto et al., 1982; Guckel et al., 1985]. The residual strain, $\varepsilon = \sigma/E$, is obtained from the critical length, L_c, at which buckling occurs (Euler's formula for elastic instability of struts):

$$\varepsilon = \frac{4\pi^2}{A}\frac{I}{L_c^2} \tag{16.54}$$

where A is the beam cross-sectional area and I the moment of inertia. As an example, with a maximum beam length of 500 μm and a film thickness of 1.0 μm, the buckling beam method can detect compressive stress as small as 0.5 MPa. This simple Euler approach does not take into considerations additional effects such as internal moments resulting from gradients in residual stress.

Ring Crossbar Structures. Tensile strain can be measured by a series of rings (Figure 16.81B) constrained to the substrate at two points on a diameter and spanned orthogonally by a clamped-clamped beam. After removal of the sacrificial layer, tensile strain in the ring places the spanning beam in compression; the critical buckling length of the beam can be related to the average strain [Guckel et al., 1988].

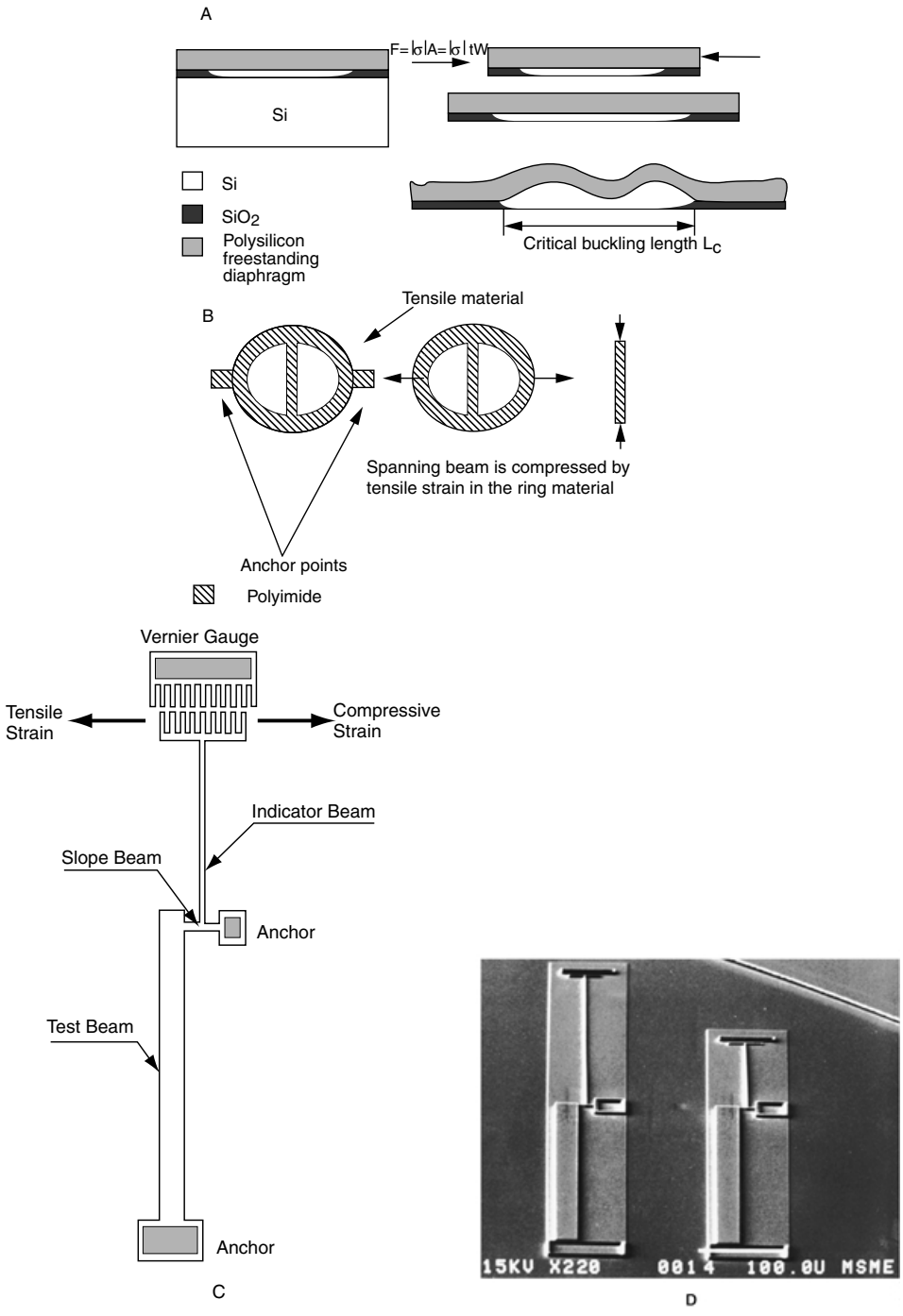


FIGURE 16.81 Some micromachined structures used for stress measurements. (A) Clamped-clamped beams: measuring the critical buckling length of clamped-clamped beams enables measurement of residual stress. (B) Crossbar rings: tensile stress can be measured by buckling induced in the crossbar of a ring structure. (C) A schematic of a strain gauge capable of measuring tensile or compressive stress. (D) SEM microphotograph of two strain gauges. (C and D from Lin, L., Selective Encapsulations of MEMS: Micro Channels, Needles, Resonators and Electromechanical Filters, Ph.D. thesis, University of California, Berkeley, 1993. With permission.)

Vernier Gauges. Both clamped-clamped beams and ring structures need to be implemented in entire arrays of structures. They do not allow easy integration with active microstructures due to space constraints. As opposed to proof structures one might use vernier gauges to measure the displacement of structures induced by residual strain [Lin, 1993]. The idea was first explored by Kim (1991), whose device consisted of two cantilever beams fixed at two opposite points. The end movement of the beams caused by the residual strain was measured by a vernier gauge. This method only requires one structure, but the best resolution for strain measurement reported is only 0.02% for 500-μm beams. Moreover, the vernier gauge device may indicate an erroneous strain when an out-of-plane strain gradient occurs [Lin, 1993]. Other types of direct strain measurement devices are the T- and H-shaped structures from Allen et al. (1987) and Mehregany et al. (1987) Optical measurement of the movement at the top of the T- or H-shape structures only becomes possible with very long beams (greater than 2.5 mm). They occupy large areas and their complexity requires finite element methods to analyze their output. The same is true for the strain magnification structure by Goosen et al. (1993). This structure measures strain by interconnecting two opposed beams such that the residual strain in the beams causes a third beam to rotate as a gauge needle. The rotation of the gauge needle quantifies the residual strain. A schematic of a micromachined strain gauge capable of measuring tensile or compressive residual stress, as shown in Figure 16.81C, was developed by Lin at University of California, Berkeley [Lin, 1993]. Figure 16.81D represents a scanning electron microscope (SEM) photograph of Lin's strain gauge. This gauge by far outranks the various *in situ* gauges explored. The strain gauge uses only one structure, can be fabricated *in situ* with active devices, determines tensile or compressive strain under optical microscopes, has a fine resolution of 0.001%, and resists to the out-of-plane strain gradient. When the device is released in the sacrificial etch step, the test beam (length L_t) expands or contracts, depending on the sign of the residual stress in the film, causing the compliant slope beam (length L_s) to deflect into an 's' shape. The indicator beam (length L_i), attached to the deforming beam at its point of inflection, rotates through an angle θ, and the deflection δ is read on the vernier scale. The residual strain is calculated as [Lin, 1993]:

$$\varepsilon_f = \frac{2L_s\delta}{3L_iL_tC} \tag{16.55}$$

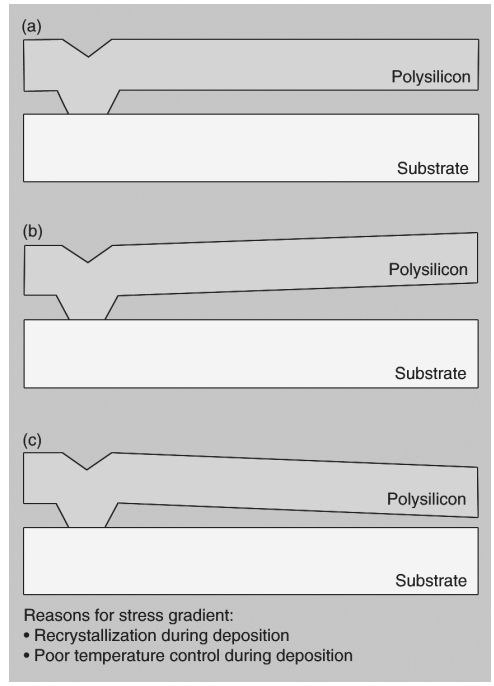
where C is a correction factor due to the presence of the indicator beam [Lin, 1993]. This equation was derived from simple beam theory relations and assumes that no out-of-plane motion occurs. The accuracy of the strain gauge is greatly improved because its output is independent of both the thickness of the deposited film and the cross section of the microstructure. Krulevitch used these devices to measure residual stress in *in situ* phosphorus-doped poly-Si films [Krulevitch, 1994], while Lin tested LPCVD silicon-rich silicon nitride films with it [Lin, 1993].

An improved micromachined indicator structure, inspired by Lin's work, was built by Ericson et al. (1995) By reading an integrated nonius scale in an SEM or an optical microscope, internal stress was measured with a resolution better than 0.5 MPa [Ericson et al., 1995; Benitez et al., 1995]. Both thick (10-μm) and thin (2-μm) poly-Si films were characterized this way.

Lateral Resonators. Biebl et al. (1995) extracted the Young's modulus of *in situ* phosphorus-doped polysilicon by measuring the mechanical response of poly-Si linear lateral comb-drive resonators (see Figure 16.88). The results reveal a value of 130 ± 5 GPa for the Young's modulus of highly phosphorus-doped films deposited at 610°C with a phosphine-to-silane mole ratio of 1.0×10^{-2} and annealing at 1050°C. For a deposition at 560°C with a phosphine to silane ratio of 1.6×10^{-3}, a Young's modulus of 147 ± 6 GPa was extracted.

Stress Nonuniformity Measurement by Cantilever Beams and Cantilever Spirals

The uniformity of stress through the depth of a film introduces an extremely important property to control. Variations in the magnitude and direction of the stress in the vertical direction can cause cantilevered



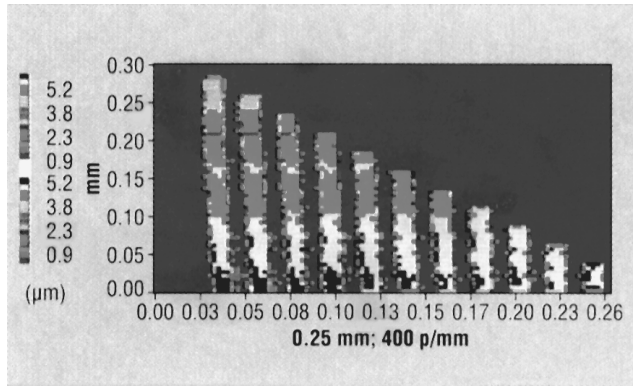


FIGURE 16.82 (A) Micro-cantilever deflection for measuring stress non-uniformity. (a) No gradient; (b) high tensile stress near the surface; and (c) lower tensile stress near the surface. (B) Topographical contour map of polysilicon cantilever array. (From Core, T.A., W.K. Tsang, and S.J. Sherman, *Solid State Technol.*, 36, 39–47, 1993. With permission.)

structures to curl toward or away from the substrate. Stress gradients present in the polysilicon film must thus be controlled to ensure predictable behavior of designed structures when released from the substrate. To determine the thickness variation in residual stress, noncontact surface profilometer measurements on an array of simple cantilever beams [Core et al., 1993; Chu et al., 1992] or cantilever spirals can be used [Fan et al., 1990].

Cantilever Beams. The deflections resulting from stress variation through the thickness of simple cantilever beams after their release from the substrate is shown in Figure 16.82A. The bending moment causing deflection of a cantilever beam follows out of pre-release residual stress and is given by (see Figure 16.82A):

$$M = \int_{-t/2}^{t/2} zb\sigma(z)\, dZ \tag{16.56}$$

where $\sigma(z)$ represents the residual stress in the film as a function of thickness and b stands for cantilever width. Assuming a linear strain gradient Γ (physical dimensions 1/length) such that $\sigma(z) = E\Gamma z$, Eq. (16.56) converts to:

$$\Gamma = \frac{M(12)}{Ebt^3} = \frac{M}{EI} \tag{16.57}$$

where the moment of inertia, I, for a rectangular cross section is given by $I = bt^3/12$. The measured deflection z, i.e., the vertical deflection of the cantilever's endpoint, from beam theory for a cantilever with an applied end moment, is given as:

$$z = \frac{ML^2}{2EI} = \frac{\Gamma L^2}{2} \tag{16.58}$$

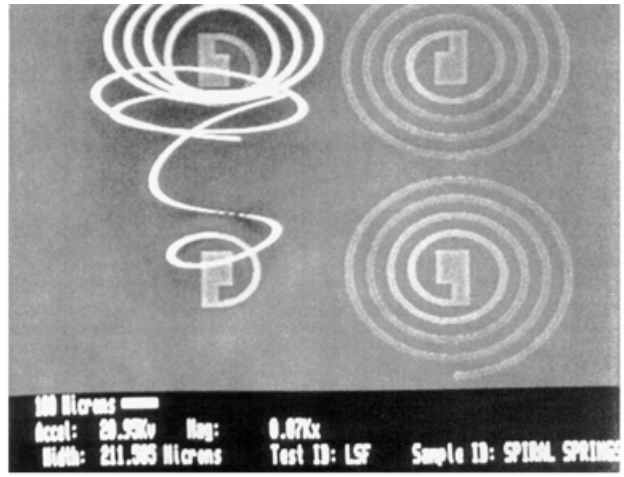
Figure 16.82B represents topographical contour map of an array of polysilicon cantilevers. The cantilevers vary in length from 25 to 300 μm by 25-μm increments. Notice that the tip of the longest cantilever resides at a lower height (approximately 0.9 μm closer to the substrate) than the anchored support, indicating a downward bending moment [Core et al., 1993]. The gradients can be reduced or eliminated with a high-temperature anneal. With integrated electronics on the same chip, long high-temperature processing must be avoided. Therefore, stress gradients can limit the length of cantilevered structures used in surface-micromachined designs.

Cantilever Spirals. Residual stress gradients can also be measured by Fan's cantilever spiral as shown in Figure 16.83A [Fan et al., 1990]. Spirals anchored at the inside spring upwards, rotate, and contract with positive strain gradient (tending to curl a cantilever upwards), while spirals anchored at the outside deflect in a similar manner in response to a negative gradient. Theoretically, positive and negative gradients produce spirals with mirror symmetry [Fan et al., 1990]. The strain gradient can be determined from spiral structures by measuring the amount of lateral contraction, the change in height, or the amount of rotation. Krulevitch presented the computer code for the spiral simulation in his doctoral thesis [Krulevitch, 1994]. Figure 16.83B shows a simulated spiral with a bending moment of $\Gamma = \pm 3.0\ \text{mm}^{-1}$ after release.

Krulevitch compared all the above surface micromachined structures for stress and stress gradient measurements on poly-Si films. His comments are summarized in Table 16.12 [Krulevitch, 1994]. Krulevitch found that the fixed-fixed beam structures for determining compressive stress from the buckling criterion produced remarkably self-consistent and repeatable results. Wafer curvature stress profiling proved reliable for determining average stress and the true stress gradient as compared with micromachined spirals. Measurements of curled cantilevers could not be used much as the strain gradients mainly were negative for poly-Si, leading to cantilevers contacting the substrate. The strain gauge dial structures were useful over a rather limited strain-gradient range. With too large a strain gradient curling of the long beams overshadows expansion effects and makes the vernier indicator unreadable.

16.12.4 Strength of Thin Films

Due to the high activation energy for dislocation motion in silicon (2.2 eV), hardly any plastic flow occurs in single crystalline silicon for temperatures lower than 673°C. Grain boundaries in poly-Si block dislocation motion; hence, polysilicon films can be treated as an ideal brittle material at room temperature [Biebl et al., 1995]. High yield strengths often are obtained in thin films with values up to 200 times as large as those found in the corresponding bulk material [Campbell, 1970]. In this light, the earlier quoted fracture stresses of poly-Si, between two and ten times smaller than that of bulk single crystal, are



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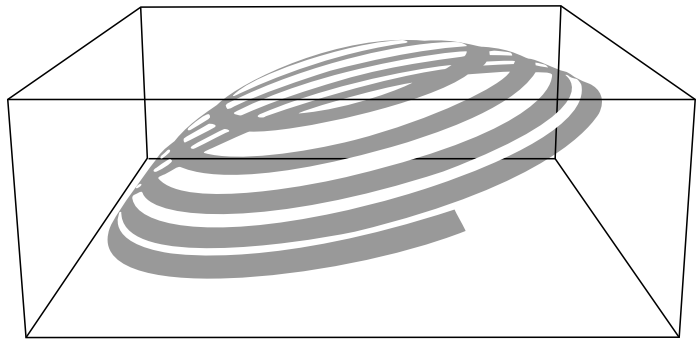


B

FIGURE 16.83 Cantilever spirals for stress gradient measurement. (A) SEM of micrographs of spirals from an as-deposited poly-Si. (Courtesy of Dr. L.S. Fan.) (B) Simulation of a thin-film micromachined spiral with $\Gamma = 3.0\ mm^{-1}$. (From Krulevitch, P.A., Micromechanical Investigations of Silicon and Ni-Ti-Cu Thin Films, Ph.D. thesis, University of California, Berkeley, 1994. With permission.)

TABLE 16.12 Summary of Various Techniques for Measuring Residual Film Stress

Measurement Technique	Measurable Stress State	Remarks
Wafer curvature	Stress gradient, average stress	Average stress over entire wafer; provides true stress gradient; approx. 5 MPa resolution
Vernier strain gauges	Average stress	Local stress; small dynamic range; resolution = 2 MPa
Spiral cantilevers	Stress gradient	Local stress, provides equivalent linear gradient
Curling beam cantilevers	Large positive stress gradient	Local stress, provides equivalent linear gradient
Fixed-fixed beams	Average compressive stress	Local stress measurement

Source: Krulevitch, P.A., Micromechanical Investigations of Silicon and Ni-Ti-Cu Thin Films, Ph.D. thesis, University of California, Berkeley, 1994. With permission.

surprising. Greek et al. (1995) explain this deviation by pointing at the high surface roughness of poly-Si films compared to single crystal Si. They believe that a reduction in surface roughness would improve the tensile fracture strength considerably.

Indentation (hardness) testing is very common for bulk materials where the direct relationship between bulk hardness and yield strength is well known. It can be measured by pressing a hard, specially shaped point into the surface and observing indentation. This type of measurement is of little use for measuring thin films

below 5×10^4 Å. Consequently, very little is known about the hardness of thin films. Recently, specialized instruments have been constructed (e.g., the Nanoindenter) in which load and displacement data are collected while the indentation is being introduced in a thin film. This eliminates the errors associated with later measurement of indentation size and provides continuous monitoring of load/displacement data similar to a standard tensile test. Load resolution may be 0.25 μN, displacement resolution 0.2 to 0.4 nm, and x-y sample position accuracy 0.5 μm. Empirical relations have correlated hardness with Young's modulus and with uniaxial strength of thin films. Hardness calculations must include both plastic and long-distance elastic deformation. If the indentation is deeper than 10% of the film, corrections for elastic hardness contribution of the substrate must also be included [Vinci and Braveman, 1991]. Mechanical properties such as hardness and modulus of elasticity can be determined on the micro- to picoscales using AFM [Bushan, 1996]. Bushan provides an excellent introduction to this field in *Handbook of Micro/Nanotribology* [Bushan, 1995].

16.13 Surface Micromachining Processes

16.13.1 Basic Process Sequence

A surface micromachining process sequence for the creation of a simple free-standing poly-Si bridge is illustrated in Figure 16.84 [Howe and Muller, 1983; Howe, 1985]. A sacrificial layer, also called a spacer layer or base, is deposited on a silicon substrate coated with a dielectric layer as the buffer/isolation layer (Figure 16.84A). Phosphosilicate glass (PSG) deposited by LPCVD stands out as the best material for the sacrificial layer because it etches even more rapidly in HF than SiO_2. In order to obtain a uniform etch rate, the PSG film must be densified by heating the wafer to 950–1100°C in a furnace or a rapid

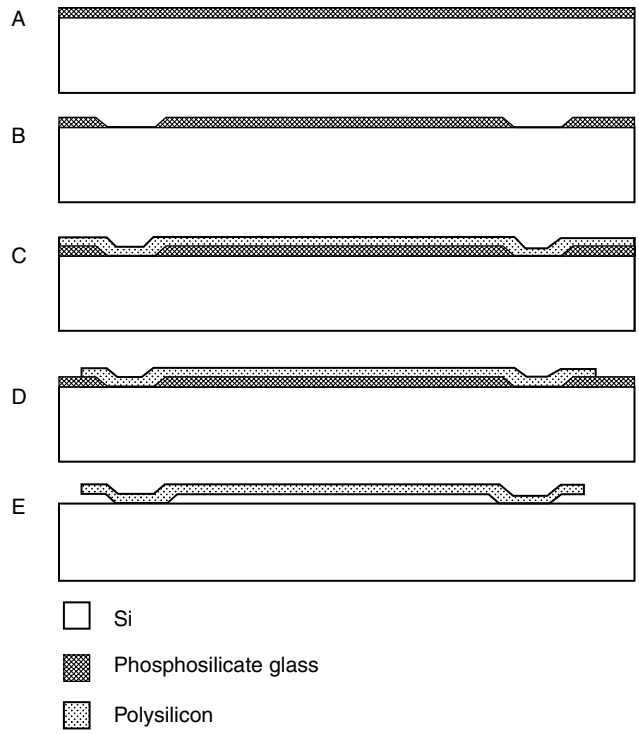


FIGURE 16.84 Basic surface micromachining process sequence. (A) Spacer layer deposition (the thin dielectric insulator layer is not shown). (B) Base patterning with mask 1. (C) Microstructure layer deposition. (D) Pattern microstructure with mask 2. (E) Selective etching of spacer layer.

thermal annealer (RTA) [Yun, 1992]. With a first mask the base is patterned as shown in Figure 16.84B. Windows are opened up in the sacrificial layer and a microstructural thin film, whether consisting of polysilicon, metal, alloy or a dielectric material, is conformably deposited over the patterned sacrificial layer (Figure 16.84C). Furnace annealing, in the case of polysilicon at 1050°C in nitrogen for one hour, reduces stress stemming from thermal expansion coefficient mismatch and nucleation and growth of the film. Rapid thermal annealing has been found effective for reducing stress in polysilicon as well [Yun, 1992]. With a second mask, the microstructure layer is patterned, usually by dry etching in a $CF_4 + O_2$ or a $CF_3Cl + Cl_2$ plasma (Figure 16.84D) [Adams, 1988]. Finally, selective wet etching of the sacrificial layer, say in 49% HF, leaves a free-standing micromechanical structure (Figure 16.84E). The surface micromachining technique is applicable to combinations of thin films and lateral dimensions where the sacrificial layer can be etched without significant etching or attack of the microstructure, the dielectric or the substrate.

16.13.2 Fabrication Step Details

16.13.2.1 Pattern Transfer to SiO_2 Buffer/Isolation Layer

A blanket n^+ diffusion of the Si substrate, defining a ground plane, often outlines the very first step in surface micromachining, followed by a passivation step of the substrate, for example, with 0.15-μm-thick LPCVD nitride on a 0.5-μm thermal oxide. Suppose the buffer/isolation passivation layer as illustrated in Figure 16.85 itself needs to be patterned, perhaps to make a metal contact pad onto the Si substrate. Then, the appropriate fabrication step is a pattern transfer to the thin isolation film as shown in Figure 16.85, illustrating a wet pattern transfer to a 1-μm-thick thermal SiO_2 film with a 1-μm resist layer. Typically, an isotropic etch such as buffered HF, e.g., BHF (5:1), which is 5 parts NH_4F and 1 part conc. HF, is used (unbuffered HF attacks the photoresist). This solution etches SiO_2 at a rate of 100 nm/min, and the creation of the opening to the underlying substrate takes about 10 min. The etch progress may be monitored optically (color change) or by observing the hydrophobic/hydrophilic behavior [Hermansson et al., 1991] of the etched layer. With a resist opening, L_m, the undercut typically measures the same thickness as the oxide thickness, t_{SiO_2}. In other words, the contact pad will have a size of $L_m + 2t_{SiO_2}$. The undercut worsens with loss of photoresist adhesion during etching. Using an adhesion promoter such

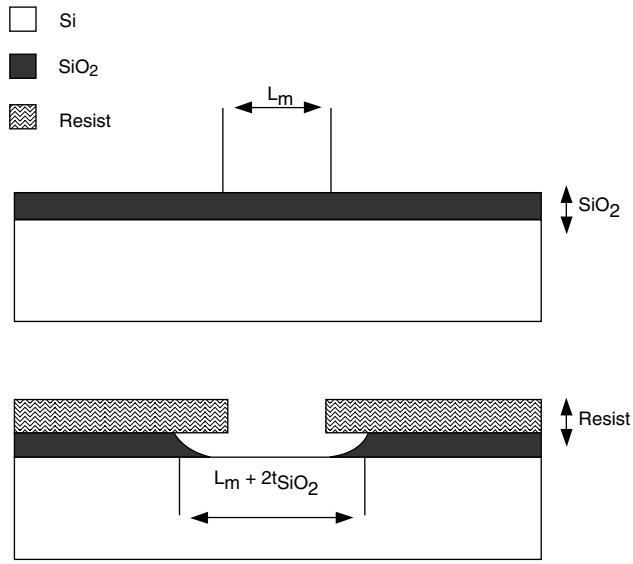


FIGURE 16.85 Wet etch pattern transfer to a thin thermal SiO_2 film for the fabrication of a contact pad to the Si substrate.

as HMDS (hexamethyldisilazane) prove useful in such case. A new bake after 5 min of etching is a good procedure to maintain the resist integrity. After the isotropic etch, the resist is stripped in a piranha etch bath. This strong oxidizer grows about 3 nm of oxide back in the cleared window. To remove the oxide resulting from the piranha, a dip in diluted BHF suffices. After cleaning and drying, the substrate is ready for contact metal and base material deposition. Applying a dry etch (say, a CF_4-H_2 plasma) to open up the window in the oxide would eliminate undercutting of the resist, but requires a longer set-up time. With an LPCVD low stress nitride on top of a thermal SiO_2, an often-used combination for etching the buffer/isolation layer is a dry etch (say, a SF_6 plasma) followed by a 5:1 BHF [Tang, 1990].

16.13.2.2 Base Layer (also Spacer or Sacrificial Layer) Deposition and Etching

A thin LPCVD phosphosilicate glass (PSG) layer (say, 2 μm thick) is a preferred base, spacer, or sacrificial layer material. Adding phosphorous to SiO_2 to produce PSG enhances the etch rate in HF [Monk et al., 1992; Tenney and Ghezzo, 1973]. Other advantages to using doped SiO_2 include its utility as a solid state diffusion dopant source to make subsequent polysilicon layers electrically conductive and helping to control window taper (see below). As deposited phosphosilicate displays a nonuniform etch rate in HF and must be densified, typically carried out in a furnace at 950°C for 30 min to 1 hr in a wet oxygen ambient. The etch rate in BHF can be used as the measure of the densification quality. The base window etching stops at the buffer isolation layer, often a Si_3N_4/SiO_2 layer which also forms the permanent passivation of the device. Windows in the base layer are used to make anchors onto the buffer/isolation layer for mechanical structures.

The edges of the etched windows in the base may need to be tapered to minimize coverage problems with subsequent structural layers, especially if these layers are deposited with a line-of-sight deposition technique. An edge taper is introduced through an optimization of the plasma etch conditions (see Madou [1997, chap. 2]), through the introduction of a gradient of the etch rate, or by reflow of the etched spacer. In Figure 16.86A we depict the reflow process of a PSG spacer after patterning in a dry etch. Viscous flow at higher temperature smoothes the edge taper. The ability of PSG to undergo viscous deformation at a given temperature primarily is a function of the phosphorous content in the glass; reflow profiles get progressively smoother the higher the phosphorous concentration—reflecting the corresponding

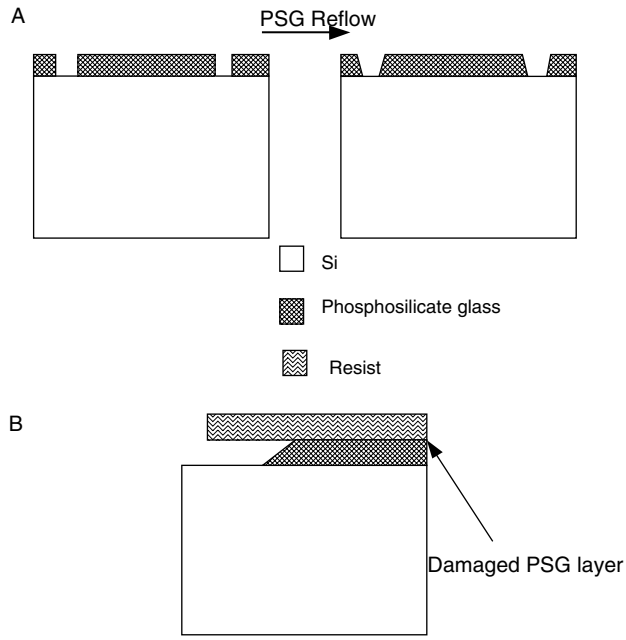


FIGURE 16.86 Edge taper of spacer layer. (A) Taper by reflow of PSG. (B) Taper by ion implantation of PSG.

enhancement in viscous flow [Levy and Nassau, 1986]. In Figure 16.86B, ion implantation of PSG has created a rapidly etching, damaged PSG layer [North et al., 1978; Goetzlich and Ryssel, 1981; White, 1980]. The steady-state taper is a function of the etch rate in PSG etchants (e.g., BHF).

16.13.2.3 Deposition of Structural Material

For the best step coverage of a structural material over the base window, chemical vapor deposition is preferred. If a physical deposition method must be used, sputtering is preferred over line-of-sight deposition techniques which lead to the poorest step coverage (see Madou [1997, chap. 3]). In the latter case, edge taper could be introduced advantageously.

The most widely used structural material in surface micromachining is polysilicon (poly-Si or simply poly). Polysilicon is deposited by low pressure (25 to 150 Pa) chemical vapor deposition in a furnace (a poly chamber) at about 600°C. The undoped material is usually deposited from pure silane, which thermally decomposes according to the reaction:

$$SiH_4 \rightarrow Si + 2H_2 \qquad \text{(Reaction 16.16)}$$

Typical process conditions may consist of a temperature of 605°C, a pressure of 550 mTorr (73 Pa), and a silane flow rate of 125 sccm. Under those conditions a normal deposition rate is 100 Å/min. To deposit a 1-μm film will take about 90 min. Sometimes the silane is diluted by 70 to 80% nitrogen. The silicon is deposited at temperatures ranging from 570 to 580°C for fine-grained poly-Si to 620 to 650°C for coarse-grained poly-Si. The characteristics of these two types of poly-Si materials will be compared in the case studies presented below. Furnace annealing of the poly-Si film at 1050°C in nitrogen for one hour is employed commonly to reduce stress stemming from thermal expansion coefficient mismatch and nucleation and growth of the polysilicon film.

To make parts of the microstructure conductive, dopants can be introduced in the poly-Si film by adding dopant gases to the silane gas stream, by drive-in from a solid dopant source or by ion implantation. When doping from the gas phase, the dopant can be readily controlled in the range of 10^{19} to $10^{21}/cm^3$. Polysilicon deposition rates, in the case of gas phase doping (*in situ* doping), may be significantly impacted. For example, decreases in poly-Si deposition rate by as much as a factor of 25 have been reported in phosphine and arsine doping. The effect is associated with the poisoning of reaction sites by phosphine and arsine [Adams, 1988]. The lower deposition rate of *in situ* phosphine doping can be mitigated by reducing the ratio of phosphine to silane flow by one third [Howe, 1995]. With the latter flow regime, deposition at 585°C (for a 2-μm-thick film), followed by 900°C rapid thermal annealing for 7 min, results in a polysilicon with low residual stress, negligible stress gradient and low resistivity [Howe, 1995; Biebl et al., 1995]. *In situ* boron doping, in contrast to arsine and phosphine doping, accelerates the polysilicon deposition rate through an enhancement of silane adsorption induced by the boron presence [Fresquet et al., 1995]. Film thickness uniformity for doped films typically is less than 1% and sheet resistance uniformity less than 2%. Alternatively, poly-Si may be doped from PSG films sandwiching the undoped poly-Si film. By annealing such a sandwich at 1050°C in N_2 for one hour, the polysilicon is symmetrically doped by diffusion of dopant from the top and the bottom layers of PSG. Symmetric doping results in a polysilicon film with a moderate compressive stress. The resulting uniform grain texture avoids gradients in the residual stress which would cause bending moments warping microstructures upon release. Finally, ion implantation of undoped polysilicon, followed by high temperature dopant drive-in, also leads to conductive polysilicon. This polysilicon has a moderate tensile stress, with a strain gradient that causes cantilevers to deflect toward the substrate [Core et al., 1993]. The poly-Si is now ready for patterning by RIE in, say, a CF_4-O_2 plasma.

Although the mechanical properties still are not well understood, microstructures based on poly-Si as a mechanical member have been commercialized [Editor, 1991; Core et al., 1993]. Other structural materials used in surface micromachining include single crystal Si (epi-Si or etched back, fusion bonded Si), SiO_2, silicon nitride, silicon oxynitride, polyimide, diamond, SiC, GaAs, tungsten, α-Si:H, Ni, W, Al etc. A few words about the merit of some of these materials as structural components follow.

Silicon nitride and silicon oxide also can be deposited by CVD methods but usually exhibit too much residual stress which hampers their use as mechanical components. However, CVD of mixed silicon oxynitride can produce substantially stress-free components.

Amorphous Si (α-Si) can be stress annealed at temperatures as low as 400°C [Chang et al., 1991]. This low-temperature anneal makes the material compatible with almost any active electronic component. Unfortunately, very little is known about the mechanical properties of amorphous Si.

Hydrogenated amorphous Si (α-Si:H), with its interesting electronic properties, is even less understood in terms of its mechanical properties. If the mechanical properties of hydrogenated amorphous Si were found as good as those of poly-Si, the material might make a better choice than poly-Si as a MEMS material given its better electronic characteristics.

Tungsten CVD deposition is IC compatible. The material has some unique mechanical properties (see Madou [1997, chap. 8, Table 8.4]). Moreover, the material can be applied selectively. Selective CVD tungsten has the unique property that tungsten will only nucleate on silicon or metal surfaces but does not deposit on dielectrics such as oxides and nitrides [Chen and MacDonald, 1991].

Metals and polyimides, because they are easily deformed, usually do not qualify as mechanical members but have been used, for example, in plastically deformable hinges [Suzuki et al., 1994; Hoffman et al., 1995]. Aluminum constitutes the mirror material in Texas Instruments' flexure-beam micromirror devices (FBMDs). The metal is used both for the L-shaped flexure hinges and the mirror itself [Lin, 1996]. Polycrystalline diamond films, deposited by CVD, are potential high-temperature, harsh environment MEMS candidates [Herb et al., 1990]. Problems include oxidation above 500°C for nonpassivated films, difficulty of making reliable ohmic contact to the material, and the reproducibility and surface roughness of the films [Obermeier, 1995]. Poly-SiC films have been deposited by an APCVD process on 4-in. polysilicon-coated, silicon wafers. A surface micromachining process using the underlying polysilicon film as the sacrificial layer was developed. Poly-SiC is projected for use as structural material for high temperatures and harsh environments, and to reduce friction and wear between moving components [Fleischman et al., 1996]. Surface micromachining of thin single crystalline Si layers in SOI and with polyimides is discussed separately below.

16.13.2.4 Selective Etching of Spacer Layer

Selective Etching

To create movable micromachines the microstructures must be freed from the spacer layers. The challenge in freeing microstructures by undercutting is evident from Figure 16.87. After patterning the poly-Si by

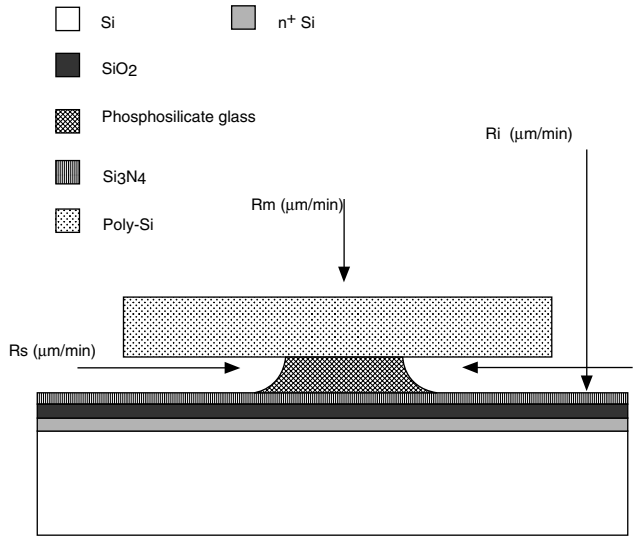


FIGURE 16.87 Selective etching of spacer layer.

RIE in, say, a SF_6 plasma, it is immersed in an HF solution to remove the underlying sacrificial layer, releasing the structure from the substrate. Commonly, a layer of sacrificial phosphosilicate glass, between 1 and 2000 μm long and 0.1 to 5 μm thick, is etched in concentrated, dilute or buffered HF. The spacer etch rate, R_s, should be faster than the attack on the microstructural element, R_m, and that of the insulator layer, R_i. For this type of complete undercutting, only wet etchants can be used. Etching narrow gaps and undercutting wide areas with BHF can take hours. To shorten the etch time, extra apertures in the microstructures sometimes are provided for additional access to the spacer layer. The etch rate of PSG, the most common spacer material, increases monotonically with dopant concentration, and thicker sacrificial layers etch faster than thinner layers [Monk et al., 1994].

The selectivity ratios for spacer layer, microstructure and buffer layer are not infinite [Lober and Howe, 1998], and in some instances even silicon substrate attack by BHF was observed under polysilicon/spacer regions [Fan et al., 1988; Mehregany et al., 1988]. Heavily phosphorous-doped polysilicon is especially prone to attack by BHF. Silicon nitride deposited by LPCVD etches much more slowly in HF than oxide films, making it a more desirable isolation film. When depositing this film with a silicon-rich composition, the etch rate is even slower (15 nm/min) [Tang, 1990]. Eaton et al. (1995) compared oxide and nitride etching in a 1:1 HF:H_2O and in a 1:1 HF:HCl solution and concluded that the HCl-based etch yielded both faster oxide etch rates (617 nm/min vs. 330 nm/min) and slower nitride etch rates (2 nm/min vs. 3.6 nm/min), providing a much greater selectivity of the oxide to silicon nitride (310 vs. 91!). The same authors also studied the optimum composition of a sacrificial oxide for the fastest possible etching in their most selective 1:1 HF:HCl etch. The faster sacrificial layer etch limited the damage to nitride structural elements. Their results are summarized in Table 16.13. A densified CVD SiO_2 was used as a control, and a 5%/5% borophosphosilicate glass (BPSG) was found to etch the fastest.

Watanabe et al. (1995) using low pressure vapor HF, found high etch ratios of PSG and BPSG to thermal oxides of over 2000, with the BPSG etching slightly faster than the PSG. We will see further that low pressure vapor HF also leads to less stiction of structural elements to the substrate. In Table 16.14 we present etch rate and etch ratios for R_i and R_s in BHF (7:1) for a few selected materials.

Detailed studies on the etching mechanism of oxide spacer layers were undertaken by Monk et al. (1994a; 1994b) They found that the etching reaction shifts from kinetic controlled to diffusion controlled as the etch channel becomes longer. This affects mainly large-area structures, as diffusion limitations were observed only after approximately 200 μm of channel etching or 15 min in concentrated HF. Eaton and Smith (1996) developed a release etch model which is an extension of the work done by Monk et al. (1994a; 1994b) and Liu et al. (1993).

TABLE 16.13 Etch Rate in 1:1 HF:HCl of a Variety of Sacrificial Oxides

Thin Oxide	Lateral Etch Rate (Å/min)
CVD SiO_2 (densified at 1050°C for 30 min)	6170
Ion-implanted and densified CVD SiO_2 (P, $8 \times 10^{15}/cm^2$, 50 keV)	8330
Phosphosilicate (PSG)	11,330
5%/5% borophosphosilicate (BPSG)	41,670

Source: Adapted from Eaton, W.P. and Smith, J.H., A CMOS-compatible, Surface Micromachined Pressure Sensor for Aqueous Ultrasonic Application, presented at SPIE Smart Structure and Materials, 1995.

TABLE 16.14 Etching of Spacer Layer and Buffer Layer in BHF (7:1)

	Material		
Property	LPCVD Si_3N_4	LPCVD SiO_2	LPCVD 7% PSG
Etch rate	7–12 Å/min (R_i)	700 Å/min (R_s)	~10,000 Å/min (R_s)
Selectivity ratio	1	60–100	~800–1200

TABLE 16.15 Etchants-Spacer and Microstructural Layer

Etchant	Buffer/Isolation	Spacer	Microstructure
Buffered HF (5:1, NH_4F: conc. HF)[a]	LPCVD Si_3N_4/thermal SiO_2	PSG	Poly-Si
RIE using CHF_3 BHF (6:1)[b]	LPCVD Si_3N_4	LPCVD SiO_2	CVD Tungsten
KOH[c]	LPCVD Si_3N_4/thermal SiO_2	Poly-Si	Si_3N_4
Ferric chloride[d]	Thermal SiO_2	Cu	Polyimide
HF[e]	LPCVD Si_3N_4/thermal SiO_2	PSG	Polyimide
Phosphoric/acetic acid/nitric acid (PAN, or 5:8:1:1 Water:phosphoric:acetic:nitric)[f]	Thermal SiO_2	Al	PECVD Si_3N_4 Nickel
Ammonium iodide/iodine alcohol[g]	Thermal SiO_2	Au	Ti
Ethylene-diamine/pyrocathecol (EDP)	Thermal SiO_2	Poly-Si	SiO_2

(a) Howe and Muller (1983), Howe (1985), Guckel and Burns (1984); (b) Chen and MacDonald (1991); (c) Sugiyama et al. (1986; 1987); (d) Kim and Allen (1991); (e) Suzuki et al. (1994); (f) Chang et al. (1991), Scheeper et al. (1991); (g) Yamada and Kuriyama (1991)

Etching is followed by rinsing and drying. Extended rinsing causes a native oxide to form on the surface of the polysilicon structure. Such a passivation layer often is desirable and can be formed more easily by a short dip in 30% H_2O_2.

Etchant-Spacer-Microstructure Combinations

A wide variety of etchant, spacer, and structural material combinations have been used; a limited listing is presented in Table 16.15. One interesting case concerns poly-Si as the sacrificial layer. This was used, for example, in the fabrication of a vibration sensor at Nissan Motor Co [Nakamura et al., 1985]. In this case poly-Si is etched in KOH from underneath a nitride/polysilicon/nitride sandwich cantilever. Also, a solution of HNO_3 and BHF can be used to etch poly-Si, but it proves difficult to control. Using aqueous solutions of NR_4OH, where R is an alkyl group, provides a better etching solution for poly-Si, with greater selectivity with respect to silicon dioxide and phosphosilicate glass. The relatively slow etch rate enables better process control [Bassous and Liu, 1978] and the etchant does not contain alkali ions, making it more CMOS compatible. With tetramethylammonium hydroxide (TMAH) the etch rate of CVD poly-Si, deposited at 600°C from SiH_4, follows the rates of the (100) face of single crystal Si and is dopant dependent. The selectivity of Si/SiO_2 and Si/PSG, at temperatures below 45°C are measured to be about 1000. Hence, a layer of 500-Å PSG can be used as the etch mask for 10,000 Å of poly-Si.

16.13.2.5 Stiction

Stiction During Release

The use of sacrificial layers enables the creation of very intricate movable polysilicon surface structures. An important limitation of such polysilicon shapes is that large-area structures tend to deflect through stress gradients or surface tension induced by trapped liquids and attach to the substrate/isolation layer during the final rinsing and drying step, a stiction phenomenon that may be related to hydrogen bonding or residual contamination. Recently, great strides were made towards a better understanding and prevention of stiction.

The sacrificial layer removal with a buffered oxide etch followed by a long, thorough rinse in deionized water and drying under an infrared lamp typically represent the last steps in the surface micromachining sequence. As the wafer dries, the surface tension of the rinse water pulls the delicate microstructure to the substrate where a combination of forces, probably van der Waals forces and hydrogen bonding, keeps it firmly attached (see Figure 16.88) [Core et al., 1993]. Once the structure is attached to the substrate by stiction, the mechanical force needed to dislodge it usually is large enough to damage the micromechanical structure [Lober and Howe, 1988; Guckel et al., 1987; Alley et al., 1988]. Basically, the same phenomena are thought to be involved in room temperature wafer bonding [Madou, 1997, chap. 8]. We will not further dwell upon the mechanics of the stiction process here, but the reader should refer to the theoretical and experimental analysis of the mechanical stability and adhesion of microstructures under capillary forces by Mastrangelo et al. (1993a; 1993b).

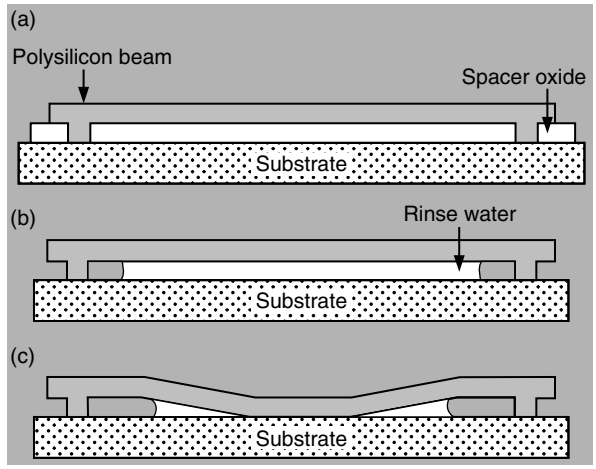


FIGURE 16.88 Stiction phenomenon in surface micromachining and the effect of surface tension on micromechanical structures. (a) Unreleased beam. (b) Released beam before drying. (c) Released beam pulled to the substrate by capillary forces as the wafer dries [conc].

Creating stand-off bumps on the underside of a poly-Si plate [Tang, 1990; Fan, 1989] or adding meniscus-shaping microstructures to the perimeter of the microstructure are mechanical means to help reduce sticking [Abe et al., 1995]. Fedder et al. (1992) used another mechanical approach to avoid stiction by temporarily stiffening the microstructures with polysilicon links. These very stiff structures are not affected by liquid surface tension forces and the links are severed afterward with a high current pulse once the potentially destructive processing is complete. Yet another mechanical approach to avoid stiction involves the use of sacrificial supporting polymer columns. A portion of the sacrificial layer is substituted by polymer spacer material, spun-on after partial etch of the oxide glass. After completion of the oxide etch, the polymer spacer prevents stiction during evaporative drying. Finally, an isotropic oxygen plasma etches the polymer to release the structure [Mastrangelo and Saloka, 1993].

Ideally, to ensure high yields, one should avoid contact between structural elements and the substrate during processing. In a liquid environment, however, this may become impossible due to the large surface tension effects. Consequently, most solutions to the stiction problem involve reducing the surface tension of the final rinse solution by physico-chemical means. Lober et al. (1988), for example, tried HF vapor and Guckel et al. (1989; 1990) used freeze-drying of water/methanol mixtures. Freezing and sublimating the rinse fluid in a low-pressure environment gives improved results by circumventing the liquid phase. Takeshima et al. (1991) used t-butyl alcohol freeze-drying. Since the freezing point of this alcohol lies at 25.6°C, it is possible to perform freeze-drying without special cooling equipment. More recently, attempts at supercritical drying resulted in high microstructure yields [Mulhern et al., 1993]. With this technique, the rinse fluid is displaced with a liquid that can be driven into a supercritical phase under high pressure. This supercritical phase does not exhibit surface tension. Typically, CO_2 under about 75 atm is used (see also Madou [1997, chap. 1 under Cleaning]).

Kozlowski et al. (1995) substituted HF in successive exchange steps by the monomer divinylbenzene to fabricate very thin (500 nm) micromachined polysilicon bridges and cantilevers. The monomer was polymerized under UV light at room temperature and was removed in an oxygen plasma. Analog Devices applied a proprietary technique involving only standard IC process technology in the fabrication of a micro-accelerometer to eliminate yield losses due to stiction [Core et al., 1993].

Stiction After Release, i.e., In-Use Stiction

Stiction remains a fundamental reliability issue due to contact with adjacent surfaces after release. Stiction free passivation that can survive the packaging temperature cycle is not known at present [Howe, 1995]. Attempted solutions are summarized below.

Adhesive energy may be minimized in a variety of ways, for example, by forming bumps on surfaces (see above) or roughening of opposite surface plates [Alley et al., 1993]. Also, self-assembled monolayer coatings have been shown to reduce surface adhesion and to be effective at friction reduction in bearings at the same time [Alley et al., 1992]. Making the silicon surface very hydrophobic or coating it with diamond-like carbon are other potential solutions for preventing postrelease stiction of polysilicon microstructures. Man et al. (1996) eliminate post-release adhesion in microstructures by using a thin conformal fluorocarbon film. The film eliminates the adhesion of polysilicon beams up to 230 μm long even after direct immersion in water. The film withstands temperatures as high as 400°C and wear tests show that the film remains effective after 10^8 contact cycles. Along the same line, ammonium fluoride-treated Si surfaces are thought to be superior to the HF-treated surfaces due to a more complete hydrogen termination, leading to a cleaner hydrophobic surface [Houston et al., 1995]. Gogoi and Mastrangelo (1995) introduced electromagnetic pulses for postprocessing release of stuck microstructures.

16.13.3 Control of Film Stress

After reviewing typical surface micromachining process sequences we are ready to investigate some of the mechanical properties of the fabricated mechanical members. Consider a lateral resonator as shown in Figure 16.89A. Electrostatic force is applied by a drive comb to a suspended shuttle. Its motion is detected capacitively by a sense comb. For many applications a tight control over the resonant frequency, f_0, is required. A simple analytical approximation for f_0 of this type of resonator can be deduced from Rayleigh's method [Howe, 1987]:

$$f_0 \approx \frac{1}{2\pi}\sqrt{\frac{4EtW^3}{ML^3} + \frac{24\sigma_r tW}{5ML}} \tag{16.59}$$

where E represents the Young's modulus of polysilicon; L, W and t are the length, width and thickness of the flexures; and M stands for the mass of the suspended shuttle (of the order of 10^{-9} kg, or less). For typical values ($L = 150$ μm and $W = t = 2$ μm) and a small tensile residual stress, the resonant frequency f_0 is between 10 and 100 kHz [Howe, 1995]. For typical values of L/W the stress term in Eq. (16.59) dominates the bending term. Any residual stress, σ_r, obviously will affect the resonant frequency. Consequently, stress and stress gradients represent critical stages for microstructural design. One of the many challenges of any surface-micromachining process is to control the intrinsic stresses in the deposited films. Several techniques can be used to control film stress. Some we detailed before, but we list them again for completeness:

- Large-grained poly-Si films, deposited around 625°C, have a columnar structure and are always compressive. Compressive stress can cause buckling in constrained structures. Annealing at high temperatures, between 900 and 1150°C, in nitrogen significantly reduces the compressive stress in as-deposited poly-Si [Guckel et al., 1985; Howe and Muller, 1983] and can eliminate stress gradients. No significant structural changes occur when annealing a columnar poly-Si film. The annealing process is not without danger in cases where active electronics are integrated on the same chip. Rapid thermal annealing might provide a solution (see IC Compatibility, below).
- Undoped poly-Si films are in an amorphous state when deposited at 580°C or lower. The stress and the structure of this low-temperature material depend on temperature and partial pressure of the silane. A low-temperature anneal leads to a fine-grained poly-Si with low tensile stress and very smooth surface texture [Guckel et al., 1989]. Tensile rather than compressive films are a necessity if lateral dimensions of clamped structures are not to be restricted by compressive buckling. Conducting regions are formed in this case by ion implantation. Fine-grained and large-grained poly-Si are compared in more detail further below.

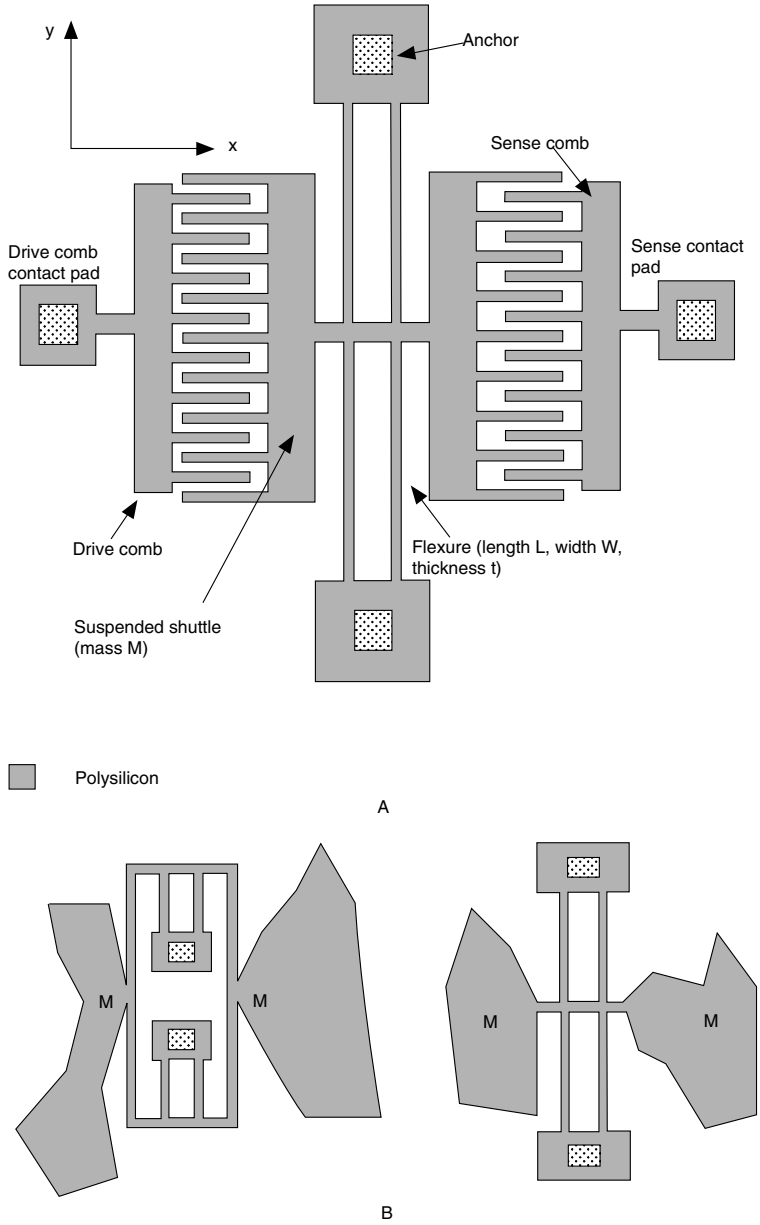


FIGURE 16.89 Layout of a lateral resonator with straight flexures. (A) Folded flexures (left) to release stress are compared with straight flexures (right). (B) M is shuttle mass.

- Phosphorus [Murarka and Retajczyk, 1983; Orpana and Korhonen, 1991; Lin et al., 1993], boron [Orpana and Korhonen, 1991; Choi and Hearn, 1984; Ding and Ko, 1991], arsenic [Orpana and Korhonen, 1991] and carbon [Hendriks et al., 1983] doping have all been shown to affect the state of residual stress in poly-Si films. In the case of single crystal Si, to compensate for strain induced by dopants, one can implant with atoms with the opposite atomic radius vs. silicon. Similar approaches would most likely be effective for poly-Si as well.
- Tang et al. (1990; 1989) developed a technique that sandwiches a poly-Si structural layer between a top and bottom layer of PSG and lets the high temperature anneal drive in the phosphorus symmetrically, producing low stress poly-Si with a negligible stress gradient.

- Another stress reduction method is to vary the materials composition, something readily done in CVD processes. An example of this method is the Si enrichment of Si_3N_4 which reduces the tensile stress [Sekimoto et al., 1982; Guckel et al., 1986].
- During plasma-assisted film deposition processes, one can influence stress dramatically. In a physical deposition process such as sputtering, stress control involves varying gas pressure and substrate bias. In plasma-enhanced chemical vapor deposition (PECVD) the RF power, through increased ion-bombardment, influences stress. In this way, the stress in a thin film starts out tensile, decreases as the power increases and finally becomes compressive with further RF power increase. PECVD equipment manufacturers also are working to build stress control capabilities into new equipment by controlling plasma frequency (see also Madou [1997, chap. 3]). In CVD, stress control involves all types of temperature treatment programs.
- A clever mechanical design might facilitate structural stress relief [Tang et al., 1989]. By folding the flexures in the lateral resonator in Figure 16.89B, and by the overall structural symmetry, the relaxation of residual polysilicon stress is possible without structural distortion. By folding the flexures, the resonant frequency, f_0, becomes independent of σ_r (see Eq. (16.59)). The springs in the resonator structure provide freedom of travel along the direction of the comb-finger motions (x) while restraining the structure from moving sideways (y), thus preventing the comb fingers from shorting out the drive electrodes. In this design, the spring constant along the y direction must be higher than along the x direction, i.e., $k_y \gg k_x$. The suspension should allow for the relief of the built-in stress of the polysilicon film and the axial stress induced by large vibrational amplitudes. The folded-beam suspensions meet both criteria. They enable large deflections in the x direction (perpendicular to the length of the beams) while providing stiffness in the y direction (along the length of the beams). Furthermore, the only anchor points (see Figure 16.89B) for the whole structure reside near the center, thus allowing the parallel beams to expand or contract in the y direction, relieving most of the built-in and induced stress [Tang, 1990]. Tang also modeled and built spiral and serpentine springs supporting torsional resonant plates. An advantage of the torsional resonant structures is that they are anchored only at the center, enabling radial relaxation of the built-in stress in the polysilicon film [Tang, 1990]. For some applications, the design approach with folded flexures is an attractive way to eliminate residual stress. However, a penalty for using flexures is increased susceptibility to out-of-plane warpage from residual stress gradients through the thickness of the polysilicon microstructure [Howe, 1995].
- Corrugated structural members, invented by Jerman for bulk micromachined sensors [Jerman, 1990], also reduce stress effectively. In the case of a single crystal Si membrane, stress may be reduced by a factor of 1000 to 10,000 [Spiering et al., 1991]. One of the applications of such corrugated structures is the decoupling of a mechanical sensor of its encapsulation, by reducing the influence of temperature changes and packaging stress [Spiering et al., 1991; Offereins et al., 1991]. Thermal stress alone can be reduced by a factor of 120 [Spiering et al., 1993]. Besides stress release, corrugated structures enable much larger deflections than do similar planar structures. This type of structural stress release was studied in some detail for single crystal Si [Zhang and Wise, 1994] (see also earlier in this chapter), polyimide [van Mullem et al. 1991] and LPCVD silicon nitride membranes [Scheeper et al., 1994]; but the quantitative influence of corrugated poly-Si structures still requires investigation. Figure 16.90 illustrates a fabrication sequence for a polyimide corrugated structure. The sacrificial Al in step 4 may be etched away by a mixture of phosphoric acidic: acetic acid: nitric acid (PAN, see Table 16.15).

16.13.4 Dimensional Uncertainties

The often-expressed concerns about run-to-run variability in material properties of polysilicon or other surface micromachined materials are somewhat misplaced, Howe points out [Howe, 1995]. He contrasts the relatively large dimensional uncertainties inherent to any lithography technique with poly-Si quality factors of up to 100,000 and long-term (>3 years) resonator frequency variation of less than 0.02 Hz.

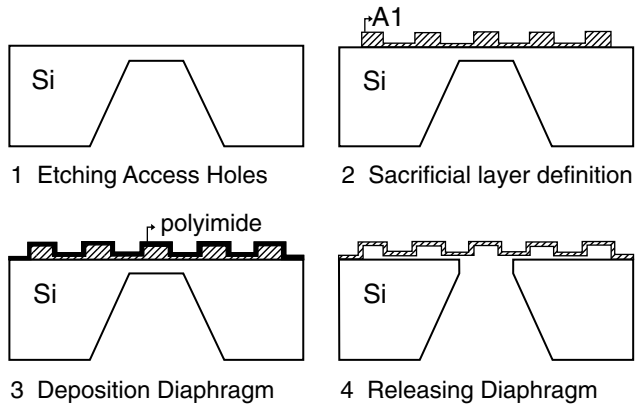


FIGURE 16.90 Schematic view of the fabrication process of a polyimide corrugated diaphragm. (From van Mullem, C.J. et al., Large Deflection Performance of Surface Micromachined Corrugated Diaphragms, presented at Transducers '91, San Francisco, CA, 1991. With permission.)

We follow his calculations here to prove the relative importance of the dimensional uncertainties. The shuttle mass M of a resonator as shown in Figure 16.89 is proportional to the thickness (t) of the polysilicon film, and neglecting the residual stress term, Eq. (16.59) reduces to:

$$f_0 \propto \left(\frac{W}{L}\right)^{\frac{3}{2}} \tag{16.60}$$

In case the residual stress term dominates in Eq. (16.59), the resonant frequency is expressed as:

$$f_0 \propto \left(\frac{W}{L}\right)^{\frac{1}{2}} \tag{16.61}$$

The width-to-length ratio is affected by systematic and random variations in the masking and etching of the microstructural polysilicon. For 2-μm-thick structural polysilicon, patterned by a wafer stepper and etched with a reactive-ion etcher, a reasonable estimate for the variation in linear dimension of etched features, Δ is about 0.2 μm (10% relative tolerance).

From Eq. (16.60) the variation Δ in lateral dimensions will result in an uncertainty δf_0 in the lateral frequency of:

$$\frac{\delta f_0}{f_0} \approx \frac{3}{2}\left(\frac{\Delta}{W}\right) \tag{16.62}$$

for a case where the residual stress can be ignored. With a nominal flexure width of $W = 2$ μm, the resulting uncertainty in resonant frequency is 15%. For the stress-dominated case, Eq. (16.61) indicates that the uncertainty is

$$\frac{\delta f_0}{f_0} \approx \frac{1}{2}\left(\frac{\Delta}{W}\right) \tag{16.63}$$

The same 2-μm-wide flexure would then lead to a 5% uncertainty in resonant frequency.

Interestingly, the stress-free case exhibits the most significant variation in the resonant frequency. In either case, resonant frequencies must be set by some postfabrication frequency trimming or other adjustment.

In Chapter 7 of Madou (1997) we draw further attention to the increasing loss of relative manufacturing tolerance with decreasing structure size (see Figure 7.1 in Madou [1997]).

16.13.5 Sealing Processes in Surface Micromachining

Sealing cavities to hermetically enclose sensor structures is a significant attribute of surface micromachining. Sealing cavities often embodies an integral part of the overall fabrication process and presents a desirable chip level, batch packaging technique. The resulting surface packages (microshells) are much smaller than typical bulk micromachined ones (see Madou [1997, chap. 8 on Packaging]).

16.13.6 IC Compatibility

Putting detection and signal conditioning circuits right next to the sensing element enhances the performance of the sensing system, especially when dealing with high impedance sensors. A key benefit of surface micromachining, besides small device size and single-sided wafer processing, is its compatibility with CMOS processing. IC compatibility implies simplicity and economy of manufacturing. In the examples at the end of this chapter we will discuss how Analog Devices used a mature 4-μm BICMOS process to integrate electronics with a surface micromachined accelerometer.

To develop an appreciation of integration issues involved in combining a CMOS line with surface micromachining, we highlight Yun's [Yun, 1992] comparison of CMOS circuitry and surface micromachining processes in Table 16.16A. Surface micromachining processes are similar to IC processes in several aspects. Both processes use similar materials, lithography and etching techniques. CMOS processes involve at least ten lithography steps where lateral small feature size plays an important role. Some processing steps, such as gate and contact patterning, are critical to the functionality and performance of the CMOS circuits. Furthermore, each processing step is strongly correlated with other steps. Change in any one of the processing steps will lead to modifications in a number of other steps in the process. In contrast, surface micromachining is relatively simple. It usually consists of two to six masks, and the feature sizes are much larger. The critical processing steps, such as structural poly-Si,

TABLE 16.16 Surface Micromachining and CMOS

A. Comparison of CMOS and Surface Micromachining

	CMOS	Surface Micromachining
Common features	Silicon-based processes; same materials, same etching principles	
Process flow	Standard	Application specific
Vertical dimension	~1 μm	~1–5 μm
Lateral dimension	<1 μm	2–10 μm
Complexity (# masks)	>10	2–6

B. Critical Process Temperatures for Microstructures

	Temperature (°C)	Material
LPCVD deposition	450	Low temperature oxide (LTO)/PSG
LPCVD deposition	610	Low stress poly-Si
LPCVD deposition	650	Doped poly-Si
LPCVD deposition	800	Nitride
Annealing	950	PSG densification
Annealing	1050	Poly-Si stress annealing

(After Yun, W., A Surface Micromachined Accelerometer with Integrated CMOS Detection Circuitry, Ph.D. Thesis, U.C. Berkeley, 1992.)

often are self-aligned which eliminates lithographic alignment. The CMOS process is mature, quite generic and fine-tuned, while surface micromachining strongly depends on the application and still needs maturing.

Table 16.16B presents the critical temperatures associated with the LPCVD deposition of a variety of frequently used materials in surface micromachining. Polysilicon is used for structural layers and thermal SiO_2, LPCVD SiO_2 and PSG are used as sacrificial layers; silicon nitride is used for passivation. The highest temperature process in Table 16.16B is 1050°C and is associated with the annealing step to release stress in the polysilicon layers. Doped polysilicon films deposited by LPCVD under conventional IC conditions usually are in a state of compression that can cause mechanically constrained structures such as bridges and diaphragms to buckle. The annealing step above about 1000°C promotes crystallite growth and reduces the strain. If one wants to build polysilicon microstructures after the CMOS active electronics have been implemented (a so-called post-CMOS procedure), one has to avoid temperatures above 950°C, as junction migration will take place at those temperatures. This is especially true with devices incorporating shallow junctions where migration might be a problem at temperatures as low as 800°C. The degradation of the aluminum metallization presents yet a bigger problem. Aluminum typically is used as the interconnect material in the conventional CMOS process. At temperatures of 400 to 450°C, the aluminum metallization will start suffering. Anneal temperatures (densification of the PSG and stress anneal of the poly-Si) only account for some of the concerns; in general, several compatibility issues must be considered: (1) deposition and anneal temperatures, (2) passivation during micromachining etching steps and (3) surface topography.

Yun (1992) compared three possible approaches to build integrated microdynamic systems: pre-, mixed and post-CMOS microstructural processes as shown in Figure 16.91. He concluded that building up the microstructures after implementation of the active electronics offers the best results.

In a post-CMOS process, the electronic circuitry is passivated to protect it from the subsequent micromachining processes. The standard IC processing may be performed at a regular IC foundry, while the surface micromachining occurs as an add-on in a specialized sensor fabrication facility. LPCVD silicon nitride (deposited at 800°C, see Table 16.16B) is stable in HF solutions and is the preferred passivation layer for the IC during the long release etching step. PECVD nitride can be deposited at around 320°C, but it displays relatively poor step coverage, while pin holes in the film allow HF to diffuse through and react with the oxide underneath. LPCVD nitride is conformably deposited. While it shows fewer pin holes, circuitry needs to be able to survive the 800°C deposition temperature.

Aluminum metallization must be replaced by another interconnect scheme in order to raise the post-CMOS temperature ceiling higher than 450°C. Tungsten, which is refractory, shows low resistivity and has a thermal expansion coefficient matching that of Si, is an obvious choice. One problem with tungsten metallization is that tungsten reacts with silicon at about 600°C to form WSi_2, implying the need for a diffusion barrier. The process sequence for the tungsten metallization developed at Berkeley is shown in Figure 16.92. A diffusion barrier consisting of $TiSi_2$ and TiN is used. The TiN film forms during a 30-sec sintering step to 600°C in N_2. Rapid thermal annealing with its reduced time at high temperatures (10 sec to 2 min) and high ramp rates (~150°C/sec) allows very precise process control as well as a dramatic reduction of thermal budgets, reducing duress for the active on-chip electronics. Titanium silicide is formed at the interface of titanium and silicon while titanium nitride forms simultaneously at the exposed surface of the titanium film. The $TiSi_2$/TiN forms a good diffusion barrier against the formation of WSi_2 and at the same time provides an adhesion and contact layer for the W metallization.

To avoid the junction migration in a post-CMOS process, rapid thermal annealing is used for both the PSG densification and polysilicon stress anneal: 950°C for 30 sec for the PSG densification and 1000°C for 60 sec for the stress anneal of the poly-Si. Alternatively, one could consider the use of fine-grained polysilicon which can yield a controlled tensile strain with low-temperature annealing [Guckel et al., 1988].

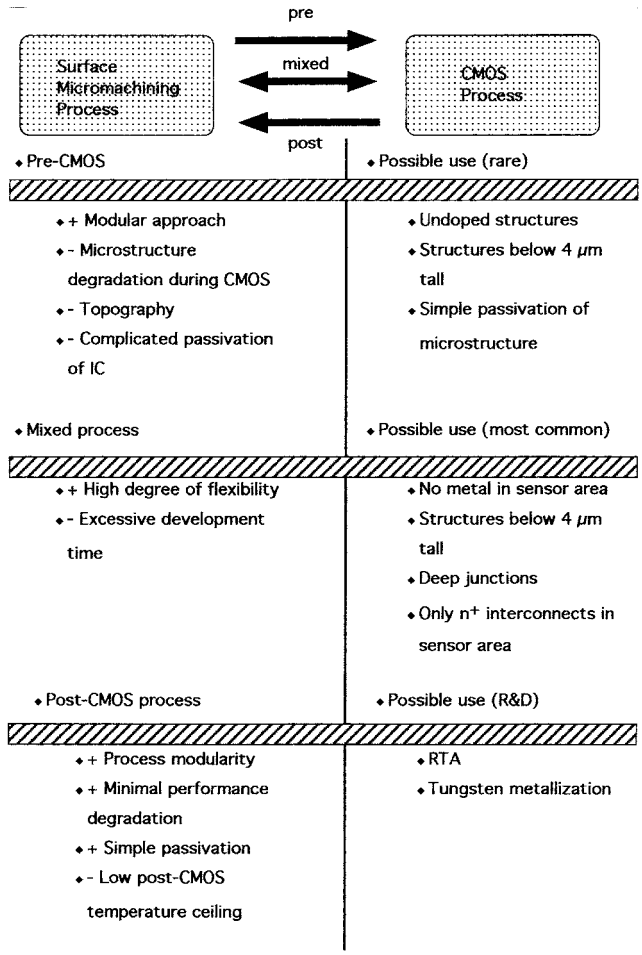


FIGURE 16.91 Comparison of various options for process integration. (Adapted from Yun, W., A Surface Micromachined Accelerometer with Integrated CMOS Detection Circuitry, Ph.D. thesis, University of California, Berkeley, 1992. With permission.)

Despite some advantages the post-CMOS process with tungsten metallization is not the preferred implementation. Hillock formation in the W lines during annealing and high contact resistance remain problems [Howe, 1995]. Moreover, the finely tuned CMOS fabrication sequence may also be affected by the heavily doped structural and sacrificial layers.

The mixed CMOS/micromachining approach implements a processing sequence which puts the processes in a sequence to minimize performance degradation for both electronic and mechanical components. According to Yun this requires significant modifications to the CMOS fabrication sequence. Nevertheless, Analog Devices relied on such an interleaved process sequence to build the first commercially available integrated micro-accelerometer (see Example 1). The modifications required on a standard BICMOS line were minimal: to facilitate integration of the IC and to surface micromachine the thickness of deposited microstructural films the line was limited to 1 to 4 μm. Relatively deep junctions permitted thermal processing for the sensor poly-Si anneal and interconnections to the sensor were made only via n^+ underpasses. No metallization is present in the sensor area. This industrial solution remains truer to the traditional IC process experience than the post-CMOS procedure. Howe recently detailed another example of such a mixed process [Howe, 1995]. In Howe's scenario, the micromachining sequence is inserted after the completion of the electronic

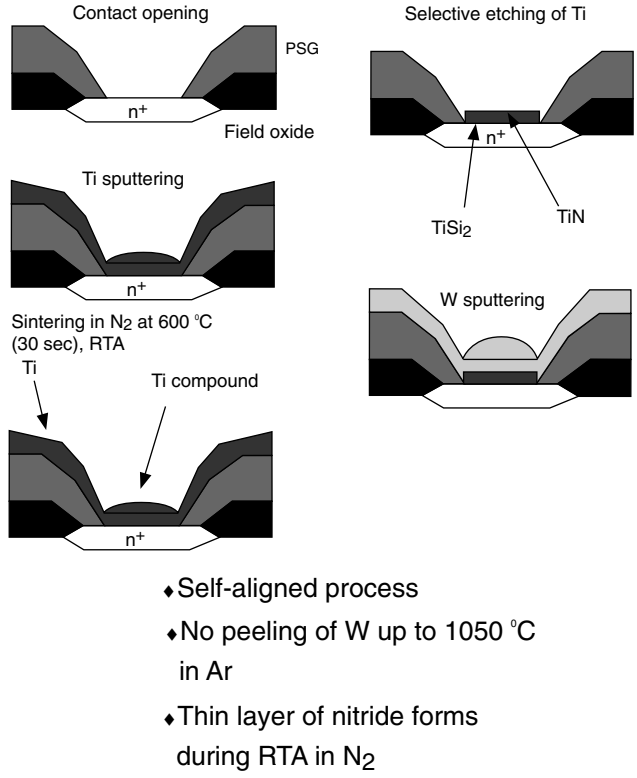


FIGURE 16.92 Tungsten metallization process in a modified CMOS process. (Adapted from Yun, W., A Surface Micromachined Accelerometer with Integrated CMOS Detection Circuitry, Ph.D. thesis, University of California, Berkeley, 1992. With permission.)

structures, but prior to contact etching or aluminum metallization. By limiting the polysilicon annealing to 7 min at 900°C, only minor dopant redistribution is expected. Contact and metallization lithography and etching become more complex now due to the severe topography of the poly-Si microstructural elements.

The pre-CMOS approach is to fabricate microstructural elements before any CMOS process steps. At first glance this seems like an attractive approach as no major modifications would be needed for process integration. However, due to the vertical dimensions of microstructures, step coverage is a problem for the interconnection between the sensor and the circuitry (the latest approach introduced by Howe faces the same dilemma). Passivation of the microstructure during the CMOS process can also become problematic. Furthermore, the fine-tuned CMOS fabrication sequence, such as gate oxidation, can be affected by the heavily doped structural layers. Consequently, this approach is only used for some special applications [Yun, 1992].

A unique pre-CMOS process was developed at Sandia National Labs [Smith et al., 1995]. In this approach, micromechanical devices are fabricated in a trench etched in a Si epilayer. After the mechanical components are complete, the trench is filled with oxide, planarized using chemical-mechanical polishing (CMP) (see Madou [1994, chap. 3]) and sealed with a nitride membrane. The flat wafer with the embedded micromechanical devices is then processed by means of conventional CMOS processing. Additional steps are added at the end of the CMOS process in order to expose and release the embedded micromechanical devices.

The SPIE "Smart Structures and Materials 1996" meeting in San Diego, CA, had two complete sessions dedicated to the crucial issue of integrating electronics with polysilicon surface micromachining [Varadan and McWhorter, 1996].

16.14 Poly-Si Surface Micromachining Modifications

16.14.1 Porous Poly-Si

In the first part of this chapter we discussed the transformation of single crystal Si into a porous material with porosity and pore sizes determined by the current density, type and concentration of the dopant and the hydrofluoric acid concentration. A transition from pore formation to electropolishing is reached by raising the current density and/or by lowering the hydrofluoric acid concentration [Memming and Schwandt, 1966; Zhang et al., 1989]. Porous silicon can also be formed under similar conditions from LPCVD poly-Si [Anderson et al., 1994]. In this case pores roughly follow the grain boundaries of the polysilicon. Figure 16.93 illustrates the masking and process sequence to prepare a wafer to make thin layers of porous Si between two insulating layers of low stress silicon nitride [Field, 1987]. The wafer, after the process steps outlined in Figure 16.93, is put in a Teflon test fixture, protecting the back from HF attack. An electrical contact is established on the back of the wafer and a potential is applied with respect to a Pt-wire counterelectrode immersed in the same HF solution. Electrolytes consisting of 5 to 49% HF (wt) and current densities from 0.1 to 50 A cm^{-2} are used. The advance of a pore-etching front, growing parallel to the wafer surface, may be monitored using a line-width measurement tool. The highest observed rate of porous-silicon formation is 15 μm min^{-1} (in 25%, wt HF). In the electro-polishing regime, at the highest currents, the etch rate is diffusion limited but the reaction is controlled by surface reaction kinetics in the porous Si growth regime.

By changing the conditions from pore formation to electropolishing and back to porous Si, an enclosed chamber may be formed with porous poly-Si walls (plugs) and 'floor and ceiling' silicon nitride layers. Sealing of the cavities by clogging the microporous poly-Si was attempted by room temperature oxidation in air and in a H_2O_2 solution. Leakage through the porous plug persisted after those room temperature oxidation treatments, but with a Ag deposition from a 400-m*M* $AgNO_3$ solution and subsequent atmospheric tarnishing (48 h, Ag_2S) the chambers appeared to be sealed, as determined from the lack of

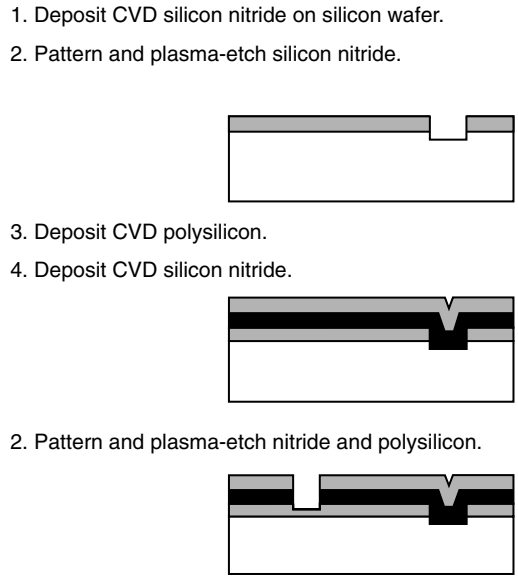


FIGURE 16.93 Masking and process sequence preparing a wafer for laterally grown porous polysilicon. (From Field, L., *Low-Stress Nitrides for Use in Electronic Devices* (University of California, Berkeley, 1987), pp. 42 and 43. With permission.)

penetration by methanol. This technology might open up possibilities for filling cavities with liquids and gases under low-temperature conditions. The chamber provided with a porous plug might also make a suitable on-chip electrochemical reference electrolyte reservoir.

Hydrofluoric acid can penetrate thin layers of poly-Si either at foreign particle inclusion sites, or at other critical film defects such as grain boundaries (see above). This way the HF can etch underlying oxide layers, creating, for example, circular regions of free-standing poly-Si, so-called 'blisters.' The poly-Si permeability associated with blistering of poly-Si films has been applied successfully by Judy and Howe (1993a; 1993b) to produce thin-shelled hollow beam electrostatic resonators from thin poly-Si films deposited onto PSG. The possible advantage of using these hollowed structures is to obtain a yet higher resonator quality factor Q. The devices were made in such a way that the 0.3-μm-thick undoped poly-Si completely encased a PSG core. After annealing, the structures were placed in HF which penetrated the poly-Si shell and dissolved away the PSG, eliminating the need for etch windows. It was not possible to discern the actual pathways through the poly-Si using TEM.

Lebouitz et al. (1995) apply permeable polysilicon etch-access windows to increase the speed of creating microshells for packaging surface micromachined components. After etching the PSG through the many permeable Si windows, the shell is sealed with 0.8 μm of low stress LPCVD nitride.

16.14.2 Hinged Polysilicon

One way to achieve high vertical structures with surface micromachining is building large flat structures horizontally and then rotating them on a hinge to an upright position. Pister et al. [Burgett et al., 1992; Ross and Pister, 1994; Lin et al., 1995; Yeh et al., 1994; Lin et al., 1996] developed the poly-Si hinges shown in Figure 16.94A; on these hinges, long structural poly-Si features (1 mm and beyond) can be rotated out of the plane of a substrate. To make the hinged structures, a 2-μm-thick PSG layer (PSG-1) is deposited on the Si substrate as the sacrificial material, followed by the deposition of the first polysilicon layer (2-μm-thick poly-1). This structural layer of polysilicon is patterned by photolithography and dry etching to form the desired structural elements, including hinge pins to rotate them. Following the deposition and patterning of poly-1, another layer of sacrificial material (PSG-2) of 0.5-μm thickness is deposited. Contacts are made through both PSG layers to the Si substrate, and a second layer of polysilicon is deposited and patterned (poly-2), forming a staple to hold the first polysilicon layer hinge to the surface. The first and second layers of poly are separated everywhere by PSG-2 in order for the first polysilicon layer to freely rotate off the wafer surface when the PSG is removed in a sacrificial etch. After the sacrificial etch, the structures are rotated in their respective positions. This is accomplished in an electrical probe station by skillfully manipulating the movable parts with the probe needles. Once the components are in position, high friction in the hinges tends to keep them in the same position. To obtain more precise and stable control of position, additional hinges and supports are incorporated. To provide electrical contact to the vertical poly-Si structures one can rely on the mechanical contact in the hinges, or poly-Si beams (cables) can be attached from the vertical structure to the substrate.

Pister's research team made a wide variety of hinged microstructures, including hot wire anemometers, a box dynamometer to measure forces exerted by embryonic tissue, a parallel plate gripper [Burgett et al., 1992], a micro-windmill [Ross and Pister, 1994], a micro-optical bench for free-space integrated optics [Lin et al., 1995] and a standard CMOS single piezoresistive sensor to quantify rat single heart cell contractile forces [Lin et al., 1996]. One example from this group's efforts is illustrated in Figure 16.94B, showing an SEM photograph of an edge-emitting laser diode shining light onto a collimating micro-Fresnel lens [Lin et al., 1995]. The micro-Fresnel lens in the SEM photo is surface micromachined in the plane and erected on a polysilicon hinge. The lens has a diameter of 280 μm. Alignment plates at the front and the back sides of the laser are used for height adjustment of the laser spot so that the emitting spot falls exactly onto the optical axis of the micro-Fresnel lens. After assembly, the laser is electrically contacted by silver epoxy. Although this hardly outlines standard IC manufacturing practices, excellent collimating ability for the Fresnel lenses has been achieved. The eventual goal of this work is a micro-optical bench (MOB) in which microlenses, mirrors, gratings and other optical components are pre-aligned in the mask

layout stage using computer-aided design. Additional fine adjustment would be achieved by on-chip micro-actuators and micropositioners such as rotational and translational stages.

Today, erecting these poly-Si structures with the probes of an electrical probe station or, occasionally, assembly by chance in the HF etch or deionized water rinse represent too complicated or too unreliable postrelease assembly methods for commercial acceptance.

Friction in poly-Si joints, as made by Pister, is high because friction is proportional to the surface area (s^2) and becomes dominant over inertial forces (s^3) in the microdomain (see Madou [1997, chap. 9]). Such joints are not suitable for microrobotic applications. Although attempts have been made to incorporate poly-Si hinges in such applications [Yeh et al., 1994], plastically deformable hinges make more sense for microrobot machinery involving rotation of rigid components. Noting that the external skeleton of insects incorporates hard cuticles connected by elastic hinges, Suzuki et al. (1994) fabricated rigid

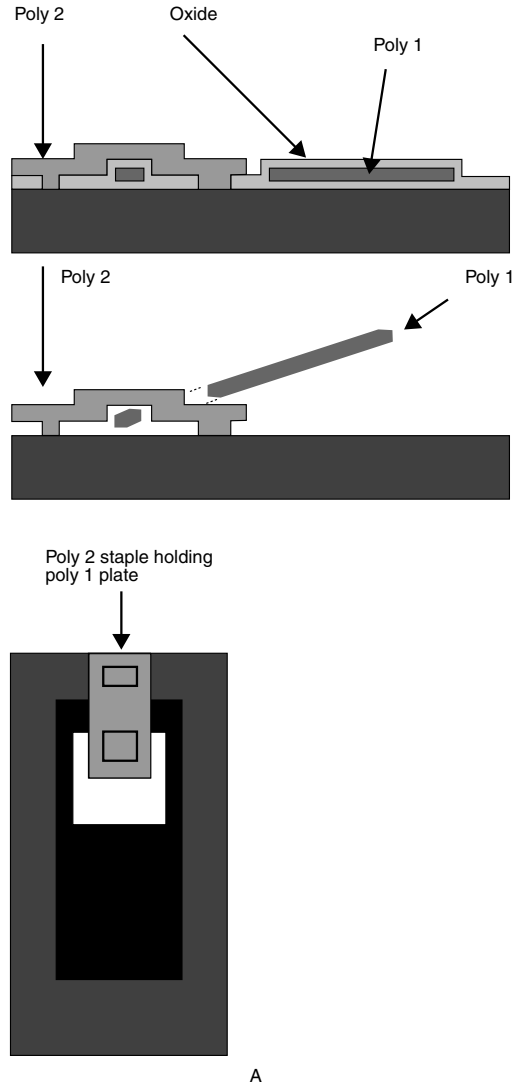
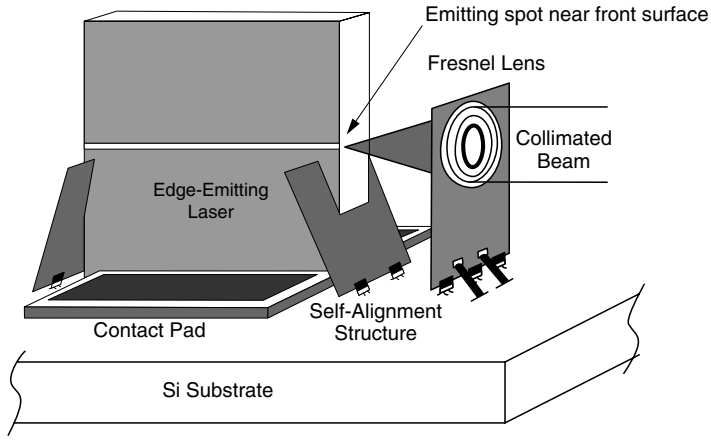
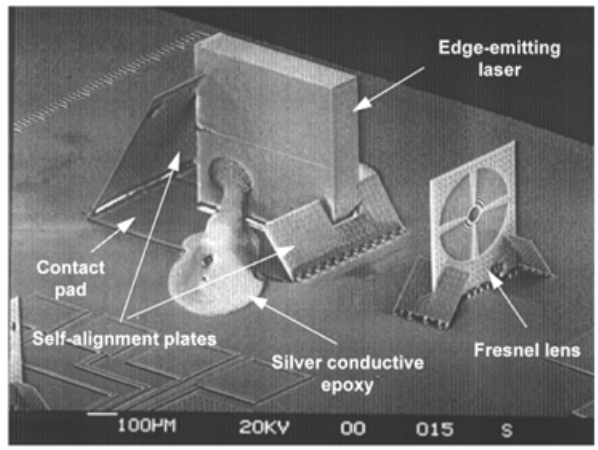


FIGURE 16.94 Microfabricated hinges. (A) Cross-section, side view and top view of a single-hinged plate before and after the sacrificial etch. (B) Schematic (top) and SEM micrograph of the self-aligned hybrid integration of an edge-emitting laser with a micro-Frensnel lens. (From Lin, L.Y. et al., Micromachined Integrated Optics for Free-Space Interconnections, presented at MEMS '96, Amsterdam, 1995. With permission.)





B

FIGURE 16.94 (Continued).

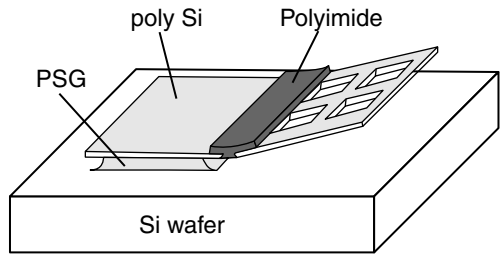


FIGURE 16.95 Flexible polyimide hinge and poly-Si plate (butterfly wing). (From Suzuki, K. et al., *J. Microelectromech. Syst.*, 3, 4–9, 1994. With permission.)

poly-Si plates (E = 140 GPa) connected by elastic polyimide hinges (E = 3 GPa) as shown in Figure 16.95 (see also section below on Polimide Surface Structures). Holes in the poly-Si plates shorten the PSG etch time compared to plates without holes. The plates without holes remain attached to the substrate while the ones with holes are completely freed. Using electrostatic actuators, a structure as shown in Figure 16.95 can be made to flap like the wing of a butterfly. By applying an AC voltage of 10 kHz, resonant vibration of such a flapping wing was observed [Suzuki et al., 1994].

More recently, Hoffman et al. (1995) demonstrated aluminum plastically deformable hinges on oxide movable thin plates. Oxide plates and Al hinges were etched free from a Si substrate by using XeF_2, a vapor phase etchant exhibiting excellent selectivity of Si over Al and oxide. According to the authors, this process, due to its excellent CMOS compatibility, might open the way to designing and fabricating sophisticated integrated CMOS-based sensors with rapid turnaround time (see also Madou [1997, chap. 2]).

16.14.3 Thick Polysilicon

Applying classical LPCVD to obtain poly-Si deposition is a slow process. For example, a layer of 10 μm typically requires a deposition time of 10 hr. Consequently, most micromachined structures are based on layer thicknesses in the 2- to 5-μm range. Basing their process on dichlorosilane (SiH_2Cl_2) chemistry, Lange et al. (1995) developed a CVD process in a vertical epitaxy batch reactor with deposition rates as high as 0.55 μm/min at 1000°C. The process yields acceptable deposition times for thicknesses in the 10-μm range (20 min). The highly columnar poly-Si films are deposited on sacrificial SiO_2 layers and exhibit low internal tensile stress making them suitable for surface micromachining. The surface roughness comprises about 3% of the thickness, which might preclude some applications.

Kahn et al. (1996) made mechanical property test structures from thick undoped and *in situ* B-doped polysilicon films. The elastic modulus of the B-doped polysilicon films was determined as 150 ± 30 GPa. The residual stress of as-deposited undoped thick polysilicon was determined as 200 ± 10 MPa.

16.14.4 Milli-Scale Molded Polysilicon Structures

The assembly of tall three-dimensional features in the described hinged polysilicon approach is complicated by the manual assembly of the fabricated microparts resembling building a miniature boat in a bottle. Keller at University of California, Berkeley, came up with an elegant alternative for building tall, high-aspect-ratio microstructures in a process that does not require postrelease assembly steps [Keller and Ferrari, 1994]. The technique involves deep dry etching of trenches in a Si substrate, deposition of sacrificial and structural materials in those trenches, and demolding of the deposited structural materials by etching away the sacrificial materials. CVD processes can typically only deposit thin films (~1 to 2 μm) on flat surfaces. If, however, these surfaces are the opposing faces of deep narrow trenches, the growing films will merge to form solid beams. In this fashion, high-aspect-ratio structures that would normally be associated with LIGA now also can be made of CVD polysilicon. The procedure is illustrated in Figure 16.96 [Keller and Ferrari, 1994; Keller and Howe, 1995]. The first step is to etch deep trenches into a silicon wafer. The depth of the trenches equals the height of the desired beams and is limited to about 100 μm with aspect ratios of about 10 (say, a 10-μm-diameter hole with a depth of 100 μm). For trench etching, Keller uses a Cl_2 plasma etch with the following approximate etching conditions: flow rates of 200 sccm for He and 180 sccm for Cl_2, a working pressure of 425 mTorr, a power setting of 400 W and an electrode gap of 0.8 cm. The etch rate for Si in this mode equals 1 μm/min. Thermal oxide and CVD oxide act as masks with 1 μm of oxide needed for each 20 μm of etch depth. Before the Cl_2 etch a short 7-sec SF_6 pre-etch removes any remaining native oxide in the mask openings. During the chlorine etch a white sidewall passivating layer must be controlled to maintain perfect vertical sidewalls. After every 30 min of plasma etching, the wafers are submerged in a silicon isotropic etch long enough to remove the residue [Keller and Howe, 1995]. Beyond 100 μm, severe undercutting occurs and the trench cross section becomes sufficiently ellipsoidal to prevent molded parts from being pulled out. Advances in dry cryogenic etching are continually improving attainable etch depths, trench profiles and minimum trench diameter. We can expect continuous improvements in the tolerances of this novel technique. After plasma etching, an additional 1 μm of silicon is removed by an isotropic wet etch to obtain a smoother trench wall surface. Alternatively, to smooth sidewalls and bottom of the trenches a thermal wet oxide is grown and etched away. The sacrificial oxide in step 2 is made by CVD phosphosilicate glass (PSG

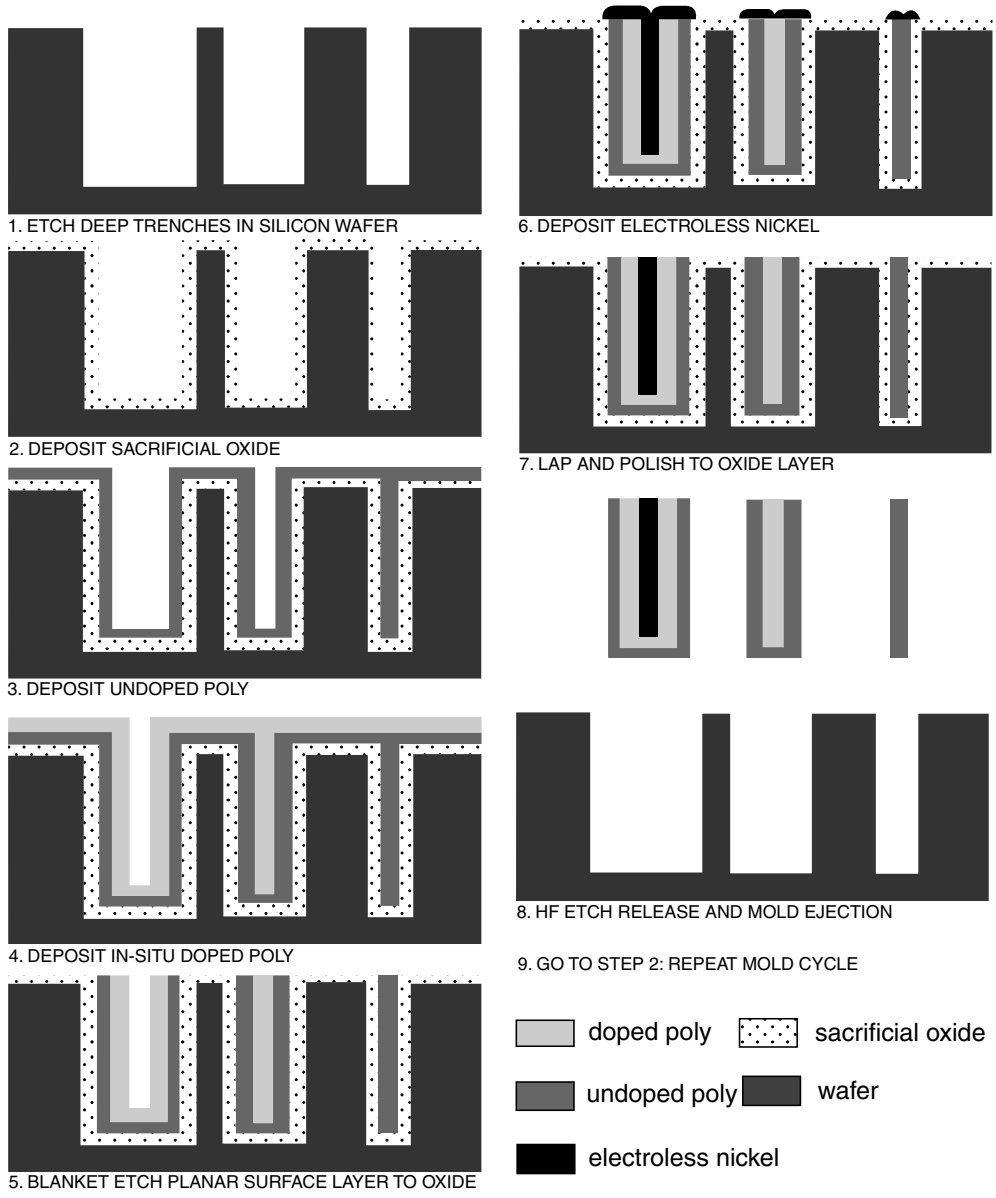


FIGURE 16.96 Schematic illustration of HEXSIL process. The mold wafer may be part of an infinite loop. (From Keller and Ferrari [1994]. Courtesy of Mr. C. Keller.)

at 450°C, 140 Å/min), CVD low-temperature oxide (LTO at 450°C) or CVD polysilicon (580°C, 65 Å/min). The latter is completely converted to SiO_2 by wet thermal oxidation at 1100°C. The PSG needs an additional reflowing and densifying anneal at 1000°C in nitrogen for 1 hr. This results in an etching rate of the sacrificial layer of ~20 μm/min in 49% HF. The mold shown in Figure 16.96 displays three different trench widths and can be used to build integrated micromachines incorporating doped and undoped poly-Si parts as well as metal parts. The remaining volume of the narrowest trench after oxide deposition is filled completely with the first deposition of undoped polysilicon (poly 1) in step 3. The undoped poly will constitute the insulating regions in the micromachine. Undoped CVD polysilicon was formed in this case at 580°C, with a 100 SCCM silane flow rate, and

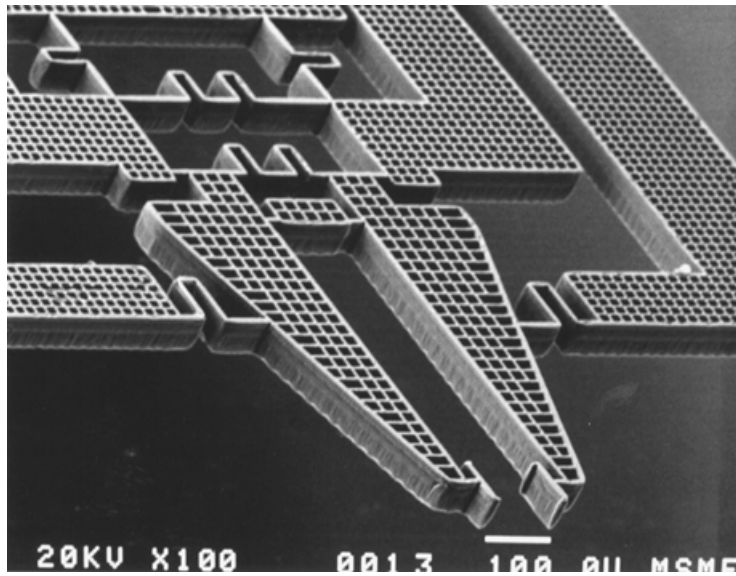


FIGURE 16.97 SEM micrograph of HEXSIL tweezers: 4 mm long, 2 mm wide and 80 μm tall. Lead wires for current supply are made from Ni-filled poly-Si beams; *in situ* phosphorus-doped polysilicon provides the resistor part for actuation. The width of the beam is 8 μm: 2 μm poly-Si, 4 μm Ni, and 2 μm poly-Si. (Courtesy of Mr. C. Keller.)

a 300-mTorr reactor pressure, resulting in a deposition rate of 0.39 μm/hr. The deposited film under these conditions is amorphous or very fine-grained. Since the narrowest trenches are completely filled in by the first deposition, they cannot accept material from later depositions. The trenches of intermediate width are lined with the first material and then completely filled in by the second deposition. In the case illustrated the second deposition (step 4) consists of *in situ* doped poly-Si and forms the resistive region in the micromachine under construction. To prevent diffusion of P from the doped poly deposited on top of the narrow undoped beams, a blanket etch in step 5 is used to remove the doped surface layer prior to the anneal of the doped poly. The third deposition, in step 6 of the example case, consists of electroless nickel plating on poly-Si surfaces but not on oxides surfaces and results in the conducting parts of the micromachine. By depositing structural layers in order of increasing conductivity, as done here, regions of different conductivity can be separated by regions of narrow trenches containing only nonconducting material. Lapping and polishing in step 7 with a 1-μm diamond abrasive in oil planarizes the top surface, readying it for HF etch release and mold ejection in step 8. Annealing of the polysilicon is required to relieve the stress before removing the parts from the wafer so they remain straight and flat. In step 8 the sacrificial oxide is dissolved in 49% HF. A surfactant such as Triton X100 is added to the etch solution to facilitate part ejection by reducing surface adhesion between the part and the mold. The parts are removed from the wafer, and the wafer may be returned to step 2 for another mold cycle. An example micromachine, resulting from the described process, is the thermally actuated tweezers shown in Figure 16.97. These HEXSIL tweezers measure 4 mm long, 2 mm wide and 80 μm tall. The thermal expansion beam to actuate the tweezers consists of the *in situ* doped poly-Si; the insulating parts are made from the undoped poly-Si material. Ni-filled poly-Si beams are used for the current supply leads. It is possible to combine the HEXSIL process with classical poly-Si micromachining, as illustrated in Figure 16.98, where HEXSIL forms a stiffening rib for a membrane filter fashioned by surface micromachining of a surface poly-Si layer. The surface poly-Si is deposited after HEXSIL. A critical need in HEXSIL technology is controlled mold ejection. Keller and Howe (1995) have experimented with HEXSIL-produced bimorphs, making the structure spring up after release.

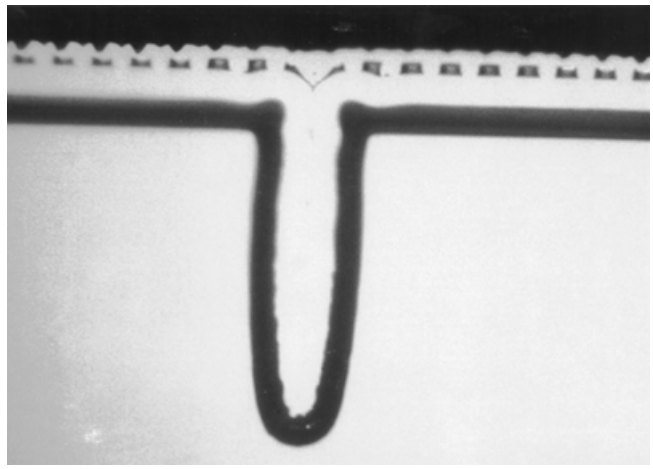


FIGURE 16.98 SEM micrograph of surface micromachined membrane filter with a stiffening rib (50 μm high). Original magnification 1000×. (Courtesy of Mr. C. Keller.)

16.15 Non-Poly-Si Surface Micromachining Modifications

16.15.1 Silicon on Insulator Surface Micromachining

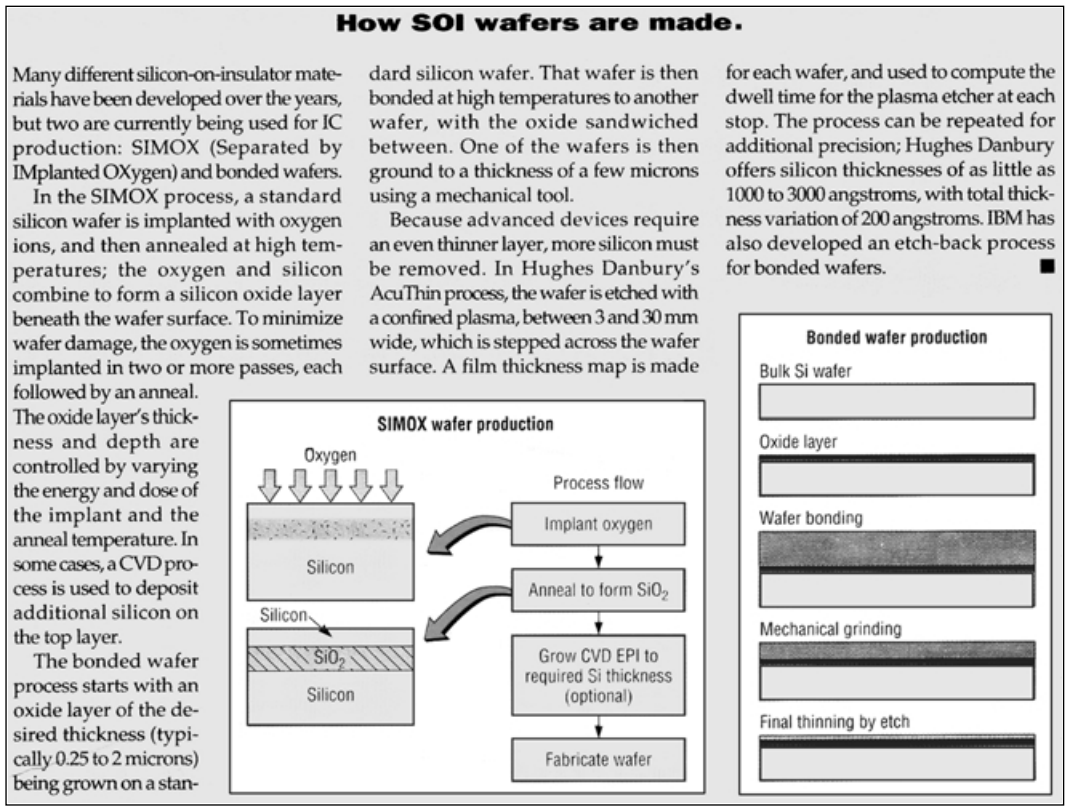
16.15.1.1 Introduction

A major sensor use of silicon on insulator wafers is established in the production of high-temperature sensors. Compared to p-n junction isolation, which is limited to about 125°C, much higher temperature devices are possible based on the dielectric insulation of SOI. Recently, a wide variety of SOI surface micromachined structures have been explored, including pressure sensors, accelerometers, torsional micromirrors, light sources, optical choppers etc. [Diem et al., 1993; Noworolski et al., 1995]

Three major techniques currently are applied to produce ***SOI*** wafers (see also under Epitary in Madou [1997, chap. 3]): ***SIMOX*** (Separated by IMplanted OXygen), the Si fusion bonded (SFB) wafer technique and zone-melt recrystallized (ZMR) polysilicon. With SIMOX, standard Si wafers are implanted with oxygen ions and then annealed at high temperatures (1300°C). The oxygen and silicon combine to form a silicon oxide layer beneath the silicon surface. The oxide layer's thickness and depth are controlled by varying the energy and dose of the implant and the anneal temperature. In some cases, a CVD process deposits additional epitaxial silicon on the top silicon layer. Attempts have also been made to implant nitrogen in Si to create abrupt etch stops. At high enough energies the implanted nitrogen is buried 1/2 to 1 μm deep. At a high enough dose, the etching in that region stops. It is not necessary to implant the stoichiometric amount of nitrogen concentration; a dose lower by a factor of 2 to 3 suffices. After implantation, it is necessary to anneal the wafer because the implantation destroys the crystal structure at the surface of the wafer.

The bonded wafer process starts with an oxide layer grown (typically about 1 μm) on a standard Si wafer. That wafer is then bonded to another wafer, with the oxide sandwiched between. For the bonding no mechanical pressure or other forces are applied. The sandwich is annealed at 1100°C for 2 hr in a nitrogen ambient leading to a strong binding between the two wafers. One of the wafers is then ground to a thickness of a few microns using mechanical and CMP.

A third process for making SOI structures is to recrystallize polysilicon (e.g., with a laser, an electron-beam or a narrow strip heater) deposited on an oxidized silicon wafer. This process is called zone melting recrystallization (ZMR). This technique is used primarily for local recrystallization and has not yet been explored much in micromachining applications.



From Dunn, P.N., *Solid State Technol.*, October, 32–35 (1993). With permission.

The crystalline perfection of conventional silicon wafers in SFB and ZMR is completely maintained in the SOI layer as the wafers do not suffer from implant-induced defects. By using plasma etching, wafers with a top Si layer thickness of as little as 1000 to 3000 Å with total thickness variations of less than 200 Å can be made [Dunn, 1993]. SOI layers of 2 μm thick are more standard [Abe and Matlock, 1990].

Kanda (1991) reviews different types of SOI wafers in terms of their micromachining and IC applications. Working with SOI wafers offers several advantages over bulk Si wafers: fewer process steps are needed for feature isolation, parasitic capacitance is reduced, and power consumption is lowered. In the IC industry these wafers are used for high-speed CMOS ICs, smart power ICs, three-dimensional ICs, and radiation-hardened devices [Kuhn and Rhee, 1973]. In micromachining, SOI wafers are employed to produce an etch stop in such mechanical devices as pressure and acceleration sensors and in high-temperature sensors, and ISFETs. Etched-back fusion-bonded Si wafers and SIMOX are already employed extensively to build micromachines. The two types of SOI wafers are commercially available. A tremendous amount of effort is spent in the IC industry on controlling the SOI thin Si layer thickness which will benefit any narrow tolerance micromachine. The silicon fusion bonded (SFB) method offers the more versatile MEMS approach due to the associated potential for thicker single crystal layers and the option of incorporating buried cavities, facilitating micromachine packaging. Sensors manufactured by means of SFB now are commercially available [Pourahmadi et al., 1992]. The SIMOX approach is less labor intensive and holds better membrane thickness control. An important expansion of the SOI technique is selective epitaxy. The latter enables a wide range of new mechanical structures (see Madou [1997, chap. 3]) and enables novel etch-stop methods [Gennissen et al., 1995], as well as electrical and/or thermal separation and independent

optimization of active sensor and readout electronics [Bartek et al., 1995]. In all cases SOI machining involves dry anisotropic etching to etch a pattern into the Si layer on top of the insulator. These structures then become free by etching the sacrificial buried SiO_2 insulator layer, which displays a thickness with very high reproducibility (400 ± 5 nm) and uniformity (<±5 nm), especially in the case of SIMOX. Etched free cantilevers and membranes consist of single crystalline silicon with thicknesses ranging from microns and submicrons (SIMOX) up to hundreds of microns (SFB). Below we review three implementations of SOI techniques that may be crucial for future MEMS development.

16.15.1.2 Silicon Fusion Bonded Micromachining

Silicon fusion bonding enables the formation of thick single crystal layers with cavities built in. An example is shown in Figure 16.99 [Noworolski et al., 1995]. The device pictured involves two 4-in. <100> wafers: a handle wafer and a wafer used for the SOI surface. The p-type (3 to 7 Ωcm) handle wafer is thermally oxidized at 1100°C to obtain a 1-μm-thick oxide. Thermal oxidation enables thicker oxides than the ones formed in SIMOX by ion implantation and avoids the potential implantation damage in the working material. To make a buried cavity, the oxide is patterned and etched. To produce yet deeper cavities, the Si handle wafer may be etched as well (as in Figure 16.99). In the case shown, the top wafer consists of the same p-type substrate material as the handle wafer with a 2- to 30-μm-thick n-type epitaxial layer. The epitaxial layer determines the thickness of the final mechanical material. The epitaxial layer is fusion bonded to the cavity side of the handle wafer (2 hr at 1100°C). The top wafer is then partially thinned by grinding and polishing (Figure 16.99A). An insulator is deposited and patterned on the back side of the handle wafer to etch access holes to the insulator. After the insulator at the bottom of the etch hole is removed by a buffered oxide etch (BOE), aluminum is sputtered and sintered to make contact to the n-type epilayer for the electrochemical etch back of the remaining p-type material (Figure 16.99B). The final single crystal silicon thickness is uniform to within ±0.05 μm (std. dev.) and does not require a costly, high accuracy polish step.

Draper Laboratory is using SOI processes in the development of inertial sensors, gyros and accelerometers as an alternative to their current devices fabricated by the dissolved wafer process (see Example 1, Section 16.9). The main advantage is that the former consists of an all Si process rather than a Si/Pyrex sandwich [Greiff, 1995].

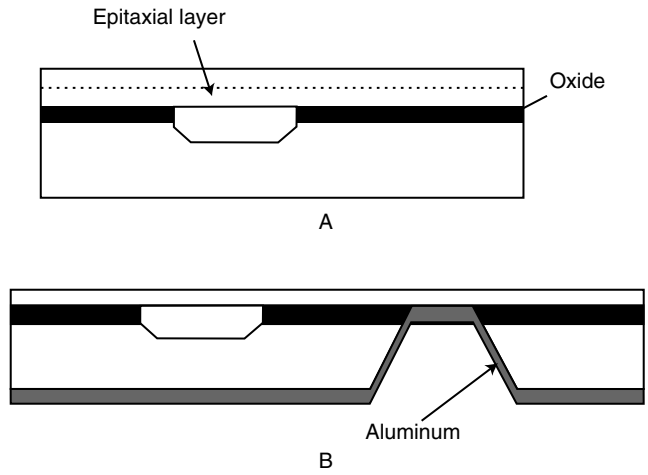


FIGURE 16.99 (A) A wafer sandwich after grind-and-polish step. (B) A wafer after electrochemical etch-back in KOH, buried oxide removal and aluminum deposition. (From Noworolski, J.M. et al., Fabrication of SOI Wafers with Buried Cavities Using Silicon Fusion Bending and Electrochemical Etchback, presented at Transducers '95, Stockholm, Sweden, 1995. With permission.)

16.15.1.3 SIMOX Surface Micromachining

Both capacitive and piezoresistive pressure sensors were microfabricated from SIMOX wafers [Diem et al., 1993]. Figure 16.100 illustrates the process sequence by Diem et al. (1993) for fabricating an absolute capacitive pressure sensor. The 0.2-μm silicon surface layer of the SIMOX wafer is thickened with doped epi-Si to 4 μm. An access hole is RIE etched in the Si layer, and vacuum cavity and electrode gap are obtained by etching the SiO_2 buried layer. Since the buried thick oxide layer exhibits a very high reproducibility and homogeneity over the whole wafer (0.4 μm ± 5 nm), the resulting vacuum cavity and electrode gap after etching also are very well controlled. The small gap results in relatively high capacitance values between the free membrane and bulk substrate (20 pf/mm^2). Diaphragm diameter, controlled by the SiO_2 etching is up to several hundreds micrometers (±2 μm). The etching hole is hermetically sealed under vacuum by plasma CVD deposition of nonstressed dielectric layer plugs.

With the above scheme Diem et al. realized an absolute pressure sensor with a size of less than 1.5 mm^2. The temperature dependence of a capacitive sensor is mainly due to the temperature coefficient of the offset capacitance. Therefore, a temperature compensation is needed for high accuracy sensors. A drastic reduction of the temperature dependence is obtained by a differential measurement, especially if the reference capacitor resembles the sensing capacitor. A reference capacitor was designed with the mem-

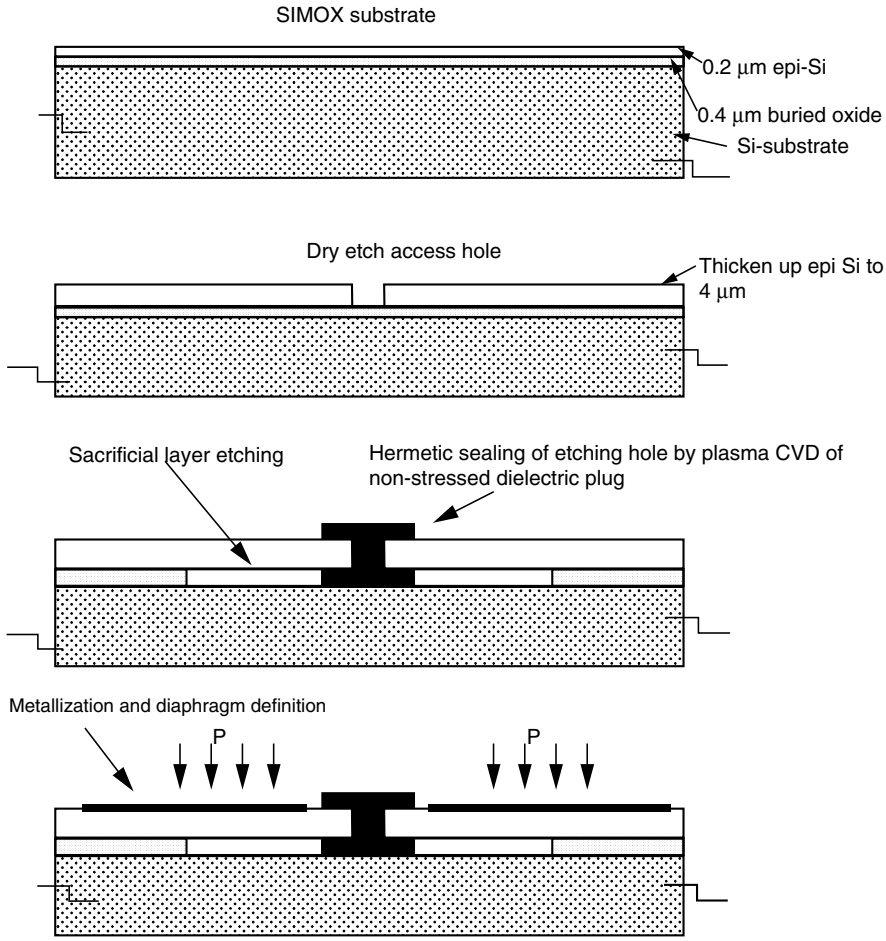


FIGURE 16.100 Process sequence of a SIMOX absolute capacitive pressure sensor by Diem et al. (From Diem, B. et al., SOI (SIMOX) as a Substrate for Surface Micromachining of Single Crystalline Silicon Sensors and Actuators, presented at Seventh Int. Conf. on Solid-State Sensors and Actuators, Yokohama, Japan, 1993. With permission.)

brane blocked by several plugs for pressure insensitivity. The localization and the number of plugs were modeled by finite element analysis (FEA) (ANSYS software was used) to get a deformation lower than 1% of the active sensor's deformation. Even without temperature calibration the high output of the differential signal resulted in an overall output error better than ±2% over the whole temperature range (−40°C to +125°C) compared to 10% for nondifferential measurements. The temperature coefficient of the sensitivity is about 100 ppm/°C which agrees with the theoretical variation of the Young modulus of silicon. A piezoresistive sensor could be achieved by implanted strain gauges in the membrane. Although SIMOX wafers are more expensive than regular wafers, they come with several process steps embedded and they make packaging easier.

16.15.1.4 Selective Epitaxy Surface Micromachining

In the discussion on epitaxy in Madou (1997, chap. 3) we drew attention to the potential of selective epitaxy for creating novel microstructures. The example in Figure 3.21 in Madou illustrates the selective deposition of epi-Si on a Si substrate through a SiO_2 window. The same figure also demonstrates the simultaneous deposition of poly-Si on SiO_2 and crystalline epi-Si on Si, creating the basis for a structure featuring an epi-Si anchor with poly-Si side arms.

Neudeck et al. (1990) and Schubert and Neudeck (1990) at Purdue and Gennissen et al. (1995) and Bartek et al. (1995) at Twente proved that selective epitaxy can also be applied for automatic etch stop on buried oxide islands. Figure 16.101 demonstrates how epitaxial lateral overgrowth (ELO) can bury oxide islands. After removal of the native oxides from the seed windows, epi is grown for 20 min at 950°C and at 60 torr using a $Si_2H_2Cl_2$-HCl-H_2 gas system. The epi growth front moves parallel to the wafer surface while growing in the lateral direction, leaving a smooth planar surface. During epi growth the HCl prevents poly nucleation on the nonsilicon areas. The epi quality is strongly dependent on the orientation of the seed holes in the oxide. Seed holes oriented in the <100> direction lead to the best epi material and surface quality. Selective epi's other big problem for fabrication remains sidewall defects [Bashir et al.]. The buried oxide islands stop the KOH etch of the substrate, enabling formation of beams and membranes as shown in Figure 16.101B. This technique might form the basis of many high performance microstructures. The Purdue and Twente groups also work on confined selective epitaxial growth (CSEG), a process pioneered by Schubert and Neudeck (1990). In this process a micromachined cavity is formed above a silicon substrate with a seed contact window to the silicon substrate and access windows for epi-Si (Figure 16.101C) [Bartek et al., 1995]. Low-stress, silicon-rich nitride layers act as structural layers to confine epitaxial growth; PSG is used as sacrificial material. This confined selective epitaxial growth technique allows electrical and/or thermal isolation separation, as well as independent optimization of active sensor and readout electronic areas.

16.15.1.5 SOI vs. Poly-Si Surface Micromachining

The power of poly-Si surface micromachining mainly lays in its CMOS compatibility. When deposited on an insulator, both poly-Si and single crystal layers enable higher operating temperatures (>200°C) than bulk micromachined sensors featuring p-n junction isolation only (130°C max) [Luder, 1986]. An additional benefit for SOI-based micromachining is IC compatibility combined with single crystal Si performance excellence. The maximum gauge factor (see Eq. (16.28)) of a poly-Si piezoresistor is about 30, roughly 15 times larger than that of a metal strain gauge but only one third of that of an indiffused resistor in single crystal Si [Obermeier and Kopystynski, 1992]. Higher piezoresistivity and fracture stress would seem to favor SOI for sensor manufacture. But there is an important counter argument: the piezoresistivity and fracture stress in poly-Si are isotropic, a major design simplification. Moreover, by laser recrystallization the gauge factor of poly-Si might increase to above 50 [Voronin et al., 1992], and by appropriate boron doping the temperature coefficient of resistance (TCR) can actually reach 0 vs. a TCR of, say, $1.7 \times 10^{-3} K^{-1}$ for single crystal p-type Si. Neither technical nor cost issues will be the deciding factor in determining which technology will become dominant in the next few years. Micromachining is very much a hostage to trends in the IC industry: promising technologies such as GaAs and micromachining do not necessarily take off in no small part because of the invested capital in some limited sets of standard silicon technologies. On this basis SOI surface micromachining is the favored candidate:

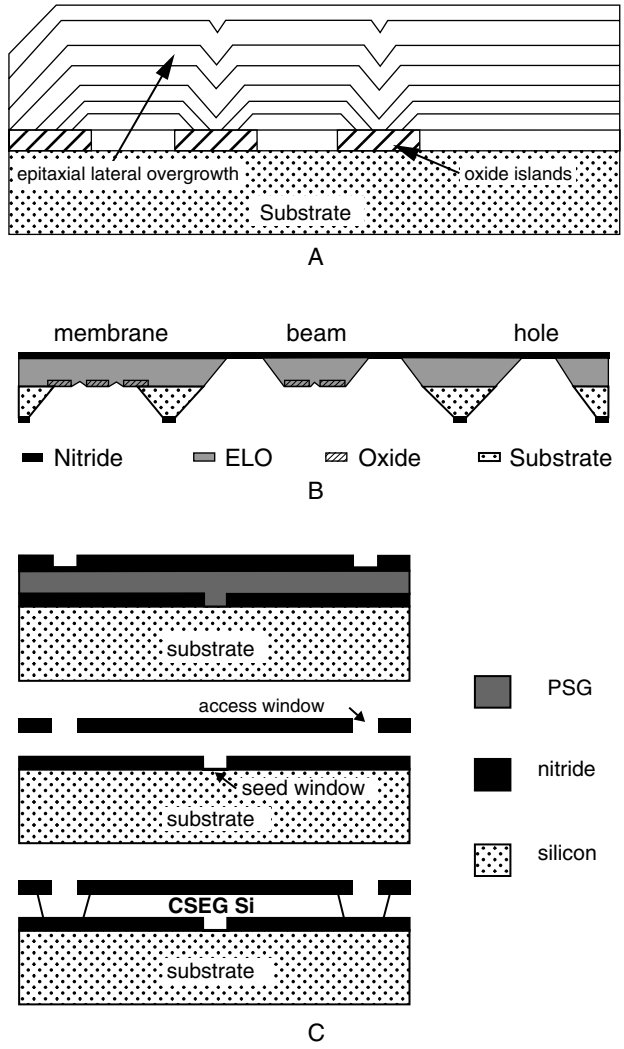


FIGURE 16.101 Micromachining with epi-Si. (A) Lateral overgrowth process of epi-Si (ELO, epitaxial lateral overgrowth) out of <100>-oriented holes in an oxide mask. (B) KOH etch stop on buried oxide islands or front side nitride. (C) Principle of confined selective epitaxial growth. (From papers presented at Transducers '95, Stockholm, Sweden, 1995. With permission.)

SOI extends silicon's technological relevance and experiences increasing investment from the IC industry, benefiting SOI micromachining [Kanda, 1991].

Based on the above we believe that SOI micromachining not only introduces an improved method of making many simple micromachines, but it also will probably become the favored approach of the IC industry. A summary of SOI advantages is listed below:

- IC industry use in all types of applications such as MOS, bipolar digital, bipolar linear, power devices, BICMOS, CCDs, heterojunction bipolar [Burggraaf, 1991] etc.
- Batch packaging through embedded cavities
- CMOS compatibility
- Substrate industrially available at lower and lower cost (about $200 today)
- Excellent mechanical properties of the single crystalline surface layer

- Freedom of shapes in the x-y dimensions and continually improving dry etching techniques, resulting in larger aspect ratios and higher features
- Freedom of choice of a very well-controlled range of thicknesses of epi surface layers
- SiO_2 buried layer as sacrificial and insulating layer and excellent etch stop
- Dramatic reduction of process steps as the SOI wafer comes with several 'embedded' process steps
- High temperature operation

16.16 Resists as Structural Elements and Molds in Surface Micromachining

16.16.1 Introduction

Polyimide and deep UV photoresists were covered already in Madou (1997, chap. 1 on lithography). We now reiterate some of the material covered there in the context of surface micromachining. Novel deep UV photoresists enable the molding of a wide variety of high aspect ratio microstructures in a wide variety of moldable materials or they are used directly as structural elements. LIGA (covered in Chapter 17), employing X-rays to pattern resists, is really just an extension of the same principles.

16.16.2 Polyimide Surface Structures

Polyimide surface structures, due to their transparency to exposing UV light, can be made very high and exhibit LIGA-like high aspect ratios. By using multiple coats of spun-on polyimide, thick suspended plates are possible. Moreover, composite polyimide plates can be made, depositing and patterning a metal film between polyimide coats. Polyimide surface microstructures are typically released from the substrate by selectively etching an aluminum sacrificial layer (see Figure 16.90), although Cu and PSG (e.g., in the butterfly wing in Figure 16.95) have been used as well (see Table 16.15).

An early result in this field was obtained at SRI International, where polyimide pillars (spacers) about 100 μm in height were used to separate a Si wafer, equipped with a field emitter array, from a display glass plate in a flat panel display [Bordie et al., 1990]. The flat panel display and an SEM picture of the pillars are shown in Figure 16.102. The Probimide 348 FC formulation of Ciba-Geigy was used. This viscous precursor formulation (48% by weight of a polyamic ester, a surfactant for wetting and a sensitizer) with a 3500-cs viscosity was applied to the Si substrate and formed into a film of a 125-μm thickness by spinning. A 30- to 40-min prebake at about 100°C removed the organic solvents from the precursor. The mask with the pillar pattern was then aligned to the wafer coated with the precursor and subjected to about 20 min of UV radiation. After driving off moisture by another baking operation the coating, still warm, was spray developed (QZ 3301 from Ciba-Geigy), revealing the desired spacer matrix. By baking the polyimide at 100°C in a high vacuum (10^{-9} Torr) the pillars shrunk to about 100 μm, while the polyimide became more dense and exhibited greater structural integrity.

More recently Frazier and Allen (1993) obtained a height-to-width aspect ratio of about 7 with polyimide structures. Ultraviolet was used to produce structures with heights in the range of 30 to 50 μm. At greater heights, the verticality of the sidewalls was relatively poor. Spun-on thickness in excess of 60 μm in a single coat was obtained for both Ciba-Geigy and Du Pont commercial UV-exposable, negative-tone polyimides. Using a G-line mask aligner, an exposure energy of 350 mJ/cm^2 was sufficient to develop a pattern with the Ciba-Geigy QZ 3301 developer. Allen and his team combined polyimide insert molds with electrodeposition to make a wide variety of metal structures [Ahn et al., 1993]. This polyimide application will be contrasted with LIGA in Chapter 17.

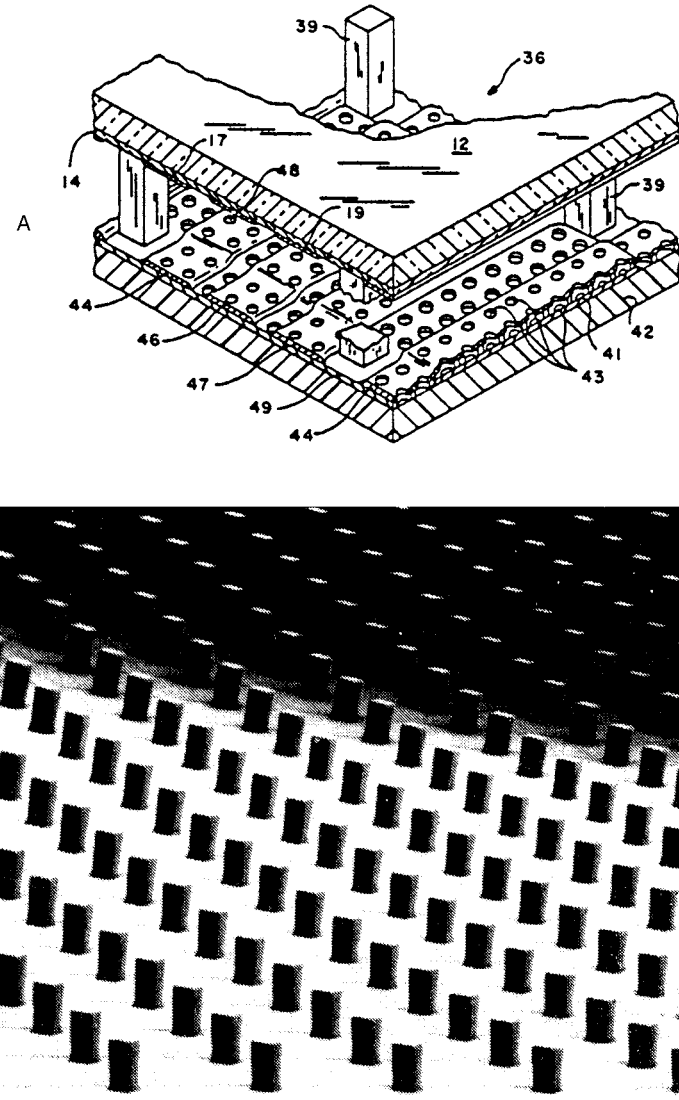


FIGURE 16.102 Polyimide structural elements. (A) Micromachined flat panel display. Number 39 represents one of the spacer pillars in the matrix of polyimide pillars (100 μm high). The spacer array separates the emitter plate from the front display plate. (B) SEM of the spacer matrix. (Courtesy of Dr. I. Brodie.) The height of the pillars is similar to what can be accomplished with LIGA. Since only a simple UV exposure was used, this polyimide is referred to as poor man's LIGA process, or pseudo-LIGA. (From Brodie, I. et al., U.S. Patent 4,923,421, 1990.)

16.16.3 UV Depth Lithography

Besides polyimides, research on novolak-type resists also is leading to higher three-dimensional features. Lochel et al. (1994; 1996a; 1996b) use novolak, positive tone resists of high viscosity (e.g., AZ 4000 series, Hoechst). They deposit in a multiple-coating process layers up to 200 μm thick in a specially designed spin coater incorporating a co-rotating cover. The subsequent UV lithography yields patterns with aspect ratios up to 10, steep edges (more than 88°) and a minimum feature size down to 3 μm. By combining this

resist technology with sacrificial layers and electroplating, a wide variety of three-dimensional microstructures resulted.

Along the same line, researchers at IBM have started experimenting with Epon SU-8 (Shell Chemical), an epoxy-based, onium-sensitized, UV transparent negative photoresist used to produce high-aspect-ratio (>10:1) features as well as straight sidewalled images in thick film (>200 μm) using standard lithography [Acosta et al., 1995; LaBianca et al., 1995]. SU-8 imaged films were used as stencils to plate permalloy for magnetic motors [Acosta et al., 1995].

Patterns generated with these thick resist technologies should now be compared with LIGA-generated patterns, not only in terms of aspect ratio, where LIGA presumably still produces better results, but also in terms of sidewall roughness and sidewall run-out. Such a comparison will determine which surface machining technique to employ for the job at hand.

16.16.4 Comparison of Bulk Micromachining with Surface Micromachining

Surface and bulk micromachining have many processes in common. Both techniques rely heavily on photolithography; oxidation; diffusion and ion implantation; LPCVD and PECVD for oxide, nitride and oxynitride; plasma etching; use of polysilicon; metallizations with sputtered, evaporated and plated Al, Au, Ti, Pt, Cr and Ni. Where the techniques differ is in the use of anisotropic etchants, anodic and fusion bonding, (100) vs. (110) starting material, p^+ etch stops, double-sided processing and electrochemical etching in bulk micromachining, and the use of dry etching in patterning and isotropic etchants in release steps for surface micromachines. Combinations of substrate and surface micromachining also frequently appear. The use of polysilicon avoids many challenging processing difficulties associated with bulk micromachining and offers new degrees of freedom for the design of integrated sensors and actuators. The technology combined with sacrificial layers also allows the nearly indispensable further advantage of *in situ* assembly of the tiny mechanical structures, because the structures are preassembled as a consequence of the fabrication sequence. Another advantage focuses on thermal and electrical isolation of polysilicon elements. Polycrystalline piezoresistors can be deposited and patterned on membranes of other materials, e.g., on a SiO_2 dielectric. This configuration is particularly useful for high-temperature applications. The p-n junctions act as the only electrical insulation in the single crystal sensors, resulting in high leakage currents at high temperatures, whereas current leakage for the poly-Si/SiO_2 structure virtually does not exist. The limits of surface micromachining are quite striking. CVD silicon usually caps at layers no thicker than 1 to 2 μm because of residual stress in the films and the slow deposition process (thick poly-Si needs further investigation). A combination of a large variety of layers may produce complicated structures, but each layer is still limited in thickness. Also, the wet chemistry needed to remove the interleaved layers may require many hours of etching (except when using the porous Si option discussed above), and even then stiction often results.

The structures made from polycrystal silicon exhibit inferior electronic and slightly inferior mechanical properties compared to single crystal silicon. For example, poly-Si has a lower piezoresistive coefficient (resulting in a gauge factor of 30 vs. 90 for single crystal Si) and it has a somewhat lower mechanical fracture strength. Poly-Si also warps due to the difference of thermal expansion coefficient between polysilicon and single crystal silicon. Its mechanical properties strongly depend on processing procedures and parameters.

Table 16.17 extends a comparison of surface micromachining with polysilicon and wet bulk micromachining. The status depicted reflects the mid-1990s and only includes poly-Si surface micromachining. As discussed, SOI micromachining, thick poly-Si, hinged poly-Si, polyimide and millimeter-molded poly-Si structures have dramatically expanded the application bandwidth of surface micromachining. In Chapter 17 on LIGA we will see how X-ray lithography can further expand the z direction for new surface micromachined devices with unprecedented aspect ratios and extremely low surface roughness. In Table 16.18 we compare physical properties of single crystal Si with those of poly-Si.

Summarizing, although polysilicon can be an excellent mechanical material, it remains a poor electronic material. Reproducible mechanical characteristics are difficult and complex to consistently realize.

TABLE 16.17 A Comparison of Bulk Micromachining with Surface Micromachining

Bulk Micromachining	Surface Micromachining
Large features with substantial mass and thickness	Small features with low thickness and mass
Utilizes both sides of the wafer	Multiple deposition and etching required to build up structures
Vertical dimensions: one or more wafer thicknesses	Vertical dimensions are limited to the thickness of the deposited layers (~2 μm), leading to compliant suspended structures with the tendency to stick to the support
Generally involves laminating Si wafer to Si or glass	Surface micromachined device has its built-in support and is more cost effective
Piezoresistive or capacitive sensing	Capacitive and resonant sensing mechanisms
Wafers may be fragile near the end of the production	Cleanliness critical near end of process
Sawing, packaging, testing are difficult	Sawing, packaging, testing are difficult
Some mature products and producers	No mature products or producers
Not very compatible with IC technology	Natural but complicated integration with circuitry; integration is often required due to the tiny capacitive signals

Source: Adapted from Jerman, H., *Bulk Silicon Micromachining,* Banf, Canada, 1994.

TABLE 16.18 Comparison of Material Properties of Si Single Crystal with Crystalline Polysilicon

Material Property	Single Crystal Si	Poly-Si
Thermal conductivity (W/cm°K)	1.57	0.34
Thermal expansion (10^{-6}/°K)	2.33	2–2.8
Specific heat (cal/g°K)	0.169	0.169
Piezoresistive coefficients	n-Si ($\pi_{11} = -102.2$); p-Si ($\pi_{44} = +138.1$); e.g., gauge factor of 90	Gauge factor of 30 (>50 with laser recrystallization)
Density (cm^3)	2.32	2.32
Fracture strength (GPa)	6	0.8 to 2.84 (undoped poly-Si)
Dielectric constant	11.9	Sharp maxima of 4.2 and 3.4 eV at 295 and 365 nm, respectively
Residual stress	None	Varies
Temperature resistivity coefficient (TCR) ($°K^{-1}$)	0.0017 (p-type)	0.0012 nonlinear, + or – through selective doping, increases with decreasing doping level, can be made 0!
Poisson ratio	0.262 max for (111)	0.23
Young's modulus ($10^{11} N/m^2$)	1.90 (111)	1.61
Resistivity at room temperature (ohm.cm)	Depends on doping	7.5 10^{-4} (always higher than for single crystal silicone)

Source: Based on Lin (1993), Adams (1988), and Heuberger (1989). (See also Madou [1997, chap. 8, Table 8.5].)

Fortunately, SOI surface micromachining and other newly emerging surface micromachining techniques can alleviate many of the problems [Petersen et al., 1991].

16.17 Materials Case Studies

16.17.1 Introduction

Thin-film properties prove not only difficult to measure but also to reproduce, given the many influencing parameters. Dielectric and polysilicon films can be deposited by evaporation, sputtering and molecular

TABLE 16.19 Comparison of Different Deposition Techniques

	Atmospheric Pressure CVD (APCVD)	Low Temperature LPCVD	Medium Temperature LPCVD	Plasma-Enhanced CVD (PECVD)
Temp (°C)	300–500	300–500	500–900	100–350
Materials	SiO_2, P-glass	SiO_2, P-glass, BP-glass	Poly-Si, SiO_2, P-glass, BP-glass, Si_3N_4, SiON	SiN, SiO_2, SiO_2, SiON
Uses	Passivation, insulation, spacer	Passivation, insulation spacer	Passivation, gate metal, structural element, spacer	Passivation, insulation, structural elements
Throughput	High	High	High	Low
Step coverage	Poor	Poor	Conformal	Poor
Particles	Many	Few	Few	Many
Film properties	Good	Good	Excellent	Poor

Note: P-glass = phosphorus-doped glass; BP-glass = borophosphosilicate glass.

Source: Adapted from Adams, A.C., in *VLSI Technology,* Sze, S.M., Ed., McGraw-Hill, New York, 1988, pp. 233–271.

TABLE 16.20 Approximate Mechanical Properties of Microelectronic Materials

	E(GPa)	ν	α(1/°C)	σ_0
Substrates				
Silicon	190	0.23	2.6×10^{-6}	—
Alumina	~415	—	8.7×10^{-6}	—
Silica	73	0.17	0.4×10^{-6}	—
Films				
Polysilicon	160	0.23	2.8×10^{-6}	Varies
Thermal SiO_2	70	0.20	0.35×10^{-6}	Compressive, e.g., 350 MPa
PECVD SiO_2	—	—	2.3×10^{-6}	—
LPCVD Si_3N_4	270	0.27	1.6×10^{-6}	Tensile
Aluminum	70	0.35	25×10^{-6} (high!)	Varies
Tungsten (W)	410 (stiff!)	0.28	4.3×10^{-6}	Varies
Polyimide	3.2	0.42	$20–70 \times 10^{-6}$ (very high)	Tensile

Note: E = Young's modulus, ν = Poisson ratio, α = coefficient of thermal expansion, σ_0 = residual stress.

Source: Based on lecture notes from S.D. Senturia and R.T. Howe.

beam techniques. In VLSI and surface micromachining, none of these techniques are as widely used as CVD techniques. The major problems associated with the former methods are defects caused by excessive wafer handling, low throughput, poor step coverage, and nonuniform depositions. From the comparison of CVD techniques in Table 16.19 we can conclude that LPCVD, at medium temperatures, prevails above all others. VLSI devices and integrated surface micromachines require low processing temperatures to prevent movement of shallow junctions uniform step coverage, few process-induced defects (mainly from particles generated during wafer handling and loading) and high wafer throughput to reduce cost. These requirements are best met by hot-wall, low-pressure depositions [Iscoff, 1991] (see also Madou [1997, chap. 3]). While depositing a material with LPCVD the following process parameters can be varied: deposition temperature, gas pressure, flow rate and deposition time.

Table 16.20 cites some approximate mechanical properties of microelectronic materials. The numbers for thin film materials must be approached as approximations; the various parameters affecting mechanical properties of thin films will become clear in the case studies below.

16.17.2 Polysilicon Deposition and Material Structure

16.17.2.1 Introduction

The IC industry applies polysilicon in applications ranging from simple resistors, gates for MOS transistors, thin-film transistors (TFT) (with amorphous hydrogenated silicon: α-Si:H), DRAM cell plates

and trench fills, as well as in emitters in bipolar transistors and conductors for interconnects. For the last application, highly doped polysilicon is especially suited; it is easy to establish ohmic contact, it is light insensitive, corrosion resistant, and its rough surface promotes adhesion of subsequent layers. Doping elements such as arsenic, phosphorous or boron reduce the resistivity of the polysilicon. Polysilicon also has emerged as the central structural/mechanical material in surface micromachining, and a closer look at the influence of deposition methodology on its materials characteristics is warranted.

16.17.2.2 Undoped Poly-Si

The properties of low-pressure chemical vapor deposited (LPCVD) undoped polysilicon films are determined by the nucleation and growth of the silicon grains. LPCVD Si films, grown slightly below the crystallization temperature (about 600°C for LPCVD), initially form an amorphous solid that subsequently may crystallize during the deposition process [Krulevitch, 1994; Lietoila et al., 1982]. The CVD method results in amorphous films when the deposition temperatures are well below the melting temperature of Si (1410°C). The subsequent transition from amorphous to crystalline depends on atomic surface mobility and deposition rate. At low temperatures, surface mobility is low, and nucleation and growth are limited. Newly deposited atoms become trapped in random positions and, once buried, require a substantial amount of time to crystallize as solid state diffusion is significantly lower than surface mobility. That is why, for low temperature deposition, amorphous layers only start to crystallize after sufficient time at temperature in the reactor. Working at temperatures between 580 and 591.5°C, Guckel et al. (1990) produced mostly amorphous films. But Krulevitch, working at only slightly higher temperatures (605°C) and probably leaving the films longer in the LPCVD set-up, produced crystallized films. Upon crossing the transition temperature between amorphous and crystalline growth (see Madou [1997, chap. 3, Figure 3.18]), crystalline growth immediately initiates at the substrate due to the increased surface mobility which allows adatoms to find low energy, crystalline positions from the start of the deposition process. The deposition temperature at which the transition from amorphous to a crystalline structure occurs depends on many parameters, such as deposition rate, partial pressure of hydrogen, total pressure, presence of dopants and presence of impurities (O, N or C) [Adams, 1988]. In the crystalline regime, numerous nucleation sites form, resulting in a transition zone of a multitude of small grains at the film/substrate interface to columnar crystallites on top, as shown in the schematic of a 620 to 650°C columnar film in Figure 16.103. In this figure, a transition zone of small, randomly oriented grains is sketched near the SiO_2 layer. The rate of crystallization is faster here than the deposition rate. Columnar grains ranging between 0.03 and 0.3 μm in diameter form on top of the small grains [Adams, 1988]. The columnar coarse grain structure arises from a process of growth competition among the small grains,

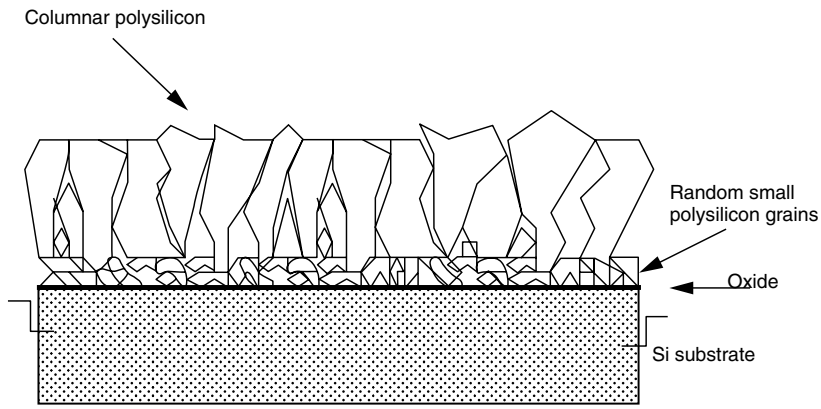


FIGURE 16.103 Schematic of compressive poly-Si formed at 620 to 650°C. The columnar coarse-grain structure arises from a process of grain growth competition among the small grains, during which those grains preferentially oriented for fast vertical growth survive at the expense of misoriented, slowly growing grain. (After Krulevitch, P.A., Micromechanical Investigations of Silicon and Ni-Ti-Cu Thin Films, Ph.D. thesis, University of California, Berkeley, 1994.)

during which those grains preferentially oriented for fast vertical growth survive at the expense of misoriented, slowly growing grains [van der Drift, 1967; Matson and Polysakov, 1977]. The lower the deposition temperature, the smaller the initial grain size will be. At 700°C, films also are columnar; however, the grains are cylindrical extending through the thickness of the entire film and there is no transition zone near the SiO_2 interface [Krulevitch, 1994].

Stress in poly-Si films was found to vary significantly with deposition temperature and silane pressure. Guckel et al. (1990) found that their mainly amorphous films, deposited at temperatures below 600°C, proved highly compressive with strain levels as high as –0.67%. At temperatures barely above 600°C, Krulevitch reports tensile films, whereas for yet higher temperatures (≥620°C) the stress again turns compressive. While films deposited at temperatures greater than 630°C all turned out compressive, the magnitude of the compression decreased with increasing temperature. The stress gradient in the poly-Si films explains why compressive undoped and unannealed poly-Si beams tend to curl upward (positive stress gradient) when released from the substrate [Lober et al., 1988].

Using high resolution transmission electron microscopy, Guckel et al. (1990) and Krulevitch (1980) found a strong correlation between the material's microstructure and the exhibited stress. Guckel et al. found that in their mainly amorphous films, deposited at temperatures below 600°C, a region near the substrate interface crystallized during growth with grains between 100 and 4000 Å. Krulevitch found that tensile, low-temperature films (605°C) have Si grains dispersed throughout the film thickness. Krulevitch suggests that the compressive stress in the higher temperature compressive films (≥620°C) relates to the competitive growth mechanism of the columnar grains. The same author concluded that thermal sources of stress are insignificant.

Importantly, Guckel et al. discovered that annealing in nitrogen or under vacuum converts the low-temperature films with compressive built-in strain (–0.007) to a tensile strain with controllable strain levels between 0 and + 0.003 (see Figure 16.104). During anneal no grain size increase was noticed (100 to 4000 Å) but a slight increase in surface roughness was measured. This type of poly-Si is referred to as fine-grain

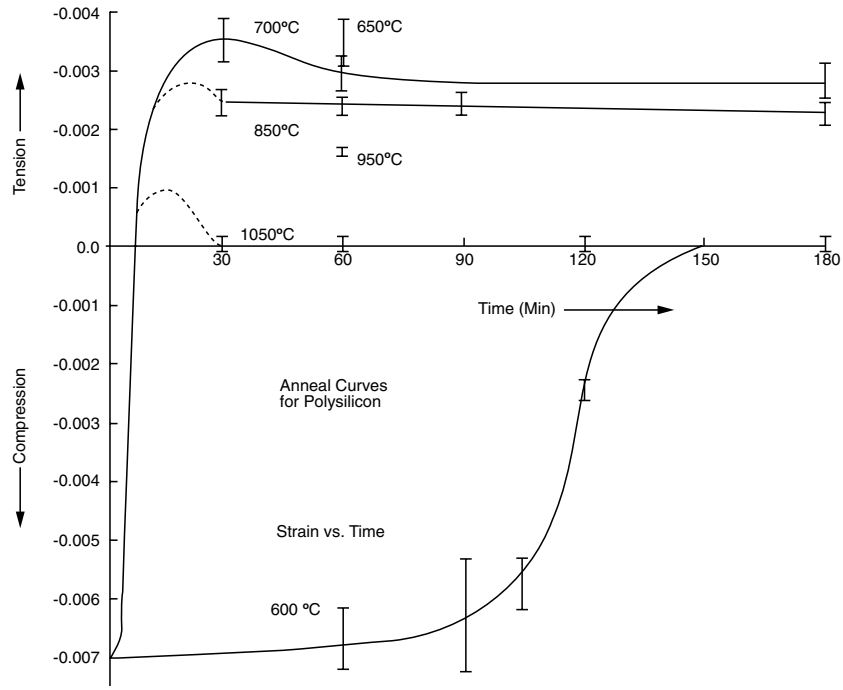


FIGURE 16.104 Anneal curves for poly-Si. Strain versus anneal time. Upper curves: low-temperature film. Lower curve: high-temperature film. (From Guckel, H. et al., *IEEE Trans. Electron. Dev.*, 35, 800–801, 1988. With permission.)

poly-Si (also Wisconsin poly-Si). Guckel et al. explain this strain field reversal as follows: as the amorphous region of the film crystallizes, it attempts to contract, but due to the substrate constrained newly crystallized region, a tensile stress results. Higher temperature films, during an anneal, also become less strained, but the strain remains compressive (see lower curve in Figure 16.104). Moreover, in this case grain size does increase and the surface turns considerably rougher. The latter is called coarse-grain poly-Si. Fine-grain poly-Si with its tensile strain is preferable; however, it cannot be doped to as low a resistivity as coarse-grain polysilicon. Hence, fine-grain polysilicon should be considered as a structural material rather than an electronic material.

Summarizing stress in poly-Si depends on the material's microstructure, with tension arising from the amorphous to crystalline transformation during deposition and compression from the competitive grain growth mechanism.

Polysilicon deposited at 600 to 650°C has a {110}-preferred orientation. At higher temperatures, the {100} orientation dominates. Dopants, impurities and temperature influence this preferred orientation [Adams, 1988]. Drosd and Washburn (1982) introduced a model explaining the experimental observation that regrowth of amorphitized Si is faster for {100} surfaces, followed by {110} and {111} which are 2.3 and 20 times slower, respectively. Interestingly, the latter also pinpoints the order of fastest to slowest etching of the crystallographic planes in alkaline etchants. As discussed earlier in this chapter, Elwenspoek et al. (1994) used this observation of symmetry between etching and growing of Si planes as an important insight to develop a new theory explaining anisotropy in etching. In Table 16.21 we compare the discussed coarse- and fine-grain poly-Si forms.

The above picture might further be complicated by the controlling nature of the substrate. For example, depositing amorphous Si ($\alpha - Si$) at even lower temperatures of 480°C from disilane (Si_2H_6) and crystallizing it by subsequent annealing at 600°C demonstrated a large dependency of crystallite size on the underlying SiO_2 surface condition. Treating the surface with $HF:H_2O$ or $NH_4OH:H_2O_2:H_2O$ leads to poly-Si films with a large grain size, two or three times as large as without SiO_2 treatment, believed to be the consequence of nucleation rate suppression [Shimizu and Ishihara, 1995].

T. Abe and M.L. Reed made low strain polysilicon thin film by DC-magnetics sputtering and post-annealing. The films showed very small regional stress and very smooth texture. The deposition rate was 193 Å/min and the substrate was neither cooled nor heated. The average roughness was found to be comparable to the surface roughness of polished, bare silicon substrates [Abe and Reed, 1996].

16.17.2.3 Doped Poly-Si

To produce micromachines, doped poly-Si is used far more frequently than undoped poly-Si. Dopants decrease the resistivity to produce conductors and control stress. Polysilicon can be doped by diffusion, implantation or the addition of dopant gases during deposition (*in situ* doping). We only detail material properties of *in situ* doped poly-Si here.

TABLE 16.21 Comparison of Coarse-Grain and Fine-Grain Poly-Si

	Coarse-Grain Poly-Si	Fine-Grain Poly-Si
Temperature of deposition (°C)	620–650	570–591.5
Surface roughness	Rough, >50Å	Smooth, <15Å
Grain size	Undoped: 160–320 Å as deposited; *in situ* P-doped: 240–400 Å	Very small grains
As deposited strain	–0.007 (compressive)	–0.007 (compressive)
Effect of high-temperature anneal	Grains size increases, residual strain decreases but remains compressive, reduced bending moment	Grain size increases to 100 Å [Guckel et al., 1988]; others have found 700–900 Å; large variation in strain (see Figure 16.102) from compressive to tensile
Dry and wet etch rate	Higher for doped material; depends on dopant concentration	Higher for doped material; depends on dopant concentration
Texture	<110> as deposited, <311> *in situ* P-doped	No texture as deposited; depends on dopant concentration, <111> after 900–1000°C anneal [Harbeke et al., 1983]

Doping poly-Si films *in situ* reduces the number of processing steps required for producing doped micro-devices and also provides the potential for uniform doping through the film thickness. *In situ* doping of poly-Si with phosphorous is accomplished by maintaining a constant PH_3 to SiH_4 gas flow ratio of about 1 vol % in a hot-wall LPCVD set-up. At this ratio the phosphorus content in the film appears above the saturation limit and the excess dopant segregates at the grain boundaries [Adams, 1988]. *In situ* phosphorus-doped poly-Si undergoes the same amorphous to crystalline growth transformation observed in the undoped film, with the material's microstructure depending on deposition temperature as well as deposition pressure. The temperature of transformation is lower for the doped films than for the undoped poly-Si and occurs between 580 and 620°C [Mulder et al., 1990; Kinsbron et al., 1983]. Phosphorus doping thus enhances crystallization in amorphous silicon [Lietoila et al., 1982] and, due to passivation of the poly-Si surface by the phosphine gas, reduces the poly-Si deposition rate [Mulder et al., 1990]. Decreases in deposition rate by as much as a factor of 25 have been reported [Meyerson and Olbricht, 1984]. Slower deposition rates allow more time for adatoms to find crystalline sites, resulting in crystalline growth at lower temperatures. From Table 16.21 we read that the grain size of phosphorus-doped poly-Si tends to be larger (240 to 400 Å) than for the undoped material and that {311} planes show up as a texture facet in the doped material.

At lower deposition temperatures and higher pressures, the microstructure again consists of amorphous and crystalline regions, while at higher temperatures and lower pressures columnar films result and as deposited films exhibit compressive residual stress. The columnar films have a stress gradient that increases towards the film surface, as opposed to the gradient found in undoped columnar poly-Si. This gradient in stress most likely is due to nonuniform distribution of phosphorus throughout the film. Annealing at 950°C for 1 hour results in the same stress and stress gradient for initially columnar and initially amorphous/crystalline films (i.e., $\sigma_f = -45$ MPa and $\Gamma = +0.2$ mm^{-1}, respectively) [Krulevitch, 1994].

As with undoped poly-Si, phosphorus-doped poly-Si films with smooth surfaces (fine-grain) can be obtained by depositing *in situ* doped films in the amorphous state and then annealing [Harbeke et al., 1983; Hendriks and Mavero, 1991]. Phosphorus-doped poly-Si oxidizes faster than undoped poly-Si. The rate of oxidation is determined by the dopant concentration at the poly-Si surface [Adams, 1988].

Two drawbacks of *in situ* phosphorus doping are slower deposition rates [Kurokawa, 1982] and reduced film thickness uniformity [Meyerson and Olbricht, 1984], although uniformity can be improved by modifying the reactor geometry [Mulder et al., 1990]. As discussed before, the lower deposition rate of *in situ* phosphine doping can be mitigated by reducing the flow of phosphine/silane ratio by one third [Howe, 1995]. In contrast to *in situ* phosphine and arsine doping, which both decrease the deposition rate, diborane doping of poly-Si to make it p^+ accelerates the deposition rate [Adams, 1988].

The addition of oxygen to poly-Si increases the film's resistivity and the resulting coating, semi-insulating poly-Si (SIPOS) acts as a passivating coating for high voltage devices in the IC industry. The latter material does not seem to have emerged in surface micromachining yet.

The values for the fracture stress of boron-, arsenic- and phosphorus-doped polysilicon are 2.77 ± 0.08 Gpa, 2.70 ± 0.09 Gpa, and 2.11 ± 0.1 Gpa, respectively, compared with 2.84 ± 0.09 Gpa for undoped polysilicon. The lower value for phosphorus-doped material has been attributed to high surface roughness and with the large number of defects associated with extensive grain growth in highly phosphorus-doped films [Biebl and von Philipsborn, 1993].

The quest for low temperature poly-Si deposition makes the 320°C PECVD deposition method especially interesting. PECVD films, deposited in a 50-kHz parallel-plate diode reactor, can be doped *in situ* and crystallized by rapid thermal annealing (RTA: 1100°C, 100 seconds). It was shown that small-grained PECVD films annealed by RTA have good electrical properties and gauge factors between 20 and 30, i.e., similar to those reported for other alternative types of polycrystalline silicon [Compton, 1992].

16.17.3 Amorphous and Hydrogenated Amorphous Silicon

Amorphous silicon behaves quite different from either fine- or coarse-grain poly-Si. The amorphous material produces a high breakdown strength (7 to 9 MV/cm) oxide with low leakage currents (vs. a low

breakdown voltage and large leakage currents for polycrystalline Si oxides). Amorphous polysilicon also attains a broad maximum in its dielectric function without the characteristic sharp structures near 295 and 365 nm (4.2 and 3.4 eV) of crystalline poly-Si. Approximate refractive index values at a wavelength of 600 nm are 4.1 for crystalline polysilicon and 4.5 for amorphous material [Adams, 1988]. As deposited, the material is under compression, but an anneal at temperatures as low as 400°C reduces the stress significantly, even leading to tensile behavior [Chang et al., 1991].

Hydrogenated amorphous silicon (α-Si:H) enables the fabrication of active semiconductor devices on foreign substrates at temperatures between 200 and 300°C. The technology, first applied primarily to the manufacturing of photovoltaic panels, now is quickly expanding into the field of large-area microelectronics such as active matrix liquid crystal displays (AMLCD). It is somehow surprising that micromachinists have not taken more advantage of this material either for powering surface micromachines or to implement electronics cheaply on non-Si substrates.

Spear and LeComber (1975) showed that, in contrast to α-Si, α-Si:H could be doped both n- and p-type. Singly bonded hydrogen, incorporated at the Si dangling bonds, reduces the electronic defect density from $\sim 10^{19}/cm^3$ to $\sim 10^{16}/cm^3$ (typical H concentrations are 5 to 10 atomic percent—several orders of magnitude higher than needed to passivate all the Si dangling bonds). The lower defect density results in a Fermi level that is free to move, unlike in ordinary amorphous Si, where it is pinned. Other interesting electronic properties are associated with α-Si:H—exposure of α-Si:H to light increases photoconductivity by four to six orders of magnitude, and its relatively high electron mobility ($\sim 1\ cm^2/V\ sec^{-1}$) enables fabrication of useful thin-film transistors. Only recently did Lee et al. (1995) note that hydrogenated amorphous silicon solar cells are an attractive means to realize an on-board power supply for integrated micromechanical systems. They point out that the absorption coefficient of α-Si:H is more than an order of magnitude larger than that of single crystal Si near the maximum solar photon energy region of 500 nm. Accordingly, the optimum thickness of the active layer in an α-Si:H solar cell can measure 1 μm, much smaller than that of single crystal Si solar cells. By interconnecting 100 individual solar cells in series, the measured open circuit potential reaches as high as 150 V under AM 1.5 conditions, a voltage high enough to drive on-board electrostatic actuators.

Hydrogenated amorphous silicon is manufactured by plasma-enhanced chemical vapor deposition from silane. Usually, planar RF-driven diode sources using SiH_4 or SiH_4/H_2 mixtures are used. Typical pressures of 75 mTorr and temperatures between 200 and 300°C allow silane decomposition with Si deposition as the dominant reaction. Decomposition occurs by electron impact ionization, producing many different neutral and ionic species [Crowley, 1992]. Deposition rates for usable device quality α-Si:H generally do not exceed ~2 to 5 Å/sec, due to the effects of temperature, pressure and discharge power. Table 16.22 gives state-of-the-art parameters for α-Si:H prepared by PECVD. Although its semiconducting properties are inferior to single crystal Si, the material is finding more and more applications. Some examples are TFT switches for picture elements in AMLCDs [Holbrook and McKibben, 1992], page-wide TFT-addressed document scanners, high-voltage TFTs capable of switching up to 500 V etc. [Bohm, 1988]. An excellent source for further information on amorphous silicon is the book *Plasma Deposition of Amorphous Silicon-Based Materials* [Bruno et al., 1995].

16.17.4 Silicon Nitride

Silicon nitride is a commonly used material in microcircuit and microsensor fabrication due to its many superior chemical, electrical, optical and mechanical properties. The material provides an extremely good barrier to the diffusion of water and to ions, particularly of Na^+. It also oxidizes slowly (about 30 times less than silicon) and has highly selective etch rates over SiO_2 and Si in many etchants. Some applications of silicon nitride are optical waveguides (nitride/oxide), encapsulant (diffusion barrier to water and ions), insulator (high dielectric strength), mechanical protection layer, etch mask, oxidation barrier and ion implant mask (density is 1.4 times that of SiO_2). Silicon nitride is also hard and can be used as, for example, a bearing material in micromotors [Pool, 1988].

TABLE 16.22 Typical Opto-Electronic Parameters Obtained for PECVD α-Si:H

	Symbol	Parameter
Undoped		
Hydrogen content		~10%
Dark conductivity at 300 K	σ_D	$\sim 10^{-10}$ $(\Omega\text{-cm})^{-1}$
Activation energy	E_σ	0.8–0.9 eV
Pre-exponent conductivity factor	σ_0	$>10^3$ $(\Omega\text{-cm})^{-1}$
Optical bank gap at 300 K	E_g	1.7–1.8 eV
Temperature variation of band gap	$E_g(T)$	$2\text{–}4 \times 10^{-4}$ eV/K
Density of states at the minimum	g_{min}	$>10^{15}$–10^{17} cm^3/eV
Density of states at the conduction band edge		$\sim 10^{15}/cm^3$
ESR spin density	N_s	$\sim 10^{21}/cm^3$–eV
Infrared spectra		2000/640 cm^{-1}
Photoluminescence peak at 77K		~1.25 eV
Extended state mobility		
Electrons	μ_n or μ_e	>10 cm^2/V–s
Holes	μ_p or μ_h	~1 cm^2/V–s
Drift mobility		
Electrons	μ_n or μ_e	~1 cm^2/V–s
Holes	μ_p or μ_h	$\sim 10^{-2}$ cm^2/V–s
Conduction band tail slope		25 meV
Valence band tail slope		40 meV
Hole diffusion length		~1 μm
Doped amorphous		
n-Type[a]	σ_D	10^{-2} $(\Omega\text{–cm})^{-1}$
	E_g	~0.2 eV
p-Type[b]	σ_D	10^{-3} $(\Omega\text{–cm})^{-1}$
	E_g	~0.3 eV
Doped microcrystalline		
n-Type[c]	σ_D	≥1 $(\Omega\text{–cm})^{-1}$
	E_g	≤0.05 eV
p-Type[d]	σ_D	≥1 $(\Omega\text{–cm})^{-1}$
	E_g	≤0.05 eV

[a] –1% pH_3 added to gas phase.

[b] –1% B_2H_6 added to gas phase.

[c] –1% PH_3 added to dilute SiH_4/H_2, or 500 vppm PH_3 added to SiF_4/H_2 (8:1) gas mixtures. Relatively high powers are involved.

[d] –1% B_2H_6 added to dilute SiH_4/H_2.

Source: Crowley, J.L., *Solid State Technol.,* February, 94–98, 1992. With permission.

Silicon nitride can be deposited by a wide variety of CVD techniques: APCVD, LPCVD and PECVD. Nitride often is deposited from SiH_4 or other Si containing gases and NH_3 in a reaction such as:

$$3SiCl_2H_2 + 4NH_3 \rightarrow Si_3N_4 + 6HCl + 6H_2 \qquad \text{(Reaction 16.17)}$$

In this CVD process, the stoichiometry of the resulting nitride can be moved toward a silicon-rich composition by providing excess silane or dichlorosilane compared to ammonia.

16.17.4.1 PECVD Nitride

Plasma-deposited silicon nitride, also plasma nitride or SiN, is used as the encapsulating material for the final passivation of devices. The plasma-deposited nitride provides excellent scratch protection, serves as a moisture barrier and prevents sodium diffusion. Because of the low deposition temperature, 300 to 350°C, the nitride can be deposited over the final device metallization. Plasma-deposited nitride

TABLE 16.23 Properties of Silicon Nitride[a]

Deposition	LPCVD	PECVD
Temperature (°C)	700–800	250–350
Density (g/cm^3)	2.9–3.2	2.4–2.8
Pinholes	No	Yes
Throughput	High	Low
Step coverage	Conformable	Poor
Particles	Few	Many
Film quality	Excellent	Poor
Dielectric constant	6–7	6–9
Resistivity (Ωcm)	10^{16}	10^6–10^{15}
Refractive index	2.01	1.8–2.5
Atom % H	4–8	20–25
Energy gap	5	4–5
Dielectric strength (10^6 V/cm)	10	5
Etch rate in conc. HF	200 Å/min	
Etch rate in BHF	5–10 Å/min	
Residual stress (10^9 dyn/cm^2)	1T	2 C–5T
Poisson ratio	0.27	
Young's modulus	270 GPa	
TCE	1.6×10^{-6}/°C	

Note: C = compressive; T = tensile.
[a] See Adams (1988), Sinha and Smith (1978) and Retajczyk and Sinha (1980).

and oxide both act as insulators between metallization levels, particularly useful when the bottom metal level is on aluminum or gold. The silicon nitride that results from PECVD in the gas mixture of Reaction 16.2 has two shortcomings: high hydrogen content (in the range of 20 to 30 atomic percent) and high stress. The high compressive stress (up to 5×10^9 dyn/cm^2) can cause wafer warping and voiding and cracking of underlying aluminum lines [Rosler, 1991]. The hydrogen in the nitride also leads to degraded MOSFET lifetimes. To avoid hydrogen incorporation, one may employ low or no hydrogen-containing source gases such as nitrogen instead of ammonia as the nitrogen source. Also, a reduced flow of SiH_4 results in less Si-H in the film. The hydrogen content and the amount of stress in the film are closely linked. Compressive stress, for example, changes toward tensile stress upon annealing to 490°C in proportion to the Si-H bond concentration. By adding N_2O to the nitride deposition chemistry an oxynitride forms with lower stress characteristics; however, oxynitrides are somewhat less effective as moisture and ion barriers than nitrides.

We discussed the effect of RF frequency on nitride stress, hydrogen content, density and the wet etch rate in detail in Madou (1997, chap. 3). We can conclude that low frequency (high energy bombardment) results in films with low compressive stress, lower etch rates and higher density. The higher the ion bombardment during PECVD, the higher the stress is. Stress also is affected by moisture exposure and temperature cycling (for a good review, see Wu and Rosler [1992]). We compare properties of silicon nitride formed by LPCVD and PECVD in Tables 16.23 and 16.24. Table 16.24 highlights typical process parameters.

16.17.4.2 LPCVD Nitride

In the IC industry, stoichiometric silicon nitride (Si_3N_4) is LPCVD deposited at 700 to 900°C and functions as an oxidation mask and as a gate dielectric in combination with thermally grown SiO_2. In micromachining, LPCVD nitride serves as an important mechanical membrane material and isolation/buffer layer. By increasing the Si content in silicon nitride the ensile film stress reduces (even to compressive), the film turns more transparent and the HF etch rate lowers. Such films result by increasing the dichlorosilane/ammonia ratio [Sakimoto et al., 1982].

Figure 16.105 illustrates the effect of gas flow ratio and deposition temperature on stress and the corresponding refractive index and HF etch rate [Sakimoto et al., 1982].

TABLE 16.24 Silicon Nitride PECVD Process Conditions

Flow (sccm)	SiH_4	190–270
	NH_3	1900
	N_2	1000
Temperature (°C)	T.C.	350 or 400
	Wafer	~330 or 380
Pressure (torr)		2.9
rf power (watt)	1100	
Deposition rate (Å/min)		1200–1700
Refractive index		2.0

Source: Wu, T.H.T. and R.S. Rosler, *Solid State Technol.*, May, 65–71, 1992. With permission.

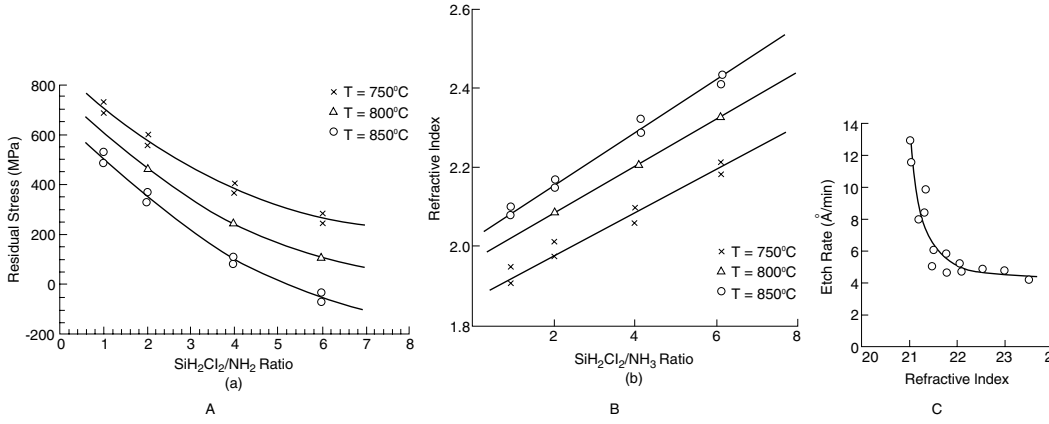


FIGURE 16.105 Silicon nitride LPCVD deposition parameters. (A) Effect of gas-flow ratio and deposition temperature on stress in nitride films. (B) The corresponding index of refraction. (C) The corresponding HF etch rate. (From Sakimoto, M. et al., *J. Vac. Sci. Technol.*, 21, 1017–1021, 1982. With permission.)

TABLE 16.25 Etching Behavior of LPCVD Si_3N_4

Etchant	Temperature (°C)	Etch Rate (Å/min)	Selectivity of Si_3N_4:SiO_2:Si
H_3PO_4	180	100	10:1:0.3
CF_4–4% O_2 plasma	—	250	3:2.5:17
BHF	25	5 to 10	1:200:±0
HF (40%)	25	200	1:>100:0.1

Silicon-rich or low-stress nitride emerges as an important micromechanical material. Low residual stress means that relatively thick films can be deposited and patterned without fracture. Low etch rate in HF means that films of silicon-rich nitride survive release etches better than stoichiometric silicon nitride. The etch characteristics of LPCVD SiN are summarized in Table 16.25. The properties of a LPCVD Si_xN_y film, deposited by reaction of $SiCl_2H_2$ and NH_3 (5:1 by volume) at 850°C, were already summarized in Table 16.23.

16.17.5 CVD Silicon Dioxides

Silicon oxides, like other dielectrics, function as insulation between conducting layers, for diffusion and ion implementation masks, for diffusion from doped oxides, for capping doped oxides to prevent the

loss of dopants, for gettering impurities and for passivation to protect devices from impurities, moisture and scratches. In micromachining, silicon oxides serve the same purposes but also act as sacrificial material. Phosphorus-doped glass (PSG), also called P-glass or phosphosilicate glass, and borophosphosilicate glasses (BPSG) soften and flow at lower temperatures enabling the smoothing of topography. They etch much faster than SiO_2, which benefits their application as sacrificial material. The deposition of thermal SiO_2 is covered in Madou (1997, chap. 3). Now we consider CVD techniques to deposit doped and undoped SiO_2.

16.17.5.1 CVD Undoped SiO_2

Several CVD methods will deposit SiO_2. CVD silicon dioxide can be deposited on the wafer out of the vapor phase from the reaction of silane (SiH_4) with oxygen at relative low temperatures (300 to 500°C) and low pressure. The silane/oxygen gas mixture has been applied at atmospheric pressure (AP) and plasma-enhanced conditions. The main advantage of silane/oxygen is the low deposition temperature; the main disadvantage is the poor step coverage.

In general, tetraethylorthosilicate (TEOS) brings about a better starting chemistry than the traditional silane-based CVD technologies. TEOS-based depositions lead to superior film quality in terms of step coverage and reflow properties. With an LPCVD reactor, the deposition temperature for TEOS is as high as 650 to 750°C, precluding its use over aluminum lines. In contrast, silicon dioxide is deposited by PECVD at 300 to 400°C from TEOS. CVD oxides in general feature porosity and low density. Low frequency (high energy) ion bombardment results in more compressive films, higher density and lower etch rates as well as better moisture resistance [Rosler, 1991]. Use of TEOS oxide, to replace SiH_4-based oxide in spin-on-glass (SOG) and photoresist planarization schemes, now has become commonplace for devices with small features.

Yet another promising silicon dioxide deposition technology is the subatmospheric pressure CVD (SACVD). Both undoped and borophosphosilicate glass have been deposited in this fashion. The process involves an ozone and TEOS reaction at a pressure of 600 Torr and at a temperature below 400°C. While offering the same good step coverage over submicron gaps, the films from the thermal reaction of ozone and TEOS exhibit relatively neutral stress and have a higher film density compared to low pressure processes. This increased density gives the oxide greater moisture resistance, lower wet etch rate and smaller thermal shrinkage. Compared to a 60-Torr process, the film density has increased from 2.09 to 2.15 g/cm^3; the wet etch rate decreased by more than 40%; and the thickness shrinkage changed from 12 to 4% after a 30-min anneal in dry N_2 at 1000°C [Lee et al., 1992].

16.17.5.2 CVD Phosphosilicate Glass Films

Adding a few percent of phosphine to the gas stream during deposition to obtain a lower melting point for the oxide (PH_3) results in a phosphosilicate glass. Numerous applications of this material exist, such as:

1. Interlevel dielectric to insulate metallization levels
2. Gettering and flow capabilities
3. Passivation overcoat to provide mechanical protection for the chip from its environment
4. Solid diffusion source to dope silicon with phosphorus
5. Fast etching sacrificial material in surface micromachining

Both wet and dry etching rates of PSG are faster than the undoped material and depend on the dopant concentration. Profiles over steps get progressively smoother with higher phosphorous concentrations, reflecting the corresponding enhancement in viscous flow [Levy and Nassau, 1986]. Increased ion bombardment (energy or density) in a PECVD PSG results in more stable phosphosilicate glass film with compressive as-deposited stress. Table 16.26 summarizes typical PSG process conditions [Wu et al., 1992].

The addition of boron to P-glass further lowers its softening temperature. Flow occurs at temperatures between 850 and 950°C, even with phosphorous concentration as low as 4 wt%. A BPSG doped at 4% boron and 6% phosphorus is normal. BPSG deposition conditions are shown in Table 16.27 [Bonifield et al., 1993].

TABLE 16.26 Typical PSG Process Conditions

Flow (sccm)	SiH_4	150–230
	N_2O	4500
	N_2	1500
	PH_3	150[a]
Temperature (°C)	T.C.	400
	Wafer	~380–390
Pressure (Torr)		2.2
RF power (watt)		1200
Deposition rate (Å/min)		4000–5000
Refractive index		1.46

[a] 10% PH_3 in N_2.

[b] 5% PH_3 in N_2.

Source: Wu, T.H.T. and R.S. Rosler, *Solid State Technol.,* May, 65–71, 1992. With permission.

TABLE 16.27 Typical BPSG Process Conditions

Parameter	Dimension	NSG	BPSG
Deposition temp.	°C	400	400
TEOS flow	g/min	0.33	0.66
O_2 flow	SLM	7.5	7.5
O_3/O_2	volume %	1	4.5
Carrier N_2 flow	SLM	18.0	18.0
B conc.	atomic %		4
P conc.	atomic %		6
Exhaust	mmH_2O	2.0	2.0
Growth rate	Å/min	1200	1800
Thickness	Å	1000	5800

Note: NSG = non-doped silicate glass; BPSG = borophosphosilicate glass.

From Bonifield, T., K. Hewes, B. Merritt, R. Robinson, S. Fisher, and D. Maisch, *Semicond. Int.*, July, 200–204, 1993. With permission.

16.18 Polysilicon Surface Micromachining Examples

Example 1. Analog Devices Accelerometer

Accelerometers based on lateral resonators represent the main application of surface micromachining today. To facilitate integration of their 50-g surface micromachined accelerometer (ADXL-50) with on-board electronics, Analog Devices opted for a mature 4-µm BICMOS process [Core et al., 1993]. Figure 16.106 presents a photograph of the finished capacitive sensor (center) with on-chip excitation, self-test and signal conditioning circuitry. The polysilicon-sensing element only occupies 5% of the total die area. The whole chip measures 500 × 625 µm and operates as an automotive airbag deployment sensor. The measurement accuracy is 5% over the ±50-g range. Deceleration in the axis of sensitivity exerts a force on the central mass that, in turn, displaces the interleaved capacitor plates, causing a fractional change in capacitance. In operation, the device has a force-balance electronic control loop to prevent the mass from actual movement. Straight flexures were used for the layout of the lateral resonator shuttle mass (see Figure 16.89B).

In the sensor design, n^+ underpasses connect the sensor area to the electronic circuitry, replacing the usual heat-sensitive aluminum connect lines. Most of the sensor processing is inserted into the BICMOS

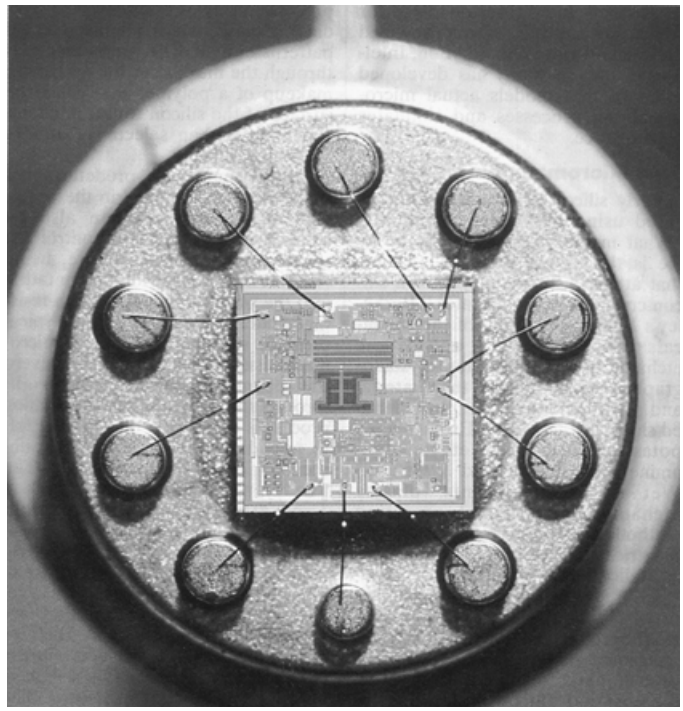


FIGURE 16.106 Analog Devices' ADXL-50 accelerometer with a surface micromachined capacitive sensor (center), on-chip excitation, self-test, and signal-conditioning circuitry. (From Core, T.A. et al., *Solid State Technol.,* October, 39–47 (1993). With permission.)

process right after the borophosphosilicate glass planarization. After planarization, a designated sensor region or moat is cleared in the center of the die (Figure 16.107a). A thin oxide is then deposited to passivate the n^+ underpass connects, followed by a thin, low-pressure, vapor-deposited nitride to act as an etch stop (buffer layer) for the final poly-Si release etch (Figure 16.107b). The spacer or sacrificial oxide used is a 1.6-μm densified low-temperature oxide (LTO) deposited over the whole die (Figure 16.107c). In a first timed etch, small depressions that will form bumps or dimples on the underside of the polysilicon sensor are created in the LTO layer. These will limit stiction in case the sensor comes in contact with the substrate. A subsequent etch cuts anchors into the spacer layer to provide regions of electrical and mechanical contact (Figure 16.107c). The 2-μm-thick sensor poly-Si is then deposited, implanted, annealed and patterned (Figure 16.108a). The relatively deep junctions of the BICMOS process permit the polysilicon thermal anneal as well as brief dielectric densifications without resulting in degradation of the electronic functions. Next is the IC metallization which starts with the removal of the sacrificial spacer oxide from the circuit area along with the LPCVD nitride and LTO layer. A low-temperature oxide is deposited on the poly-Si sensor part and contact openings appear in the IC part of the die where platinum is deposited to form a platinum silicide (Figure 16.108b). The trimmable thin-film material, TiW barrier metal and Al/Cu interconnect metal are sputtered on and patterned in the IC area. The circuit area is then passivated in two separate deposition steps. First, plasma oxide is deposited and patterned (Figure 16.108c), followed by a plasma nitride to form a seal with the earlier deposited LPCVD nitride (Figure 16.109a). The nitride acts as an HF barrier in the subsequent long etch release. The plasma oxide left on the sensor acts as an etch stop for the removal of the plasma nitride (Figure 16.109a). Subsequently, the sensor area is prepared for the final release etch. The undensified dielectrics are removed from the sensor and the final protective resist mask is applied. The photoresist protects the circuit area from the long-term buffered oxide etch (Figure 16.109b). The final device cross section is shown in Figure 16.109c.

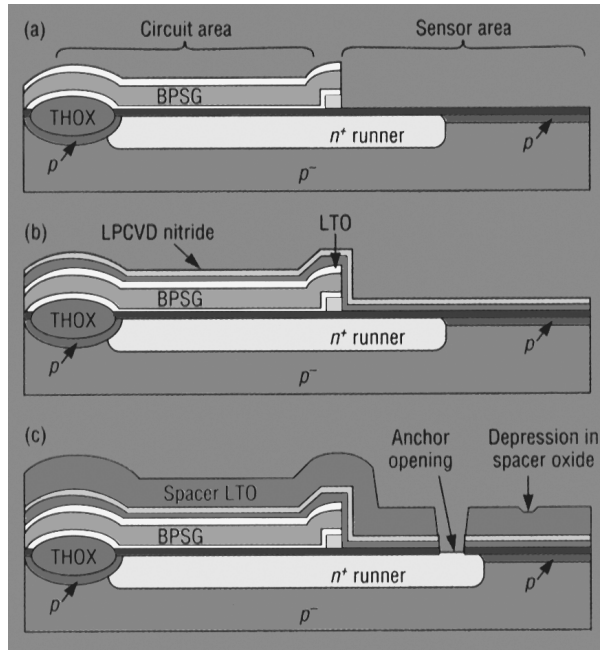


FIGURE 16.107 Preparation of IC chip for poly-Si. (a) Sensor area post-BPSG planatization and moat mask. (b) Blanket deposition of thin oxide and thin nitride layer. (c) Bumps and anchors made in LTO spacer layer. (From Core, T.A., W.K. Tsang, and S.J. Sherman, *Solid State Technol.*, 36, 39–47, 1993. With permission.)

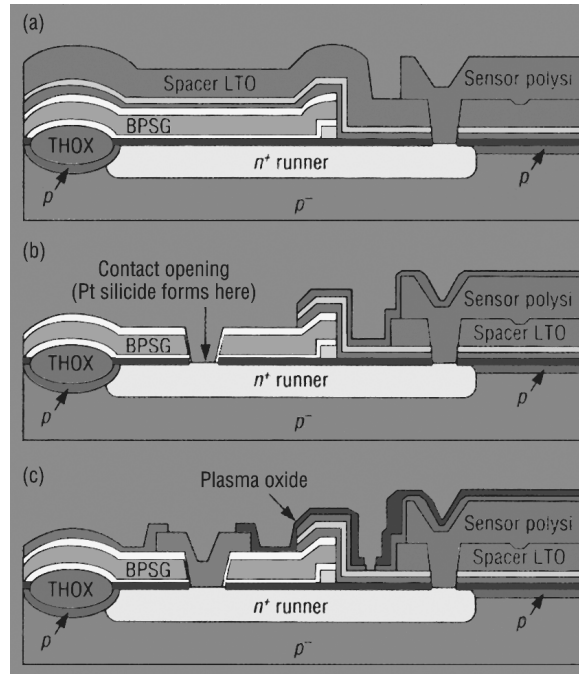


FIGURE 16.108 Poly-Si deposition and IC metallization. (a) Cross-sectional view after polysilicon deposition, implant, anneal, and patterning. (b) Sensor area after removal of dielectrics from circuit area, contact mask, and Pt silicide. (c) Metallization scheme and plasma oxide passivation and patterning. (From Core, T.A., W.K. Tsang, and S.J. Sherman, *Solid State Technol.*, 36, 39–47, 1993. With permission.)

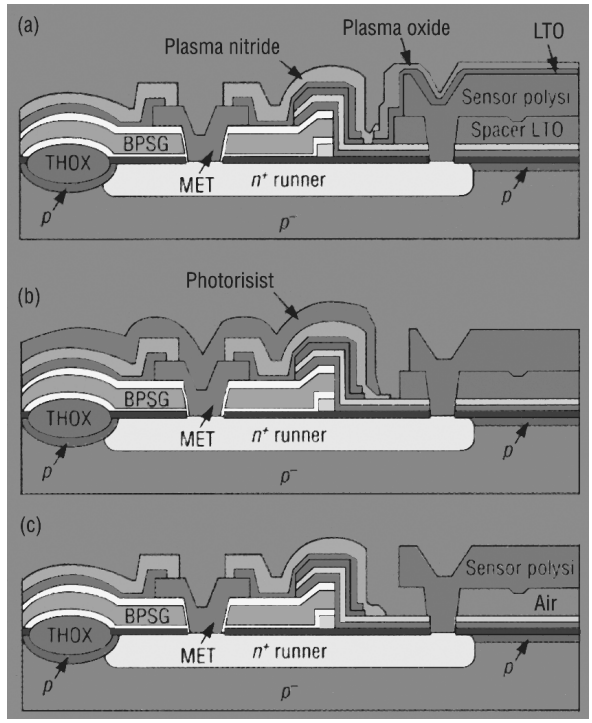


FIGURE 16.109 Pre-release preparation and release. (a) Post-plasma nitride passivation and patterning. (b) Photoresist protection of the IC. (c) Freestanding, released poly-Si beam. (From Core, T.A., W.K. Tsang, and S.J. Sherman, *Solid State Technol.*, 36, 39–47, 1993. With permission.)

Example 2. Polysilicon Stepping Slider

The principle of operation of the stepping slider is illustrated in Figure 16.110 [Akiyama, 1993; Akiyama and Shono, 1993]. Figure 16.110A shows a cross-sectional view of the polysilicon slider plate (length = 50 μm, width = 30 μm, height = 1.0 μm) and bushing (height = 1 μm) on an insulator film (Si_3N_4) as it sets one step. Figure 16.110B displays a schematic of the complete slider. At the rise of an applied voltage pulse on the slider rail, the polysilicon plate is pulled down. Since one end of the plate, supported by the bushing, cannot move, the other part is pulled down to come into contact with the surface of the insulator. The warp of the plate causes the bushing to shift. At the fall of the pulse, the distortion is released and the

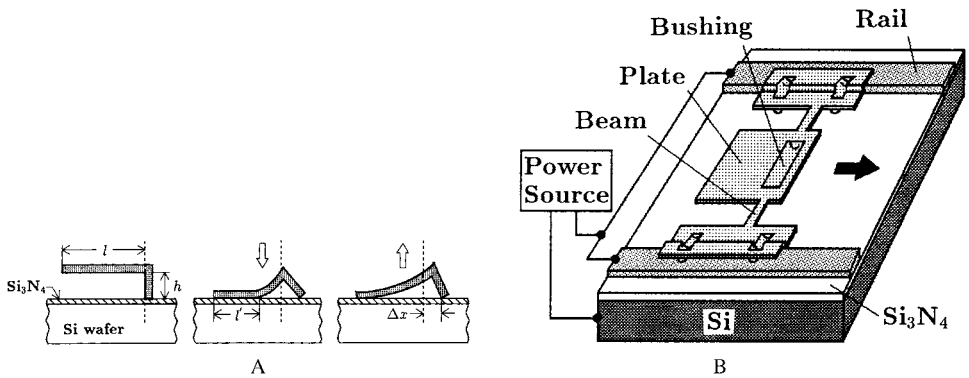


FIGURE 16.110 Principle of operation of stepping slider. (A) Cross-sectional view of the polysilicon plate and bushing on an insulator (Si_3N_4) on Si as the plate moves one step. (B) Schematic diagram of stepping slider.

plate snaps back to its original shape. If the size of the polysilicon step is Δx, the velocity of the polysilicon microstructure is given by:

$$v = \Delta x \cdot f \tag{16.64}$$

where f is the frequency of the pulse. The size of the step itself is given by:

$$\Delta x = \frac{h^2}{2(I - I')} \tag{16.65}$$

where I' stands for the length of the plate touching the insulator film.

Figure 16.111 illustrates the sequence of a stepping slider fabrication process. A layer of 0.3-μm silicon nitride is deposited at 900°C by the reaction of SiH_4 and NH_3 in N_2. Next, *in situ* phosphorus-doped polysilicon is deposited and patterned in a SF_6 plasma to form the sliding rail for the power supply of the slider (A) (mask 1). Thick sacrificial SiO_2 is deposited at 610°C by CVD of SiH_4 and O_2 in N_2. The thickness of the oxide (1 μm) determines the future bushing height. The oxide is patterned with a second mask exposing the silicon nitride in the area of the bushing. Fifty nm of CVD PSG is then deposited over the whole wafer at 610°C from the thermal reaction of SiH_4, PH_3 and O_2 in N_2 (B). In step C, 1.4-μm

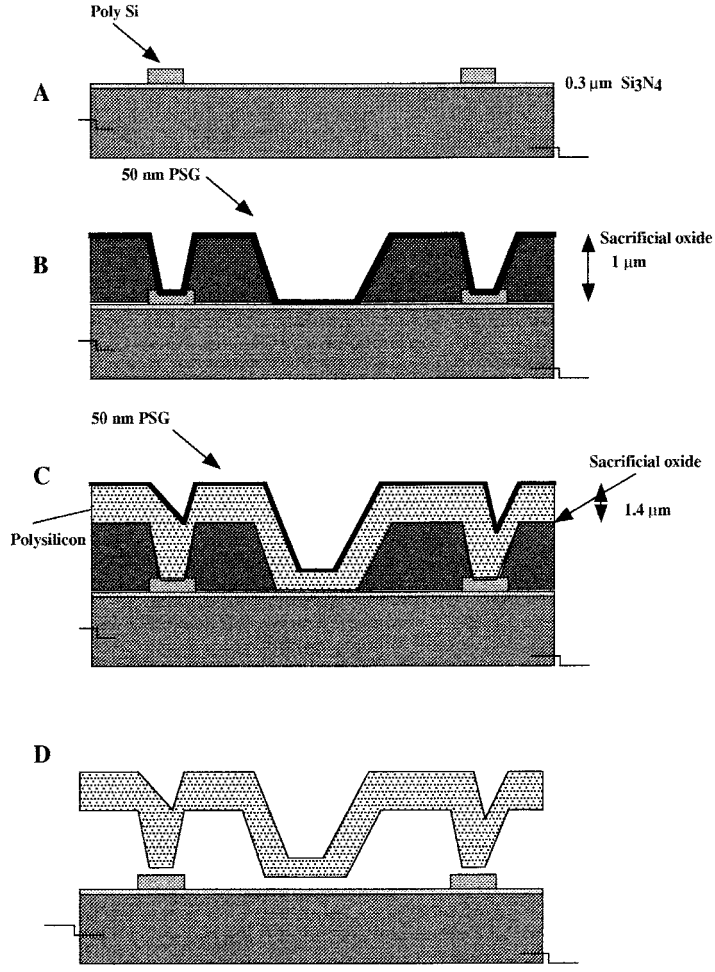
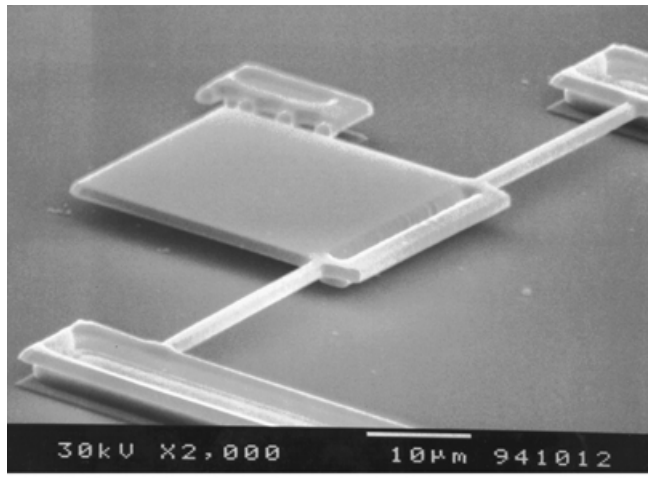
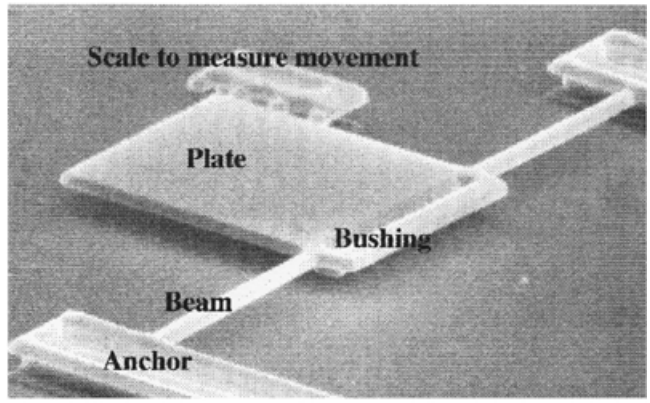


FIGURE 16.111 Process sequence for the fabrication of polysilicon stepper slider. (After Akiyama, T., *J. Microelectromech. Syst.*, 2, 106–110, 1993. With permission.)



A



B

FIGURE 16.112 SEM micrograph of the stepping slider (top) and scanned image (bottom). (From Akiyama, T., *J. Microelectromech. Syst.*, 2, 106–110, 1993. With permission.)

polysilicon is deposited at 610°C from SiH_4, coated with PSG and patterned with mask 3 to shape the slider plate. The silicon wafer is then heated in N_2 at 1050°C for 60 min to release the residual strain in the polysilicon and at the same time to activate and diffuse phosphorus from the PSG into the polysilicon slider. The last step (D) in the fabrication process is the release of the polysilicon slider, by dipping the wafer into 50% HF to fully dissolve the sacrificial oxide. Finally, the wafer is rinsed in deionized water and IPA (isopropyl-alcohol) and dried in N_2. In the fabrication process, to avoid washing away the slider in the rinse, the slider is attached by polysilicon springs to the end of the rail. The springs are cut by the step motion of the slider and subsequently the sliders can move along the rail. The velocity at the peak voltage of 150 V is 30 µm/sec with a 1200-Hz pulse. Figure 16.112 shows an SEM photo of the resulting slider (top). Components of the slider are named on the scanned image (bottom).

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