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Packaging of Harsh-Environment MEMS Devices

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23.1 Introduction

Microelectromechanical system (MEMS) devices, as they are defined, are both electrical and mechanical devices. Via microlevel mechanical operation, MEMS devices, as sensors, transform mechanical, chemical, optical, magnetic and other nonelectrical parameters to electrical/electronic signals; as actuators, MEMS devices transform electrical/electronic signal to nonelectrical/electronic operations. Therefore, MEMS devices very often interact with the environment electrically, magnetically, optically, chemically and mechanically. In order to support these nonconventional device operations (i.e., the device mechanical operation and the nonelectrical interactions between the device and their environments), new packaging capabilities beyond those provided by conventional integrated circuit (IC) packaging technology are required [Madou, 1997]. A chemically inert, optically dark and electromagnetically "quiet" environment for packaging conventional ICs, provided by hermetic sealing and electromagnetic screening, is no longer suitable for packaging most MEMS devices. Because MEMS devices have very specific requirements for their immediate packaging environment, it is expected that the design of MEMS packaging will be very device dependent. This is in contradiction to the conventional IC packaging practice in which a universal package design can accommodate many different ICs. Compared to conventional IC packaging, the most distinct issue of MEMS packaging is to meet the requirements imposed by the mechanical operability and reliability of MEMS devices.

NASA is interested in using harsh-environment-operable MEMS and electronic devices [Neudeck et al., 2000; McCluskey and Pecht, 1999; Kirschman, 1999; Willander and Hartnagel, 1997] to characterize *in situ* combustion environments of aerospace engines and the atmosphere of inner solar planets such as Venus. The operation environment of a high-temperature pressure sensor, one of the most wanted sensors by NASA and the aerospace industry for diagnosis and control of a new generation of aerospace engines, specifies the general requirements for packaging these harsh-environment MEMS: This pressure sensor must operate in an engine combustion chamber and be completely exposed to the combustion environment in order to measure *in situ* combustion chamber pressure in real time. The specifications of the high-temperature pressure sensor and the standard of *in situ* operation environment have all been determined by the Propulsion Instrumentation Working Group [PIWG, 2001]. The sensor operates at temperatures up to 500°C in a gas ambience composed of chemically reactive species such as oxygen in air, hydrocarbon/hydrogen in fuel, and catalytically poisoning species such as NO_x and SO_x in combustion products. The sensor operation environment is summarized as high temperature, high dynamic pressure and chemically corrosive. This is indeed a typical harsh environment compared to the standard operation conditions for most advanced (commercial) sensors/electronics, so the packaging materials and basic components—including substrate, metallization material(s), electrical interconnections (such as wirebond) and die-attach—must be able to withstand an environment that is 500°C, corrosive and especially oxidizing/reducing and with high dynamic pressure. As discussed in Chapter 20, one of the suggested high-temperature pressure sensors is a semiconductor piezoresistive device. The sensing mechanism of this device depends on the mechanical deformation of semiconductor resistors residing on a diaphragm fabricated by micromachining. Therefore, this device is very sensitive to external forces applied to the device. The major source of undesired external force is the thermal mechanical stress from the die-attach structure due to mismatches of coefficients of thermal expansion (CTE) of the die material (such as SiC), the substrate material and the die-attaching material. The thermal stress of the die-attach must be suppressed in order to achieve precise and reliable device operation because the thermally induced stress may generate unwanted device response to the changes in thermal environment, and in the extreme case thermal stress can cause permanent mechanical damage to the die-attach.

A high-temperature pressure sensor is needed for a planned space mission to determine the atmospheric pressure profile of Venus, where the temperature is up to 500°C and the gas ambient is chemically corrosive. Normal conditions of the operating environment of these pressure sensors include high temperatures (500°C), chemical corrosion and high dynamic pressure, under which most conventional electronic packaging materials can no longer operate. Therefore, development of revolutionary MEMS devices operable in harsh environments presents significant challenges to the device packaging field. In the next section, general material requirements for the major components of harsh-environment MEMS packaging are analyzed by adopting the basic structure of conventional IC packaging, in which the die is attached to a substrate using a die-attaching material layer and the die is electrically interconnected to the package by wirebond.

23.2 Material Requirements for Packaging Harsh-Environment MEMS

A summary of the basic requirements of the major materials needed for packaging harsh environment MEMS may help to establish the general guidelines for material selections.

23.2.1 Substrates

The basic function of the packaging substrate is to provide a framework for attaching the device die, metallization for electrical interconnection (such as wirebond), mounting the leads connecting the chip to the external environment, building nonelectrical signal paths and mechanical and possibly also electromagnetical shielding. Plastic/polymer-type materials are not suitable for 500°C operation because of melting and depolymerization at temperatures above 350°C [McCluskey et al., 1997; Pecht et al., 1999].

Most metal and alloy materials suffer severely from corrosion, especially, from oxidation at temperatures approaching 500°C in air. So the remaining material system suitable for substrate is ceramics, which meets the basic requirements for a substrate: excellent and stable chemical and electrical properties in a harsh environment, especially at high temperatures and corrosive gas ambience. After selecting the substrate material, a metallization scheme (both materials and processing) and associated sealing materials matching the substrate material must be identified or developed simultaneously. In order to reduce the thermal stress of the die-attach, the CTE of the substrate material must match that of the device material (such as SiC). The properties of substrate surface and the interfaces formed at high temperature with other packaging materials, such as the die-attach material, also become very important. At high temperatures, the surfaces of some ceramics (nitrides and carbides) gradually react with gas ambience, such as oxygen and water vapor, and therefore would lead to changes in properties such as surface resistivity and surface adhesiveness. Concerns such as these regarding the surface properties of "well-known" ceramic materials in high-temperature corrosive gas ambience may lead to valuable results from research into packaging materials for high-temperature MEMS.

23.2.2 Metallization/Electrical Interconnection System

Most metals and alloys, including some noble metals, oxidize at temperatures approaching 500°C in air. So the metals and alloys commonly used in conventional IC packaging such as Cu, Al and Au/Ni coated Kovar are excluded from packaging applications at 500°C and above, unless a perfectly hermetically sealed inert/vacuum condition is achievable. Intermetallic phases form at the interfaces of different metals such as Al and Cu at temperatures above 200°C. The intermetallic phase very often may reduce mechanical strength of an interconnection system, so achieving material consistency of an interconnection system becomes extremely important to avoid thermal mechanical failure at high temperatures.

Because of their chemical stability and good electrical conductivity, precious metals are naturally considered for applications in substrate metallization and electrical interconnection. Some precious metals (e.g., platinum and palladium) react with atomic hydrogen to form H-rich alloys at elevated temperatures [Lewis, 1967]. Though this is desirable for gas-sensing devices [Hunter et al., 1999] it is not for electrical interconnection applications, because the phase transition may cause significant changes in the physical and electrical properties. Gold (Au) is widely used for both substrate metallization and wirebond in packaging and hybridizing conventional high-frequency, high-reliability ICs. Besides the high conductivities and superior chemical stability at high temperatures, Au also has a low Young's modulus and a narrow elastic region. If Au is used as a die-attaching material, these properties of Au are helpful to reduce thermal stress generated at the Au–die and the Au–substrate interfaces due to CTE mismatches. These features of Au are especially desirable for applications in packaging 500°C-operable MEMS because a wide range of operating temperature is of concern. It has been reported that Au thin film/wire with small grain size suffers from electromigration of Au atoms at grain boundaries at high temperature under extreme current density (~10^6 A/cm^2) operation [Goetz and Dawson, 1996]. Surface modification and coating have been suggested for the Au conductor to withstand high-temperature and high-current-density operation [Goetz and Dawson, 1996]. The electrical migration effect is proportional to J^{-2} (J is the current density); therefore, the obtainable lifetime of a Au conductor operated at high temperature but low current density may still be substantial even without the surface modification as demonstrated in the next section. Developing a low-cost, highly conductive and thermally and chemically stable conductor with excellent thermal–mechanical properties for electrical interconnection is a valuable goal for packaging harsh-environment (high-temperature) devices [Grzybowski and Gericke, 1999; Harman, 1999].

23.2.3 Die-Attach

The basic function of die-attach is to provide mechanical, electrical and thermal support to the die. Most die-attaching (adhesive) materials used for packaging conventional ICs for operation at temperatures below 250°C are not suitable for 500°C operation. The basic failure mechanisms are depolymerization of epoxy-type materials, oxidizing and melting of eutectic-type materials and softening and melting of glass-type materials. Generally, we expect the die-attach materials to be electrically and thermally

conductive and physically and chemically stable at high temperatures and to permit a low-temperature attaching process. For applications in packaging MEMS devices, the thermal mechanical properties of the die-attach material such as CTE, Young's modulus, fatigue/creep properties and their temperature dependences are very much of concern, as the die-attaching material is the material in intimate contact, both thermally and mechanically, with the die and the substrate. The material properties, especially the CTE, are expected to match those of the die and the substrate materials. In case the CTE of the die is not completely consistent with that of the substrate, the die-attaching material is ideally expected to thermomechanically compensate for any possible CTE mismatch between the die and the substrate materials by absorbing the thermal strain. Another major concern regarding die-attaching materials for packaging high-temperature MEMS devices is the long-term chemical and mechanical stability of the interfaces formed with the die (or the metallization of the die) and substrate (or the metallization of the substrate) materials at high temperatures. If the die-attach is expected to be electrically conductive, then the electronic properties of its interface with the die (or the metallization materials on the die) would also become critically important. Combining all these thermal mechanical, chemical and electrical requirements for die-attaching material, it is apparent that a material system for die attach with a suitable process is critical to success in packaging high-temperature MEMS device.

The thermomechanical stress in the die-attach due to the differences in properties of the materials of the die-attach structure (particularly CTE mismatch) may cause degradation and failure of packaged devices. The extreme case of die-attach failure caused by thermal stress is cracking of the die or the attaching material. Besides this catastrophic failure due to fatigue and creep of the die or the attaching material(s), thermal stress in die-attach can also cause the high-temperature MEMS device an undesired thermal response, irreproducibility of device operation, and output signal drift. Therefore, thermal mechanical failure due to CTE mismatches of the materials involved in the die-attach is expected to be a common and important thermal mechanical issue that must be addressed, especially for high-temperature MEMS devices.

23.2.4 Hermetic Sealing

The basic purpose of hermetic sealing is to create and maintain a stable and sometimes inert ambience for the packaged device. This simple function at low (room) temperature is difficult to achieve at temperatures approaching 500°C because, first, at such high temperatures most soft or flexible sealing materials such as plastic/polymer-based materials can no longer operate; second, sealing very often applies between different materials. The CTE mismatches of these materials make hermetic sealing difficult over a wide temperature range, especially under thermal cycling condition. Third, high temperatures activate and significantly promote thermal processes such as diffusion and degassing at material surfaces [Palmer, 1999], thus it becomes difficult to maintain an ambience in a small enclosure by sealing. Therefore, it is expected that creative sealing concepts are necessary to meet the requirements for packaging many high-temperature MEMS devices.

Harsh-environment MEMS packaging offers new challenges to the device packaging field. Discussions on the basic requirements of properties of the materials necessary for packaging harsh-environment MEMS are followed by addressing an electrical interconnection system (both electrically and mechanically) that is based on a ceramic substrate and thick-film metallization, with a compatible conductive die-attach scheme for chip-level packaging of low-power, harsh-environment SiC MEMS devices. The thermal mechanical optimization of Au thick-film material-based die-attach is discussed using nonlinear finite element analysis (FEA) results.

23.3 High-Temperature Electrical Interconnection System

As discussed in the last section, ceramic materials are naturally selected as packaging substrate materials because of their superior high-temperature chemical and electrical stabilities. Aluminum oxide (Al_2O_3) is a low-cost substrate widely used for conventional IC packaging. Another advantage of using Al_2O_3 is that many thick-film materials have been developed for metallization of Al_2O_3. In comparison to Al_2O_3,

aluminum nitride (AlN) has a higher thermal conductivity and a low CTE that is very close to that of SiC. These features of AlN make it be useful in packaging high-temperature and high-power devices [Martin and Bloom, 1999]. If the basic framework of conventional IC packaging is adopted, the next step after selecting the substrate is to identify metallization material(s). In this section we review a Au thick-film-based 500°C operable electrical interconnection system for chip-level, low-power, harsh-environment MEMS packaging [Chen et al., 2000a; 2000c].

Thick-film metallization materials are usually composed of fine metal (such as gold) powder, inorganic binder (such as metal oxides) and organic vehicle. The screenprinting technique is usually used for thick-film coating for thickness control and patterning. During the initial drying process (at 100 to 150°C), the organic vehicle evaporates and the paste becomes a semisolid phase mixture of metal powder and binder. In the final curing process (~850°C recommended for most thick-film products), the inorganic binder molecules migrate to the metal/substrate (e.g., Au–ceramic) interface and form reactive binding chains. Au thin wires can be bonded directly to Au thick-film metallization pads using commercialized wirebond equipment to provide electrical interconnection in the packaging. Some new thick-film materials may be applicable to various ceramic substrates such as alumina (Al_2O_3) [Keusseyan et al., 1996] and aluminum nitride [Chitale et al., 1994; Shaikh, 1994; Keusseyan et al., 1996]. Compared with direct thin-film metallization on ceramic substrate, thick-film metallization offers low cost, simple process, low resistance, and better adhesion provided by the reactive binders at metal–substrate interface. Both the electrical and mechanical properties of Au thick-film materials for applications in hybrid-packaging conventional ICs have been extensively validated at $T < 150$°C. In order to evaluate Au thick-film materials for 500°C application, both electrical and mechanical tests at 500°C are necessary. Test results of Au thick-film-material-based electrical interconnections (Au thick-film printed wires and thick-film-metallization-based Au wirebond) and a conductive die-attach scheme using Au thick-film as die-attaching material for operation up to 500°C [Chen et al., 2000c] are reviewed as follows.

23.3.1 Thick-Film Metallization

A Au thick-film-printed wire circuit, as shown in Figure 23.1, was screenprinted on a ceramic substrate (AlN or 96% Al_2O_3) and cured at 850°C in air using the recommended curing process, forming printed wire and metallization pads for wirebond on ceramic substrate. The circuit was electrically and thermally tested at 500°C in air for a total of ~1500 hr by four-probe resistance measurement. The electrical resistance of the thick-film wire/circuit was first measured at room temperature; afterward, the temperature

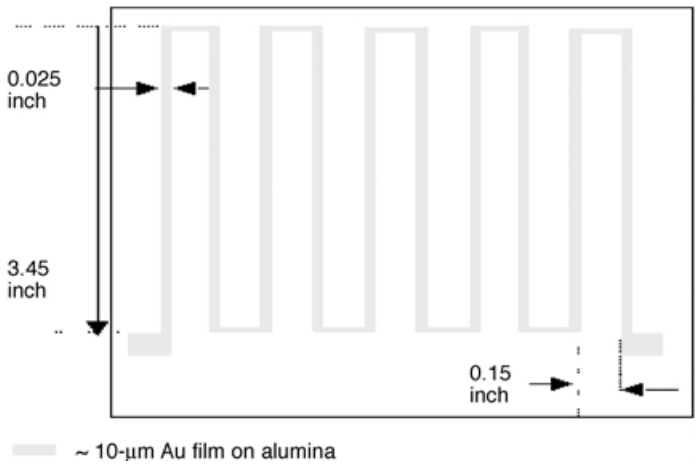


FIGURE 23.1 Schematic diagram of Au thick-film printed wire for high-temperature tests.

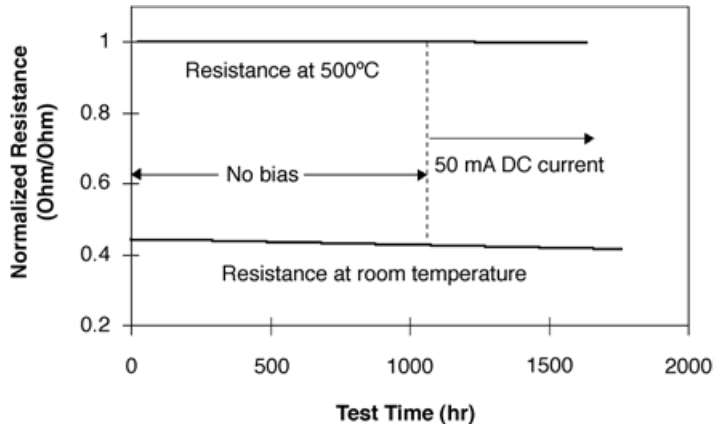


FIGURE 23.2 Normalized resistance of thick-film wire at various temperatures with and without dc bias.

was ramped up to 500°C for ~1000 hr without electrical current flow, and the resistance of the wire was measured periodically during this period of time. The resistance slightly fluctuated within ±0.1% during the 1000 hours test, as shown in Figure 23.2. After testing for 1000 hr without electrical bias, the circuit was biased with 50 mA dc current and the resistance was continuously monitored by four-probe resistance measurement. The resistance fluctuated slightly within ±0.1% for 500 hr with electrical bias. This very small change in resistance is acceptable for almost all envisioned high-temperature device packaging application.

As discussed earlier, Au thick-film materials for various substrates have been systematically validated both electrically and mechanically for conventional IC packaging; however, in order to be reliably applicable at high temperatures, these Au thick-film material systems must be mechanically evaluated at elevated temperatures in addition to the electrical validation discussed above. The tensile strength of Au thick-film metallization on a 96% Al_2O_3 substrate has been tested at room temperature after extended storage at 500°C [Salmon et al., 1998]. In order to examine the mechanical strength and the thermal dynamic stability of the binding system of Au thick films at high temperatures, the shear strength of selected Au thick-film metallization on 96% Al_2O_3 substrate was tested at temperatures up to 500°C [Chen et al., 2001]. The shear strength (breaking point) at 500°C reduced by a factor of ~0.80 with respect to that at 350°C, while the shear strength (breaking point) at 350°C was close to that at room temperature. The shear strengths of selected Au thick films designed for AlN were not as high as those for Al_2O_3 but were sufficient for application in microsystem packaging operable at 500°C.

23.3.2 Thick-Film-Based Wirebond

After the qualifications of Au thick-film metallization, the thick-film-based wirebond needs to be evaluated for high-temperature operation. The electrical test circuit including Au thick-film printed wires/pads and multiple thin gold wires bonded to the thick-film pads is illustrated in Figure 23.3. The geometry of the printed thick-film conductor was designed so that the electrical resistance of the test circuit was dominated by the resistance of thin (0.0254-mm diameter) bonded gold wires. The thick-film conductive wires/pads were processed according to the standard drying and curing processes [DuPont, 1999] suggested by the material manufacturer. The thin gold wires were bonded to the thick-film pads on the substrate by a thermal-compression wirebonding technique.

The electrical resistance of a thick-film-metallization-based wirebond test circuit (Figure 23.3) includes those of thick-film conductive wire/pads, bonded thin Au wires, and the interfaces of the wirebonds. The resistances of 22 units (44 bonds) in series were measured at room temperature and 500°C vs. accumulated

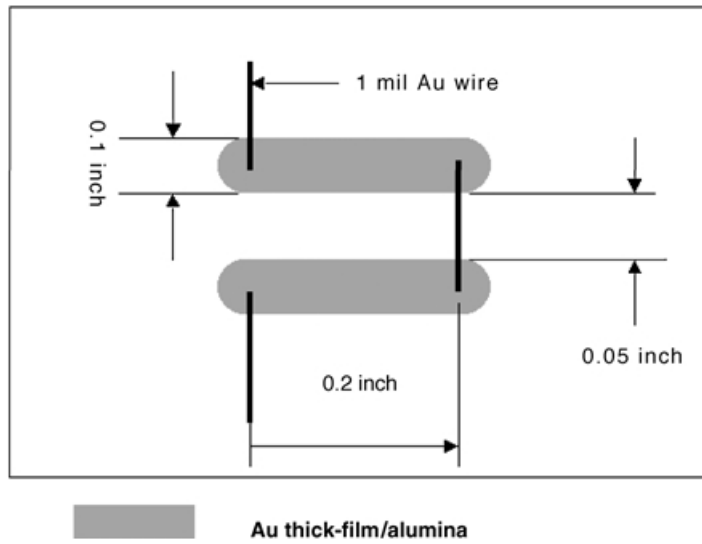


FIGURE 23.3 Schematic diagram of one unit of thick-film-metallization-based wirebond test circuit; 0.0254-mm (0.001 in.) Au wires were bonded to thick-film pads using the thermal-compression technique.

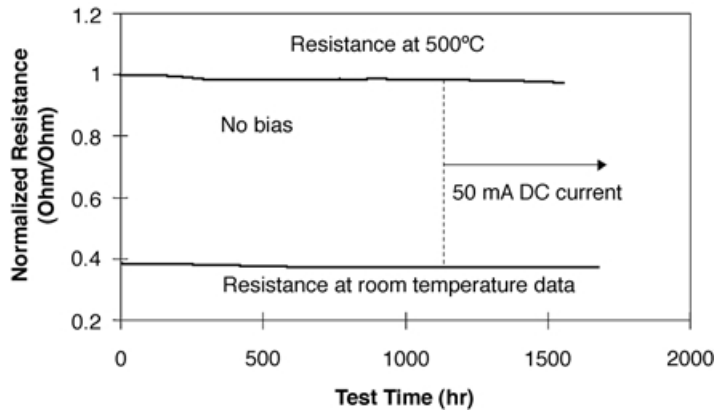


FIGURE 23.4 Normalized resistance of thick-film-metallization-based wirebond at various temperatures with and without dc bias.

testing time at 500°C. The resistance was first measured at room temperature, after which the temperature was ramped to 500°C and the resistance was monitored in air without electrical bias for 670 hr. As shown in Figure 23.4, the temperature was then lowered back to room temperature and the resistance was recorded again. After this thermal cycle, the circuit resistance was continuously monitored for a total of 1200 hr at 500°C in air without electrical bias (current flow), followed by another 500 hr at 500°C with 50-mA (dc) current. The resistances under all these conditions were desirably low (less than 0.5 Ω per unit) and decreased slowly and slightly at an average rate of 2.7% over the 1500-hr testing period. The rate of resistance decrease under the dc bias is close to that without electrical bias.

An identical wirebond sample was electrically tested in a dynamic thermal environment. The same wirebond circuit was tested in thermal cycles between room temperature and 500°C with an initial temperature rate of 32°C/min for 123 cycles and a dwell time of 5 min at 500°C, then at the temperature rate of 53°C/min (higher than thermal shock rate) for an additional 100 cycles with 50-mA dc current.

The maximum change in electrical resistance, during the thermal cycle test, was 1.5% at room temperature and 2.6% at 500°C [Chen et al., 2001]. The electrical stability of this Au thick-film-based wirebond system should meet most interconnection needs for high-temperature, low-power applications.

23.3.3 Conductive Die-Attach

23.3.3.1 SiC Test Die

The fabrication of a high-temperature SiC Schottky diode used to test the conductive die-attach scheme was previously reported in detail [Chen et al., 2000b]. An N-type (nitrogen, resistivity less than 0.03 Ω-cm), Si-terminated 4H-SiC wafer was used to fabricate test Schottky diode. The backside wafer (unpolished side) was first coated with a nickel (Ni) thin film by electron beam evaporation. The SiC wafer was then annealed at 950°C in argon in a tube furnace for 5 min, forming an ohmic contact on the backside of the SiC wafer. The device structure on the front side of the SiC wafer was fabricated by electron-beam evaporation of thin titanium (Ti) and thin Au films on cleaned SiC wafer and patterned with the liftoff technique.

23.3.3.2 Conductive Die-Attach

After dicing, the 1-mm × 1-mm SiC diode chips were attached to a ceramic substrate (either AlN or 96% alumina) using selected Au thick-film materials, as shown in Figure 23.5. An optimized thick-film die-attaching process for SiC device results in a low-resistance, conductive die-attach that is very often required for packaging devices requiring backside electrical contact.

The SiC test die with a Ni contact on the back was attached to a ceramic substrate using an optimized two-step Au thick-film processing [Chen et al., 2000b]. A thick-film layer was first screenprinted on the substrate and cured at 850°C using the standard process. The SiC die was then attached to the cured thick-film pattern with a minimal amount of subsequent thick film. A slower drying process (120 to 150°C) was critical to keeping the thick-film bonding layer uniform and the die parallel to the substrate after the curing process. Following the drying, the attached die was processed at a lower final curing temperature (600°C).

This optimized Au thick-film die-attach process allows sufficient diffusion of inorganic binders toward the thick film–substrate interface, resulting in a good strength of binding to the ceramic substrate. Meanwhile, it prevents the attached semiconductor chip from being exposed to temperatures above the ultimate operation temperature of SiC devices (600°C) during the die-attach process. The second advantage of this die-attach process is that the distribution of the thick film (after the final curing) between the chip and the substrate can be better controlled because only a minimal amount of thick-film material is necessary to attach the chip to a cured thick-film pad. Therefore, many potential problems caused by nonuniform thick-film distribution at the chip–substrate interface might be avoided.

A 0.001-in.-diameter Au wire was bonded onto the top of the Au thin-film metallization area covered with a Au thick-film overlayer by the thermal-compression bonding technique. Thick-film material was also used to reinforce the top Au thin film for better wire bonding. The Au thin-film metallization area

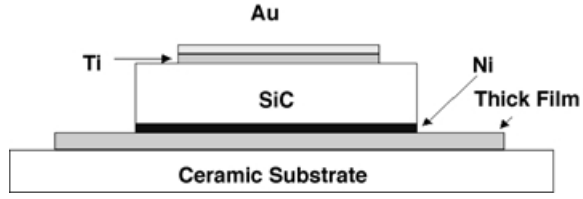


FIGURE 23.5 Schematic diagram of as-fabricated SiC device and die-attach structure.

was coated with thick film on the top then dried at 150°C for 10 min. The thick film on the device top was cured during the final die-attach process (at 600°C).

23.3.3.3 Electrical Test

The attached SiC test diode (Figure 23.5) was characterized by current–voltage (I–V) measurements at both room temperature and 500°C for various heating times at 500°C. A minimum dynamic resistance (dV/dI) under forward bias which is reduced from the I–V curve was used to estimate the upper limit of resistance of the die-attach structure (both interfaces and materials) and to monitor the resistance stability of the die-attach, as shown in Figure 23.6. This dynamic resistance includes the forward dynamic resistance of the Au–Ti–SiC interface, SiC wafer bulk resistance, the die-attach materials/interfaces resistance, bonded wire resistance and the test leads resistance in series. The resistance contributed from test leads and bonded wire were measured independently and subtracted. The attached device was first characterized by I–V measurements at room temperature. The device exhibited rectifying behavior, and the minimum dynamic resistance after subtracting the test-leads/bond-wire resistance (which also applies to all of the following discussion) measured under forward bias was ~2.6 Ω, as shown in Figure 23.7.

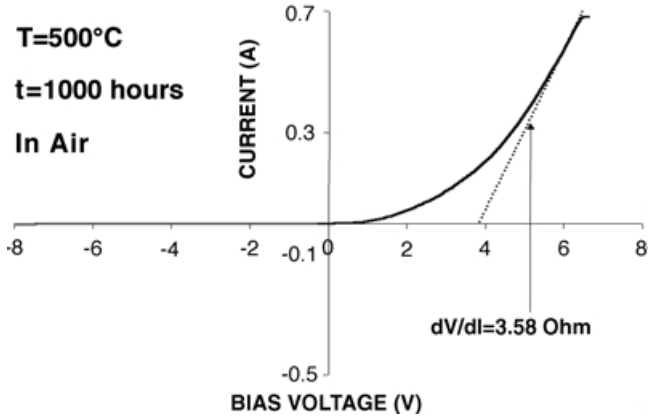


FIGURE 23.6 I–V curve of an attached SiC test diode characterized at 500°C after being tested for 1000 hr in 500°C oxidizing air.

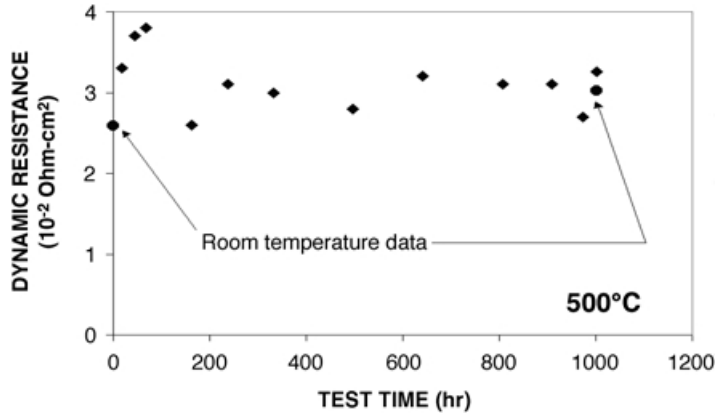


FIGURE 23.7 Minimum specific dynamic resistance (normalized to device area) calculated from I–V data vs. heating time at 500°C. This resistance includes resistances contributed from the Au(Ti)–SiC rectifying interface, SiC wafer and die-attach materials/interfaces. Resistances of the bonded wire and the test leads have been subtracted.

The temperature was then ramped up to 500°C (in air) and the diode was *in situ* characterized periodically by I–V measurement for ~1000 hr. During the first 70 hr at 500°C, the minimum dynamic resistance under forward bias increased slightly from 3.3 to 3.8 Ω. After that, the minimum dynamic resistance decreased slightly and remained at an average of 3.1 Ω. The diode was then cooled down to room temperature and characterized again. The minimum forward dynamic resistance measured at room temperature was 3.3 Ω. It is worth noting that the I–V curve of the device changed somewhat with time during heat treatment at 500°C. However, the minimum dynamic resistance of the attached diode remained comparatively low over the entire duration of the test and the entire temperature range, indicating a low and relatively stable die-attach resistance.

23.4 Thermomechanical Properties of Die-Attach

By adopting a conventional die-attach structure, in which the die backside is attached to a substrate using a thin attaching material layer, the die-attach using Au thick-film material discussed in the last section (illustrated in Figure 23.5) is a typical example of this structure. As discussed previously, the most important issue that concerns the thermal mechanical reliability of a packaged MEMS is the die-attach thermal stress and the guidelines for material selection, structure design and optimization of the attaching process to minimize the overall die-attach thermal stress effects on the mechanical operation of the device.

We start with a list of static equations governing the thermomechanical behavior of the die-attach structure to analyze the material properties and other factors determining the thermal mechanical properties of the structure. Following that, optimization of the die-attach thermal mechanical reliability is discussed using the simulation results of nonlinear finite element analysis [Lin, 2001].

23.4.1 Governing Equations and Material Properties

Assuming that the temperature distribution in the die-attach is static ($\frac{\partial T}{\partial t} = 0$) and uniform ($\frac{\partial T}{\partial x} = \frac{\partial T}{\partial y} = \frac{\partial T}{\partial z} = 0$), and the external force on the die-attach structure is zero, the general thermal mechanical governing equations for the die-attach system are

$$\frac{\partial^2 u}{\partial x^2} + \frac{\partial^2 v}{\partial x \partial y} + \frac{\partial^2 w}{\partial x \partial z} + (1 - 2\nu)\nabla^2 u = 0 \tag{23.1}$$

$$\frac{\partial^2 v}{\partial y^2} + \frac{\partial^2 u}{\partial x \partial y} + \frac{\partial^2 w}{\partial y \partial z} + (1 - 2\nu)\nabla^2 v = 0 \tag{23.2}$$

$$\frac{\partial^2 w}{\partial z^2} + \frac{\partial^2 u}{\partial x \partial z} + \frac{\partial^2 v}{\partial y \partial z} + (1 - 2\nu)\nabla^2 w = 0 \tag{23.3}$$

where $\nabla^2 = \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2}$; u, v and w are the displacements in the x, y and z directions, respectively; ν is Poisson's ratio of the material. The normal stress distribution are determined by material properties, the temperature and the displacements [Lau et al., 1998]:

$$\sigma_x = \frac{\lambda}{\nu}\left[(1 - \nu)\frac{\partial u}{\partial x} + \left(\frac{\partial v}{\partial y} + \frac{\partial w}{\partial z}\right)\right] - \beta(T - T_o) \tag{23.4}$$

$$\sigma_y = \frac{\lambda}{\nu}\left[(1 - \nu)\frac{\partial v}{\partial y} + \left(\frac{\partial w}{\partial z} + \frac{\partial u}{\partial x}\right)\right] - \beta(T - T_o) \tag{23.5}$$

$$\sigma_z = \frac{\lambda}{\nu}\left[(1 - \nu)\frac{\partial w}{\partial z} + \left(\frac{\partial u}{\partial x} + \frac{\partial v}{\partial y}\right)\right] - \beta(T - T_o) \tag{23.6}$$

Shear stress are reduced from u, v and w as:

$$\tau_{xy} = \frac{E}{2+2\nu}\left(\frac{\partial u}{\partial y} + \frac{\partial v}{\partial x}\right) \tag{23.7}$$

$$\tau_{yz} = \frac{E}{2+2\nu}\left(\frac{\partial v}{\partial z} + \frac{\partial w}{\partial y}\right) \tag{23.8}$$

$$\tau_{zx} = \frac{E}{2+2\nu}\left(\frac{\partial w}{\partial x} + \frac{\partial u}{\partial z}\right) \tag{23.9}$$

where $\lambda = \frac{\nu E}{(1+\nu)(1-2\nu)}$, and $\beta = \frac{\alpha E}{1-2\nu}$. E is Young's modulus and α is the coefficient of linear thermal expansion (CTE). Material properties α, E and ν generally vary from the die to the attaching layer and the substrate. If there is no residual stress at a certain temperature, such as the die-attaching temperature, then the mismatch of CTEs of the die-attach is the major source of thermal mechanical stress. This would become more apparent if the governing equations, Eqs. (23.1) to (23.3), are listed for the die, the attaching layer and the substrate separately. There would be an external force term in these equations because of the mechanical interactions at the boundaries—the interface between the die and the attaching layer and the interface between the attaching layer and the substrate. These external force terms are generated by the mismatch of material CTEs or the residual stresses. In case there is no residual stress and the CTEs match with each other, these external force terms vanish and solutions for the equations would be trivial.

In the temperature range for conventional IC packaging, all these material properties can be approximated as constants. However, in the operation temperature range from room temperature to 500°C, the temperature dependences of these material properties must be quantitatively considered for a precise solution for these equations.

The boundary conditions at the interface between the die and the attaching layer and the interface between the attaching layer and the substrate are largely determined by the bonding quality and the thermal mechanical stability of the die/attaching layer interface and the attaching layer/substrate interface. The simplest model of boundary conditions is ideal bonding: The continuity of all displacement components at interfaces in the entire temperature range $u|_{S_s+} = u|_{S_s-}$, $v|_{S_s+} = v|_{S_s-}$, $w|_{S_s+} = w|_{S_s-}$, $u|_{S_a+} = u|_{S_a-}$, $v|_{S_a+} = v|_{S_a-}$ and $w|_{S_a+} = w|_{S_a-}$. S_s is the interface between the die and the attaching material, and S_a is the interface between the attaching material and the substrate, respectively.

The effects of thermal mechanical stress on the performance of a material/component are usually evaluated by either Von-Mises stress, $\sigma_{VM} = 1/2 S_{ij} S_{ij}$ (the deviation stress tensor, $S_{ij} = \sigma_{ij} - 1/3\sigma_{\alpha\alpha}\delta_{ij}$, where $\delta_{ij} = 1$ for $i = j$, and $\delta_{ij} = 0$ for $i \neq j$), or the maximum principle stress σ_{MP} [Giacomo, 1996].
Assume:

1. The substrate size is much larger than that of die and the material is amorphous/polycrystalline (isotropic).
2. One of the basal planes of the chip crystal is parallel to the die-attach interface.
3. Boundary conditions at the interfaces are determined by ideal bonding; all displacement components are continuous at both the interface between the die and the attaching layer and the interface between the attaching layer and the substrate.
4. The die-attach structure is in a uniform temperature field.

Then, the maximum thermal stress distribution, either Von-Mises stress or maximum principle stress (MPS), is basically a function of the thickness of the die (θ_d); the thickness of the attaching material layer (θ_a); the properties E, α and ν of the die material (E_d, α_d and ν_d); the properties of the attaching material (E_a, α_a and ν_a); the properties of the substrate material (E_s, α_s and ν_s); and the temperature deviation from the thermal stress relaxing temperature, $T - T_R$, where the T_R is thermal stress relaxing temperature:

$$\sigma = \sigma(x, y, z, \theta_d, \theta_a, \theta_s, \vec{M}_d, \vec{M}_a, \vec{M}_s, (T - T_R)) \tag{23.10}$$

where $\vec{M}_{d,a,s}$ are material property parameters of the die, the attaching material and the substrate, respectively. For 500°C operable packaging, because the operation temperature range is, relatively, much wider compared to that for conventional ICs, the temperature dependencies of these material properties and their nonlinearity have to be considered for a precise assessment of the stress/strain distribution. Usually σ is symmetric about the vertical die central axis if the package dimensions are much larger than those of the die. For example, if the die is in a square shape, σ has approximately lateral fourfold (90°) symmetry about the vertical die central axis. In case the die surface is off the crystal basal plane, then σ depends on the angle off the basal plan, and the horizontal symmetry of σ reduces from 90° to 180°. Ideally, if the CTEs of the die, attaching materials and substrate are consistent with each other in the entire operation temperature range and stress is relaxed as an initial condition, then at any temperature:

$$\sigma = \sigma(x, y, z, \theta_d, \theta_a, \vec{M}_d = \vec{M}_a = \vec{M}_s, (T - T_R)) = 0 \tag{23.11}$$

At the relaxing temperature, T_R, the global thermal stress is largely relaxed: $\sigma = \sigma(x, y, z, \theta_d, \theta_a, \vec{M}_d, \vec{M}_a, \vec{M}_s, (T = T_R)) = 0$. Sometime the stress distribution at relaxing temperature may not be completely relaxed but reaches a minimum; this minimum stress depends on the die-attaching material, the physical and chemical processes of die-attaching and the thermal experience of the die-attach.

Consider thick-film material-based die-attach as an example. T_R is basically the final curing temperature if the cooling process after the final curing is so rapid that thermal stress does not have a chance to relax through sufficient diffusion at lower temperatures. However, T_R can be lower than the final curing temperature if the cooling process is so slow that a relaxing configuration is reached at lower temperatures. Therefore, T_R is initially determined by a die-attach processing temperature but it may change with the thermal history (temperature vs. time) after the attachment. The dependence of T_R on the thermal history is not desired because this may cause a reproducibility problem for device response. The basic physical/chemical attaching process certainly has significant impact on T_R. For some die-attach materials and attaching process, such as phase-transition material, T_R may not be the die-attach processing temperature.

In addition to the direct impact from material properties of the attaching layer, the thermomechanical properties of the interfaces between the die, the attaching layer and the substrate are also important to the thermal stress–strain configuration of the die-attach structure. The interfacial shear elastic/plastic properties, the interfacial fatigue/creep behavior, and their temperature dependencies are determined by the chemical/physical interactions between the materials composing the interface. If the materials chemically react at the interface, an interphase may form and dominate the interfacial thermomechanical properties. The thermal mechanical properties of these interphases can certainly be critical to the overall thermomechanical properties of the die-attach structure.

In order to improve the thermal mechanical reliability of the packaged device the thermomechanical properties of the die-attach need to be optimized either locally or globally through material selection, structure design and process control. The guideline for local optimization is to minimize the maximum local thermal stress where the device mechanically operates to optimize mechanical operation with the least thermal stress effects. The guideline for global optimization is to minimize the weighted global stress. The parameters that can be adjusted to thermomechanically optimize the die-attach structure are $\vec{M}_a$, $\vec{M}_s$, θ_a and T_R after determination of die material and die size.

The thermal mechanical governing Eqs. (23.1) to (23.3) are so complicated that closed nontrivial (analytical) solutions of these equations are very difficult to obtain even for simple boundary geometry. The nonlinear temperature dependences of the material properties make it almost impossible to solve the equations with closed analytical solutions; however, numerical computing methods such as finite element analysis provide a powerful tool for simulation and optimization of the thermomechanical properties of a die-attach structure through material selection, structure design and processing control. Numerical methods make it possible to calculate the thermomechanical configuration of the packaging components/materials in a wide temperature range; however, it is still not trivial to optimize a die-attach

structure for operation in a wide temperature range using FEA simulation because of the following reasons:

1. The numerical calculations involved in FEA sometimes can be difficult, especially when the boundary geometry of the MEMS devices is complicated and the dimensions of the mechanical structures are much smaller than the die-attach size [Rudd, 2000].
2. Currently, thermomechanical and fatigue/creep properties of many electronic and packaging materials in such a wide and high temperature range are often not completely available.
3. If the die-attaching process is based on phase-transition phenomena, then detailed changes in the thermomechanical properties of the attaching material, before and after the phase transition, may not be completely known.
4. Quantitative modeling of interfaces between the die, attaching layer, and substrate can be difficult.

Lin and Zou used a Si stress-monitoring chip to measure surface stress–strain of a die-attach [Lin et al., 1997a; Zou et al., 1999]. This unique *in situ* stress–strain monitoring method can be modified by using a high-temperature-operable SiC stress-monitoring chip to optimize the die-attach for high-temperature MEMS packaging.

23.4.2 Thermomechanical Simulation of Die-Attach

For high-temperature MEMS packaging, the thermomechanical reliability of a die-attach structure needs to be addressed at two levels: (1) mechanical damages of a die-attach structure resulted from thermal mechanical stress, and (2) thermal stress–strain effects on the mechanical operation of the device. Failures at both levels are rooted in thermomechanical stress in the die-attach. In the remaining part of this section FEA simulation results [Lin, 2001] of the Au thick-film-based SiC die-attach reviewed in the last section are analyzed as an example of die-attach optimization for high-temperature MEMS packaging.

23.4.2.1 High-Temperature Material Properties

The basic thermal and mechanical properties of SiC, Au, AlN and 96% Al_2O_3 and their temperature dependences used for FEA simulation are listed in Table 23.1 [Lin, 2001]. The temperature dependence of Young's modulus of AlN in a wide temperature range has not been reported, so it is extrapolated as a constant from the data at room temperature. The Poisson's ratios of 4H single-crystal SiC and AlN are not available; they were estimated according to those of other carbides and nitrides. The thermal and mechanical properties of 4H-SiC were assumed to be isotropic. Because the yield strength of gold thick-film material has not been published either, the simulation was conducted in a range of values from 650 to 3000 psi. However, computations using the yield strength at the low end very often diverged so the calculation was difficult.

23.4.2.2 Stress Distribution and Die Size Effects

Figure 23.8 shows Von-Mises stress and maximum principle stress contours of a quarter of a SiC–Au–AlN die-attach structure at room temperature assuming the relaxing temperature is 600°C. Horizontally, at the interface with the Au thick-film layer, the stress in the die basically increases with the distance from the center of the die-attach interface; the stress reaches a maximum at the area close to the die edges, especially at the corner area. This is understandable. The source of thermal stress of the die-attach structure is CTE mismatch at bonding interfaces. At the area far from the neutral point (larger distance from neutral point, DNP) the trends of relative displacement with respect to Au thick-film, driven by the CTE mismatch, would be larger. It can be predicted with these results that the maximum thermal stress would increase tremendously with the increase of die size or the attaching area. Vertically, the stress attenuates rapidly with the distance from the interface. At the die center region the stress near the die surface attenuates by a factor of 1/80 with respect to the stress at the interface. This picture of the thermal stress distribution indicates that flip-chip bonding would not be recommended for high-temperature MEMS

TABLE 23.1 Basic Material Properties of SiC, Au, 96% Alumina and AlN Used for FEA Simulation for Die-Attach Structure

Temp (deg C)	CIE (×E–6/C)	E (×E6 psi)	
	AIN Material Properties		
–15	3.14	50.00	0.25
20	3.90	50.00	0.25
105	5.36	50.00	0.25
205	6.51	50.00	0.25
305	7.25	50.00	0.25
405	7.76	50.00	0.25
505	8.25	50.00	0.25
605	8.72	50.00	0.25
705	9.09	50.00	0.25
	Au Material Properties		
–15	14.04	11.09	0.44
20	14.24	10.99	0.44
105	14.71	10.83	0.44
205	15.23	10.59	0.44
305	15.75	10.28	0.44
405	16.29	9.92	0.44
505	16.89	9.51	0.44
605	17.58	9.03	0.44
705	18.38	8.50	0.44
	96% Alumina Properties		
–15	5.34	44.00	0.21
20	6.20	44.00	0.21
105	7.83	43.58	0.21
205	8.48	43.06	0.21
305	8.89	42.51	0.21
405	9.28	41.93	0.21
505	9.65	41.34	0.21
605	10.00	40.74	0.21
705	10.33	40.13	0.21
	SiC Material Properties		
–15	2.93	66.72	0.3
20	3.35	66.72	0.3
105	3.97	66.42	0.3
205	4.23	66.08	0.3
305	4.46	65.74	0.3
405	4.68	65.39	0.3
505	4.89	65.05	0.3
605	5.10	64.71	0.3
705	5.29	64.36	0.3

devices if the CTE mismatch is not well controlled, and a significantly thicker die (or a stress buffer layer of the same material as that of the chip) can reduce the thermal stress at the die surface region.

Figure 23.8c shows equivalent plastic strain (EPS) in the Au thick-film layer. Because of the same physical mechanism as that for the SiC die, the highest EPS in the Au layer is located in an area close to the corner where the DNP is larger. This indicates again that a smaller die size or attaching area may better satisfy die-attach thermomechanical reliability requirements.

23.4.2.3 Effects of Substrate Material

In comparison with the AlN substrate, a 96% Al_2O_3 substrate has relatively higher CTE (~6.2×10^{-6}/°C compared with ~3.9×10^{-6}/°C of AlN). In order to evaluate the substrate material effects on the thermomechanical stress of the die-attach structure, FEA simulation was used to compare the maximum stress in both the SiC die and the gold thick-film attaching layer using both substrates [Lin, 2001]. The results indicate that using AlN substrate would result in an improvement of maximum Von-Mises stress in the SiC die by a factor of 0.29, an improvement of Von-Mises stress in the substrate by a factor of

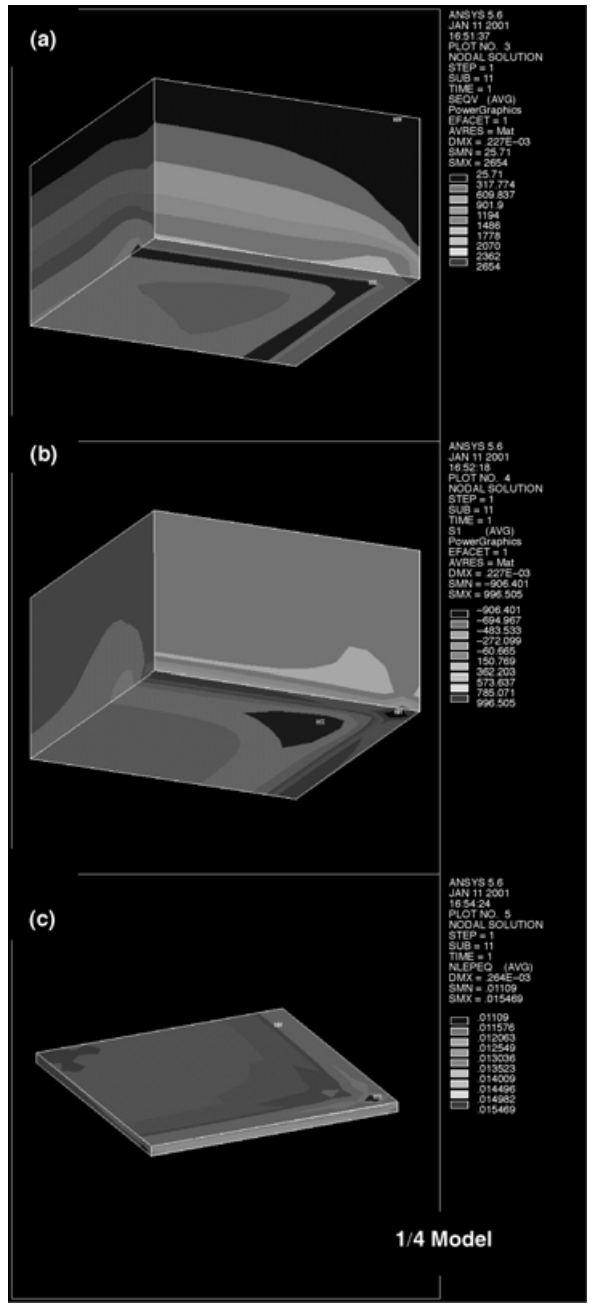


FIGURE 23.8 (Color figure follows p. **12**-26.) Thermal stress and strain distribution in SiC die and Au thick-film layer. (a) Von-Mises stress distribution in SiC die; (b) principle stress distribution in SiC die; (c) equivalent plastic strain in Au thick-film layer.

0.33, and an improvement of MPS in the Au thick-film layer by a factor of 0.42 assuming the yield strength of Au thick-film is 3000 psi. This improvement of thermal stress–strain corresponds to an improvement of fatigue lifetime by a factor of 4.3 to 9.0 (assuming that the power law exponent in the Coffin–Mason model, C, is -0.4 and -0.6, respectively). So, in terms of the thermomechanical reliability of the die-attach, AlN is suggested for packaging SiC high-temperature MEMS devices when compared to 96% Al_2O_3 owing to the fact that the CTE of AlN is closer to that of SiC.

SiC is another candidate substrate material for packaging SiC devices, but currently the cost of single-crystal SiC material is much higher compared with other ceramics suitable for packaging. The CTEs of α- and β-polycrystalline SiC are very close to that of single-crystal SiC so thermomechanically they are ideal substrates for packaging large SiC die for high-temperature operation. However, both the dielectric constants and the dissipation factors of these materials are relatively high [Johnson, 1999]. In order to be used as packaging substrates, the surface properties of polycrystalline SiC must be modified, but these materials might still be suitable only for low-frequency application because of the high dissipation factors.

23.4.2.4 Effects of Thickness of the Attaching Layer

The Au attaching layer contributes to the thermomechanical properties of the die-attach structure in two ways:

1. *Direct interface effect*. The Au layer forms interfaces with both the SiC die and the substrate, so the material properties and the configurations of the Au layer directly influence the thermal stress distributions in both the die and the substrate.
2. *Coupling effects*. As an interlayer between the die and the substrate, the Au layer couples the die with the substrate mechanically.

When the interlayer is very thick, the substrate and die are decoupled from each other, thus the second effect vanishes and the first effect dominates; if the thickness of the interlayer $\rightarrow 0$, then the die and the substrate are directly coupled with each other, the influence of Au material properties vanishes, and the second effect dominates.

Figure 23.9 shows maximum Von-Mises stress in the SiC die and the substrates vs. the thickness of the Au attaching layer, θ_a. The maximum stress in the SiC die decreases by a factor of 0.75 with respect to the change in θ_a from 20 to 50 μm for an AlN substrate, while the maximum Von-Mises stress in the SiC die decreases by a factor of 0.5 with respect to the change in θ_a from 20 to 50 μm for the alumina substrate. The increase of Au layer thickness also significantly reduces the stress in the alumina substrate, as shown in Figure 23.9b. Figure 23.9c shows the maximum equivalent plastic strain in the Au layer vs. θ_a. The increase of θ_a from 20 to 50 μm significantly reduces the EPS in the Au layer in both AlN and Al_2O_3 cases. The maximum stress in SiC die and the substrate and EPS in Au attaching layer were calculated against the yield strength of Au thick-film.

23.4.2.5 Effects of Relaxing Temperature

In addition to the dependence of thermal stress in the die-attach on material properties of the die, the attaching layer and the substrate, the thermomechanical stress in the die-attach structure also depends on the temperature deviation from the relaxing temperature, T_R, at which the structure is largely relaxed. Therefore, the relaxing temperature of the die-attach structure is another important factor determining thermomechanical configuration (stress and strain) of a die-attach structure at a certain temperature. Generally, the more the temperature deviates from the relaxing temperature, the higher the thermomechanical stress that exists in the die-attach structure. For the type of die-attaching using diffusion-based bonding (e.g., thick-film-material-based die-attaching), the relaxing temperature is likely to be close to the processing (curing) temperature. For phase-transition-phenomena-based die-attach processes, the residual thermal stress could exist at the processing/attaching temperature because of the changes in material properties during the phase transition. In this case, the die-attach structure reaches a minimum stress configuration at certain temperature but the residual stress may not be completely relaxed.

In order to assess the relaxing temperature effects on the thermal stress of die-attach structure, the stress distribution of the die-attach at room temperature is simulated by FEA assuming that the structure is relaxed at various temperatures (from 300 to 600°C). Figure 23.10 shows the maximum Von-Mises stress in the die and EPS in the Au thick-film layer vs. the relaxing temperature. If the relaxing temperature could be lowered from 600 to 300°C, the maximum Von-Mises stress in the die could be reduced by a factor of 0.8, and the maximum EPS in the Au thick-film layer could be reduced by a factor of 0.5. The fatigue lifetime corresponding to the stress reduction is improved by a factor of 3 (assuming the exponent

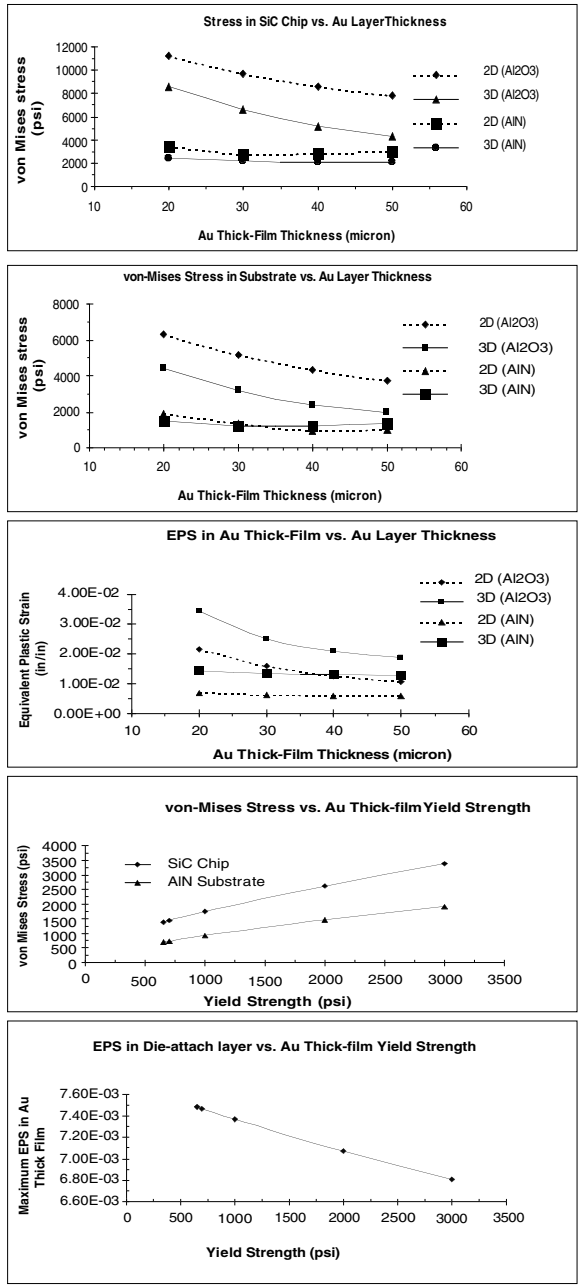
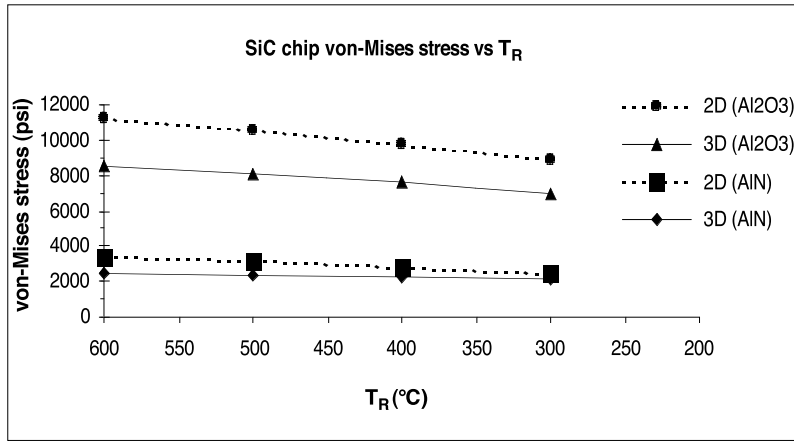
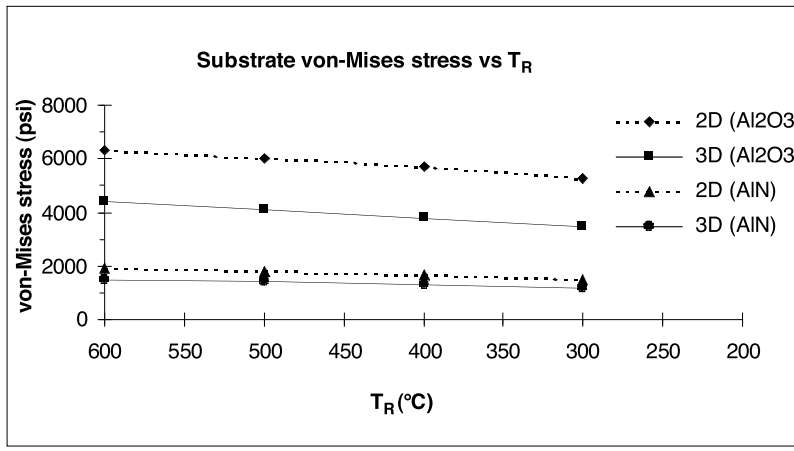


FIGURE 23.9 Dependence of stress–strain in SiC die, substrate and Au attaching layer on the thickness and the yield strength of Au thick-film layer. (From Lin, 2001. With permission.)

in the Coffin-Mason model of fatigue, C, is –0.6). Ideally, the thermal mechanical property of the die-attach structure is optimized if the relaxing temperature could be set at the middle of the operation temperature range, but physically this is not always realistic.

Mathematically, optimization of the thermomechanical property of a die-attach is a complicated multi-parameter problem. So, even if the numerical computing is possible, both the skill and the amount of calculations required for the optimization can be considerable.





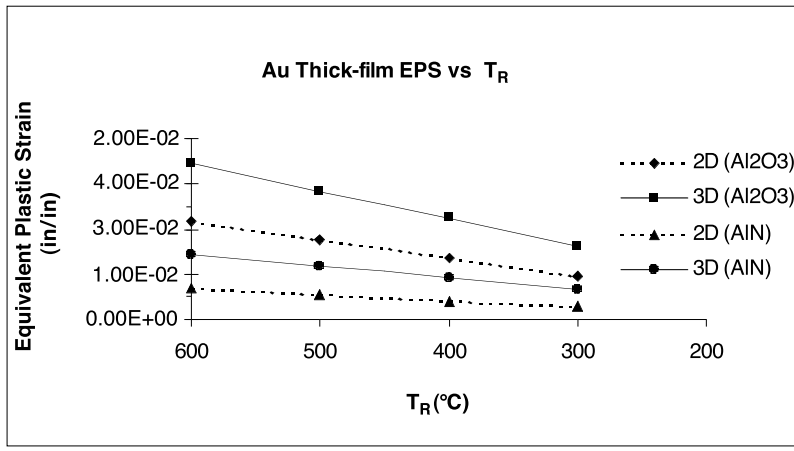


FIGURE 23.10 Relaxing temperature dependence of maximum stress and strain in SiC chip, substrate and Au attaching layer. (From Lin, 2001. With permission.)

23.5 Discussion

The combination of versatile functions of MEMS devices and survivability/operability in harsh environments leads to a new generation of microdevices, harsh-environment MEMS, with revolutionary capabilities for aerospace and civil applications. Packaging these revolutionary devices, however, has generated new and challenging research in the device-packaging field. In order to meet these challenges, innovative packaging materials with superior physical/chemical properties suitable for harsh-environment operation, innovative packaging structures and designs to meet the requirements of microstructures and micromechanical operations and innovative packaging processes to utilize these innovative packaging materials to fabricate innovative packaging structures are expected.

23.5.1 Innovative Materials

An ideal die-attaching material suitable for use in a wide temperature range is an illustration of the need for innovative materials to package harsh-environment MEMS devices. In addition to the superior chemical and electrical stabilities at high temperatures and in a corrosive environment, the die-attaching materials must possess good thermal and electrical conductivity, unique features of metallic material; meanwhile, the CTE of such a material should match those of the die and the ceramic substrate. Ideally, if the CTE of the substrate slightly mismatches that of the die, the die-attach material should be able to compensate the CTE mismatch between the die and the substrate. A material with low Young's modulus and narrow elastic region certainly would help to absorb thermal strain, thus reducing the stresses in the die and the substrate. However, this would reduce the lifetime of the die-attach material layer in a dynamic thermal environment because of the accumulated permanent strain. Comparing the extraordinary material requirements listed above with the features of carbon nano tubes (CNT) we discover that CNT is an ideal die-attach interlayer that matches all these requirements: CNTs have been reported to have superior electrical and thermal conductivities [Saito et al., 1998; Hone et al., 2000]. The longitudinal mechanical strength (both elastic modulus and breaking point) of CNTs is very high in comparison with steel [Wong et al., 1997; Hernandez et al., 1998; Poncharal et al., 1999; Salvetat et al., 1999; Yu et al., 2000], but the shear modulus of single-walled CNTs is low [Salvetat, 1999]. The graphitic bond between neighboring in-wall carbon atoms of each CNT makes the interaction between the neighboring tube walls weak [Girifalco et al., 2000]. Combining all these features of CNTs we can visualize an innovative die-attaching interlayer material. If CNT can be vertically grown on the C face of a SiC (the C face of a SiC is usually used for die-attach because the Si face is favored for fabrication of most electronic devices) wafer, it may provide an ideal interlayer with excellent thermal and electrical conductivities, superior mechanical strength and very low lateral Young's modulus and thus possess the unique capability to manage the CTE mismatch between the die and the substrate. A schematic diagram using CNT as die-attach interlayer that is expected to decouple the die mechanically from the substrate is illustrated in Figure 23.11.

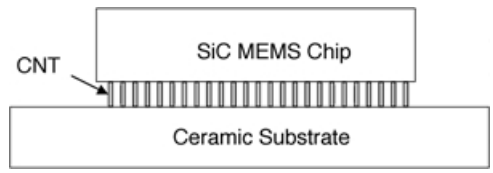


FIGURE 23.11 Schematic diagram of die-attach structure using carbon nano tube as an interlayer with capability to match the CTEs of both SiC chip and the substrate.

23.5.2 Innovative Structures

As discussed in previous sections, suppressing thermal stress in the die-attach in a wide temperature range is a common thermomechanical concern for high-temperature MEMS packaging. A bellow structure was invented (for conventional MEMS packaging) to absorb thermal strain and thus release thermal stress in the area where the device operates mechanically [Garcia and Sniegowski, 1995]. The bellow structure can be fabricated between the mechanical operation part and the chip base so the mechanical operation part is mechanically decoupled laterally from the rest of the device chip. Or, the bellow structure can be fabricated between the device chip and the packaging substrate so the entire chip is mechanically decoupled from the packaging environment. A similar structure can also be used for harsh-environment MEMS packaging. Various thermal stress suppression methods for packaging conventional MEMS were summarized by Madou (1997). Some of these methods may be modified for applications in packaging high-temperature MEMS.

As discussed in Section 23.4.2.2, the thermomechanical stress in the SiC die of the die-attach structure discussed in the last section attenuates rapidly with the vertical distance to the interface composed of SiC and Au with different CTEs. Horizontally, the maximum thermal stress increases rapidly with the die size or die-attaching area. These results suggest a simple but effective thermal stress suppression method, side die-attach, which attaches the die through one of the die sides to the packaging base rather than the bottom of the die. This die-attach scheme allows a much larger distance from the mechanical operation area to the die-attach interface and reduces the die-attach area. The side die-attach structure is expected to be especially effective to release thermomechanical stress–strain in the direction vertical to the die-attach interface because the chip has no direct restraint in this direction.

23.5.3 Innovative Processes

In order to accommodate the microsize mechanical features of MEMS devices and support their microlevel mechanical operation, the immediate device packaging environment may have to meet micromechanical requirements in both alignment and assembly. An innovative, organic-solution-based, self-assembly method was used to integrate microsized GaAs light emission diodes (LED) onto a micromachined Si substrate [Yeh and Smith, 1994]. GaAs LEDs are suspended in ethanol above a micromachined Si wafer. Macrovibration enables the LEDs to randomly walk in the solution. When a LED hits a vacancy on the Si wafer it fits in and gains the lowest potential there because of surface–ethanol–surface interactions. These interactions are so strong that perturbation from vibration would not free trapped LEDs. This is a good example of how innovative packaging processes at various levels beyond conventional IC packaging technology are introduced to package MEMS devices.

Madou (1997) summarized oxidation bonding, fusion bonding, field-assisted thermal bonding and modified field-assisted thermal bonding techniques developed for Si MEMS packaging. Low-pressure and low-temperature hermetic wafer bonding using microwave heating was introduced for Si wafer packaging [Budraa et al., 1999]. Some of these wafer-bonding methods may be modified for applications in high-temperature MEMS wafer materials such as SiC.

A microcavity is a common microstructure necessary to support the operation of many MEMS devices such as an absolute pressure sensor or a microresonator [Ikeda et al., 1990; Hanneborg and Øhlckers, 1990]. These microcavities are often included in the device fabrication instead of being assigned later to conventional packaging that typically is macrolevel processing. This reflects the trend that micromachining/fabrication processes initially used only for device fabrication now are also used to package MEMS devices. An extreme example of using microfabrication to package MEMS devices would be wireless "bug sensors" for operations *in vivo* and other harsh environments. The packaged device must be miniaturized; therefore, both the device and the package have to be microfabricated and micro-assembled. These MEMS devices become "self-packaged" because their fabrication and device packaging processes are completely merged [Santos, 1999]. These "self-packaged" MEMS devices may have the unique advantage of material consistency for operation at high temperatures.

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